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Freemove Semiconductor  
 Technical Data

Document Number: MMA20312BV  
 Rev. 2, 9/2014



# Heterojunction Bipolar Transistor Technology (InGaP HBT) High Efficiency/Linearity Amplifier

The MMA20312BV is a 2-stage high efficiency, Class AB InGaP HBT amplifier designed for use as a linear driver amplifier in wireless base station applications as well as an output stage in femtocell or repeater applications. It is suitable for applications with frequencies from 1800 to 2200 MHz such as CDMA, TD-SCDMA, PCS, UMTS and LTE at operating voltages from 3 to 5 V. The amplifier is housed in a cost-effective, surface mount QFN plastic package.

- Typical Performance:  $V_{CC} = 5 \text{ Vdc}$ ,  $I_{CQ} = 70 \text{ mA}$ ,  $P_{out} = 17 \text{ dBm}$

| Frequency | $G_{ps}$<br>(dB) | ACPR<br>(dBc) | PAE<br>(%) | Test Signal |
|-----------|------------------|---------------|------------|-------------|
| 1880 MHz  | 29.0             | -47.4         | 9.1        | TD-SCDMA    |
| 1920 MHz  | 29.0             | -46.7         | 9.0        | TD-SCDMA    |
| 2010 MHz  | 27.4             | -52.0         | 9.3        | TD-SCDMA    |
| 2025 MHz  | 26.8             | -50.0         | 9.5        | TD-SCDMA    |
| 2140 MHz  | 27.0             | -51.7         | 9.4        | W-CDMA      |

MMA20312BVT1

1800-2200 MHz, 27.2 dB  
 30.5 dBm  
 InGaP HBT LINEAR AMPLIFIER



QFN 3 x 3

## Features

- Frequency: 1800-2200 MHz
- P1dB: 30.5 dBm @ 2140 MHz (CW Application Circuit)
- Power Gain: 26.4 dB @ 2140 MHz (CW Application Circuit)
- OIP3: 44.5 dBm @ 2140 MHz (W-CDMA Application Circuit)
- Active Bias Control (adjustable externally)
- Single 3 to 5 V Supply
- Cost-effective 12-pin, 3 mm QFN Surface Mount Plastic Package
- In Tape and Reel. T1 Suffix = 1,000 Units, 12 mm Tape Width, 7-inch Reel.

Table 1. Typical Performance (1)

| Characteristic                 | Symbol | 1800<br>MHz | 2140<br>MHz | 2200<br>MHz | Unit |
|--------------------------------|--------|-------------|-------------|-------------|------|
| Small-Signal Gain (S21)        | $G_p$  | 28.8        | 26.4        | 25.5        | dB   |
| Input Return Loss (S11)        | IRL    | -17.6       | -10.9       | -9.7        | dB   |
| Output Return Loss (S22)       | ORL    | -20.3       | -14.7       | -13.7       | dB   |
| Power Output @ 1dB Compression | P1dB   | 30.5        | 30.5        | 30.5        | dBm  |

1.  $V_{CC1} = V_{CC2} = V_{BIAS} = 5 \text{ Vdc}$ ,  $T_A = 25^\circ\text{C}$ , 50 ohm system, CW Application Circuit

Table 2. Maximum Ratings

| Rating                    | Symbol    | Value       | Unit             |
|---------------------------|-----------|-------------|------------------|
| Supply Voltage            | $V_{CC}$  | 6           | V                |
| Supply Current            | $I_{CC}$  | 550         | mA               |
| RF Input Power            | $P_{in}$  | 14          | dBm              |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | $^\circ\text{C}$ |
| Junction Temperature      | $T_J$     | 175         | $^\circ\text{C}$ |

Table 3. Thermal Characteristics

| Characteristic                                                                                                               | Symbol          | Value (2) | Unit               |
|------------------------------------------------------------------------------------------------------------------------------|-----------------|-----------|--------------------|
| Thermal Resistance, Junction to Case<br>Case Temperature $86^\circ\text{C}$ , $V_{CC1} = V_{CC2} = V_{BIAS} = 5 \text{ Vdc}$ | $R_{\theta JC}$ | 52        | $^\circ\text{C/W}$ |

2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>.  
 Select Documentation/Application Notes - AN1955.

**Table 4. Electrical Characteristics** ( $V_{CC1} = V_{CC2} = V_{BIAS} = 5$  Vdc, 2140 MHz,  $T_A = 25^\circ\text{C}$ , 50 ohm system, in Freescale W-CDMA Application Circuit)

| Characteristic                                  | Symbol   | Min  | Typ   | Max | Unit |
|-------------------------------------------------|----------|------|-------|-----|------|
| Small-Signal Gain (S21) <sup>(1)</sup>          | $G_p$    | 23.6 | 27.2  | —   | dB   |
| Input Return Loss (S11)                         | IRL      | —    | -10.7 | —   | dB   |
| Output Return Loss (S22)                        | ORL      | —    | -15.5 | —   | dB   |
| Power Output @ 1dB Compression, CW              | P1dB     | —    | 28.2  | —   | dBm  |
| Third Order Output Intercept Point, Two-Tone CW | OIP3     | —    | 44.5  | —   | dBm  |
| Noise Figure                                    | NF       | —    | 3.3   | —   | dB   |
| Supply Current <sup>(1)</sup>                   | $I_{CQ}$ | 62.5 | 70    | 77  | mA   |
| Supply Voltage                                  | $V_{CC}$ | —    | 5     | —   | V    |

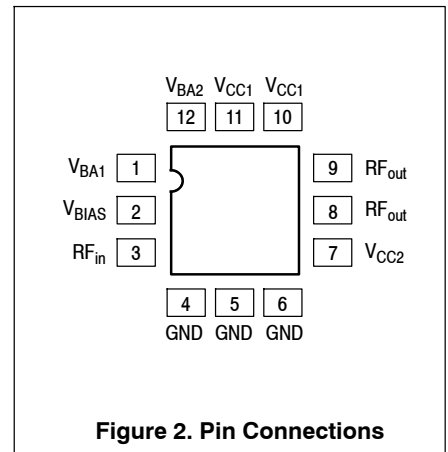
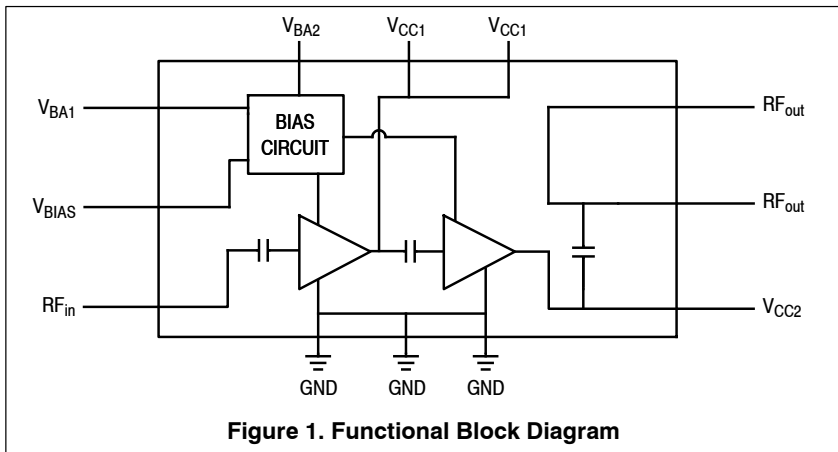
**Table 5. ESD Protection Characteristics**

| Test Methodology                      | Class             |
|---------------------------------------|-------------------|
| Human Body Model (per JESD22-A114)    | 0, rated to 150 V |
| Machine Model (per EIA/JESD22-A115)   | A                 |
| Charge Device Model (per JESD22-C101) | III               |

**Table 6. Moisture Sensitivity Level**

| Test Methodology                     | Rating | Package Peak Temperature | Unit             |
|--------------------------------------|--------|--------------------------|------------------|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3      | 260                      | $^\circ\text{C}$ |

1. Specified data is based on performance of soldered down part in W-CDMA application circuit.



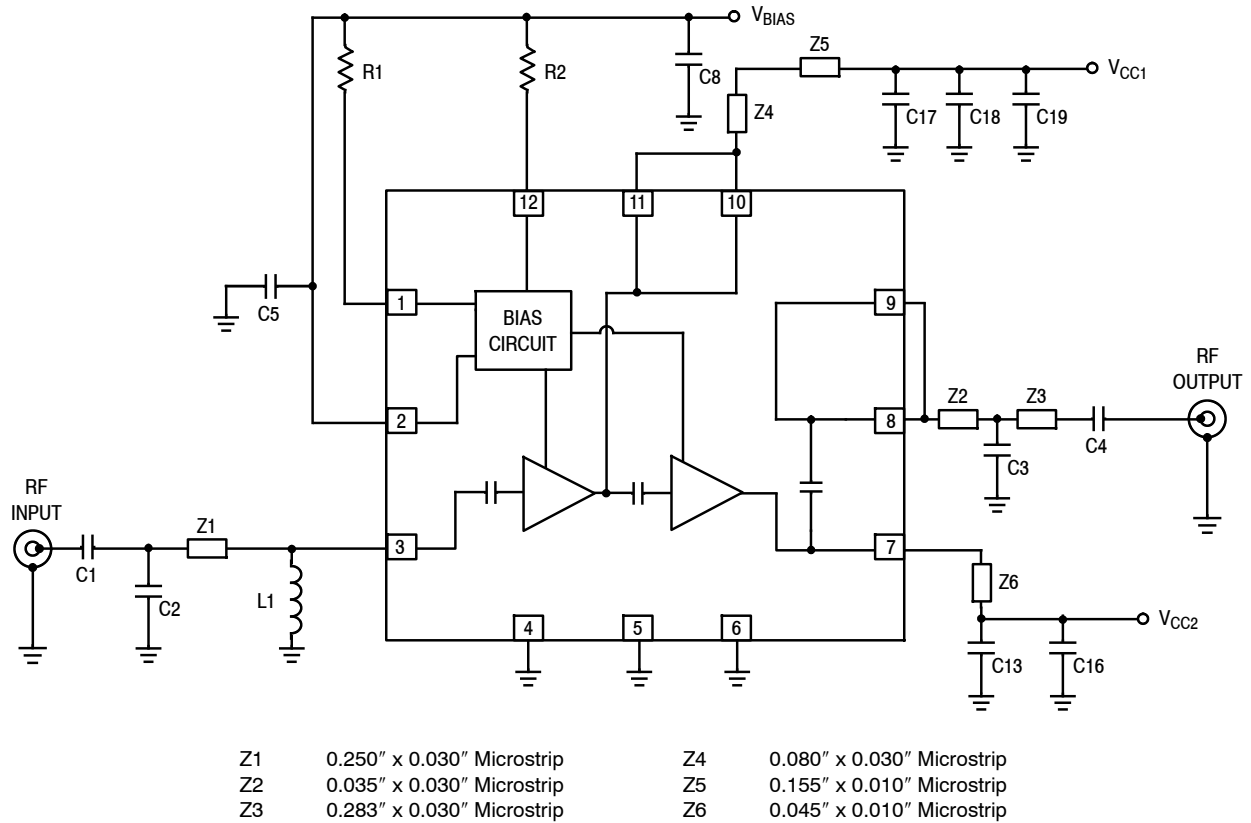
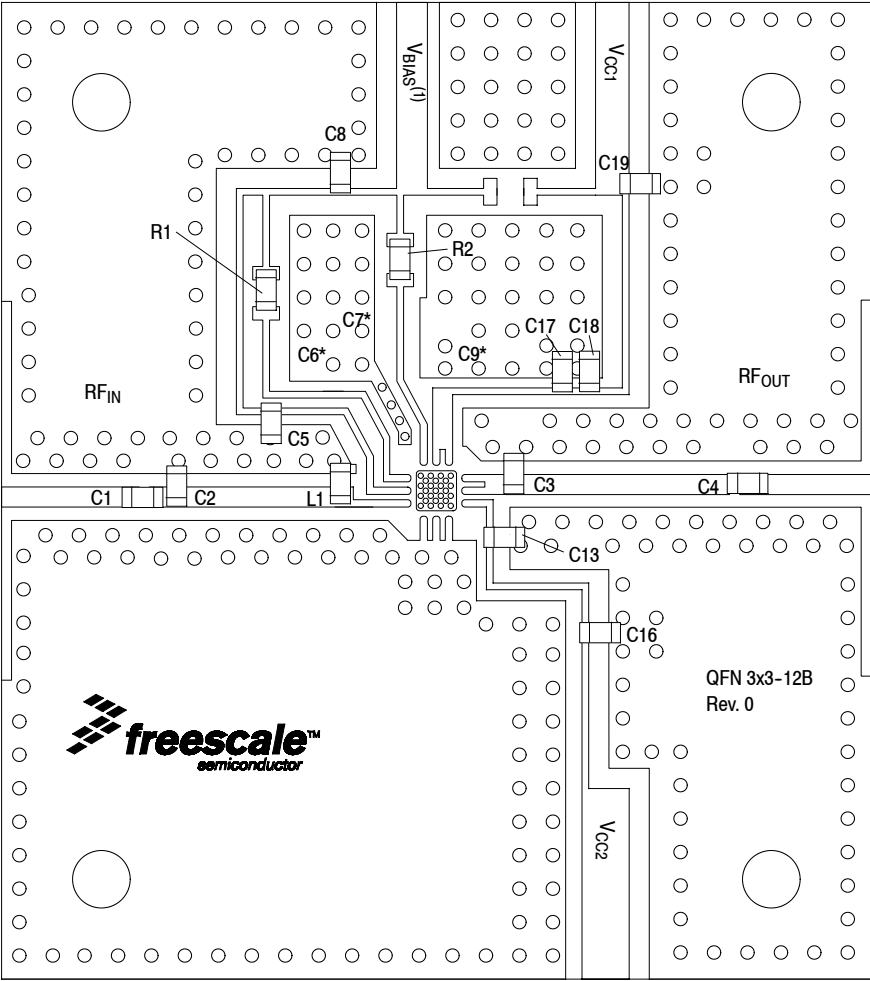


Figure 3. MMA20312BV Test Circuit Schematic — TD-SCDMA, 5 Volt Operation

Table 7. MMA20312BV Test Circuit Component Designations and Values — TD-SCDMA, 5 Volt Operation

| Part       | Description                  | Part Number       | Manufacturer |
|------------|------------------------------|-------------------|--------------|
| C1, C5     | 22 pF Chip Capacitors        | 06033J220GBS      | AVX          |
| C2         | 1.8 pF Chip Capacitor        | 06035J1R8BBS      | AVX          |
| C3         | 2.2 pF Chip Capacitor        | 06035J2R2BBS      | AVX          |
| C4         | 5.6 pF Chip Capacitor        | 06035J5R6BBS      | AVX          |
| C6, C7, C9 | Components Not Placed        |                   |              |
| C8, C18    | 1 $\mu$ F Chip Capacitors    | GRM188R61A105KA61 | Murata       |
| C13        | 10 pF Chip Capacitor         | 06035J100GBS      | AVX          |
| C16, C19   | 10 $\mu$ F Chip Capacitors   | GRM188R60J106ME47 | Murata       |
| C17        | 0.1 $\mu$ F Chip Capacitor   | GRM188R71H104KA93 | Murata       |
| L1         | 1.8 nH Chip Inductor         | LL1608-FS1N8S     | TOKO         |
| R1         | 330 $\Omega$ Chip Resistor   | RR0816Q-331-D     | Susumu       |
| R2         | 1.5 k $\Omega$ Chip Resistor | RR0816Q-152-D     | Susumu       |
| PCB        | 0.01", $\epsilon_r = 3.38$   | 680-338           | Isola        |

Note: Component numbers C6, C7 and C9 are labeled on board but not placed. C10, C11, C12, C14 and C15 are intentionally omitted.



(1) V<sub>BIAS</sub> [Board] supplies V<sub>BA1</sub>, V<sub>BA2</sub> and V<sub>BIAS</sub> [Device].  
 Note: Component numbers C6\*, C7\* and C9\* are labeled on board but not placed.

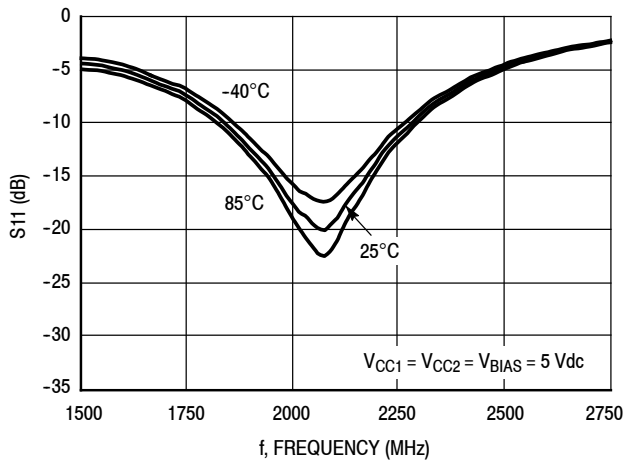
Figure 4. MMA20312BV Test Circuit Component Layout — TD-SCDMA, 5 Volt Operation

Table 7. MMA20312BV Test Circuit Component Designations and Values — TD-SCDMA, 5 Volt Operation

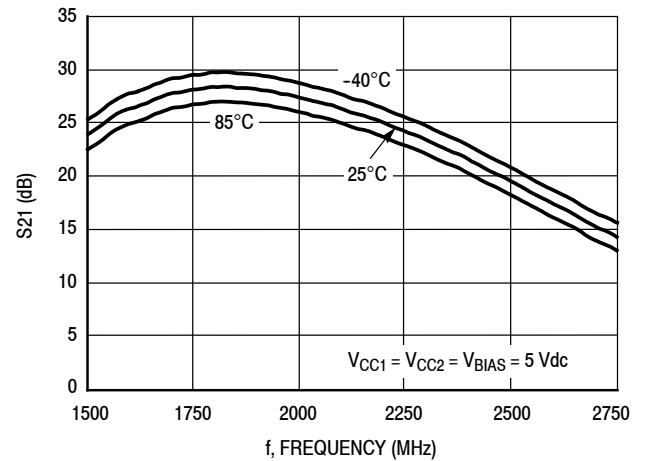
| Part       | Description                  | Part Number       | Manufacturer |
|------------|------------------------------|-------------------|--------------|
| C1, C5     | 22 pF Chip Capacitors        | 06033J220GBS      | AVX          |
| C2         | 1.8 pF Chip Capacitor        | 06035J1R8BBS      | AVX          |
| C3         | 2.2 pF Chip Capacitor        | 06035J2R2BBS      | AVX          |
| C4         | 5.6 pF Chip Capacitor        | 06035J5R6BBS      | AVX          |
| C6, C7, C9 | Components Not Placed        |                   |              |
| C8, C18    | 1 μF Chip Capacitors         | GRM188R61A105KA61 | Murata       |
| C13        | 10 pF Chip Capacitor         | 06035J100GBS      | AVX          |
| C16, C19   | 10 μF Chip Capacitors        | GRM188R60J106ME47 | Murata       |
| C17        | 0.1 μF Chip Capacitor        | GRM188R71H104KA93 | Murata       |
| L1         | 1.8 nH Chip Inductor         | LL1608-FS1N8S     | TOKO         |
| R1         | 330 Ω Chip Resistor          | RR0816Q-331-D     | Susumu       |
| R2         | 1.5 kΩ Chip Resistor         | RR0816Q-152-D     | Susumu       |
| PCB        | 0.01", ε <sub>r</sub> = 3.38 | 680-338           | Isola        |

Note: Component numbers C10, C11, C12, C14 and C15 are intentionally omitted.  
 (Test Circuit Component Designations and Values table repeated for reference.)

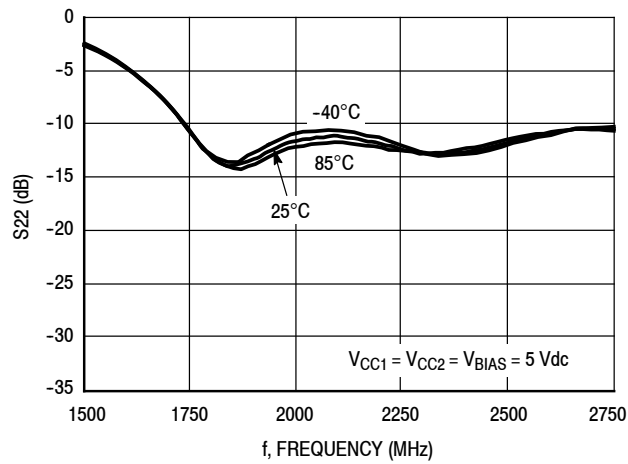
### TYPICAL CHARACTERISTICS — TD-SCDMA



**Figure 5. S11 versus Frequency versus Temperature**

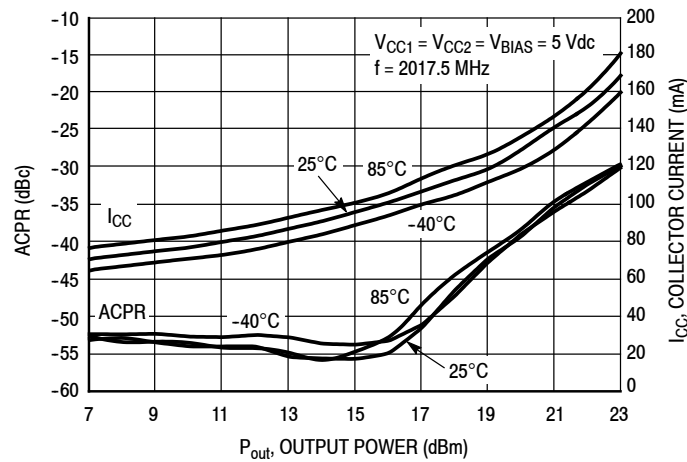


**Figure 6. S21 versus Frequency versus Temperature**

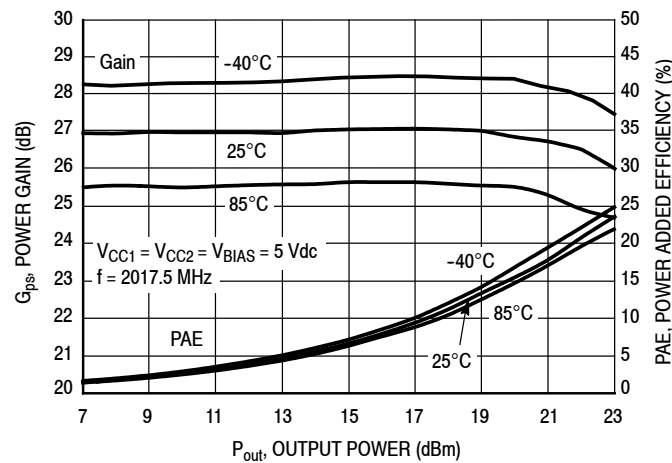


**Figure 7. S22 versus Frequency versus Temperature**

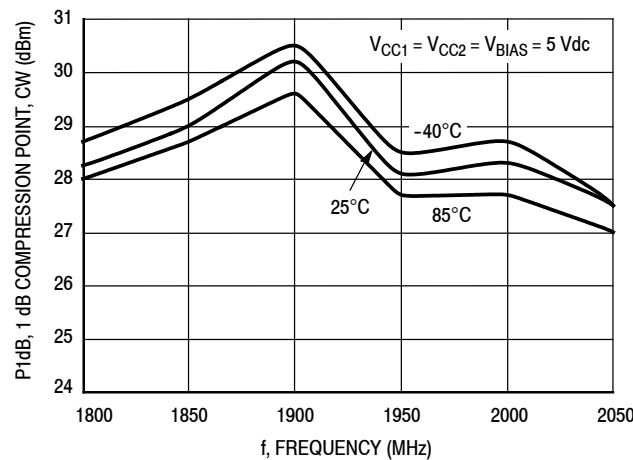
### TYPICAL CHARACTERISTICS — TD-SCDMA



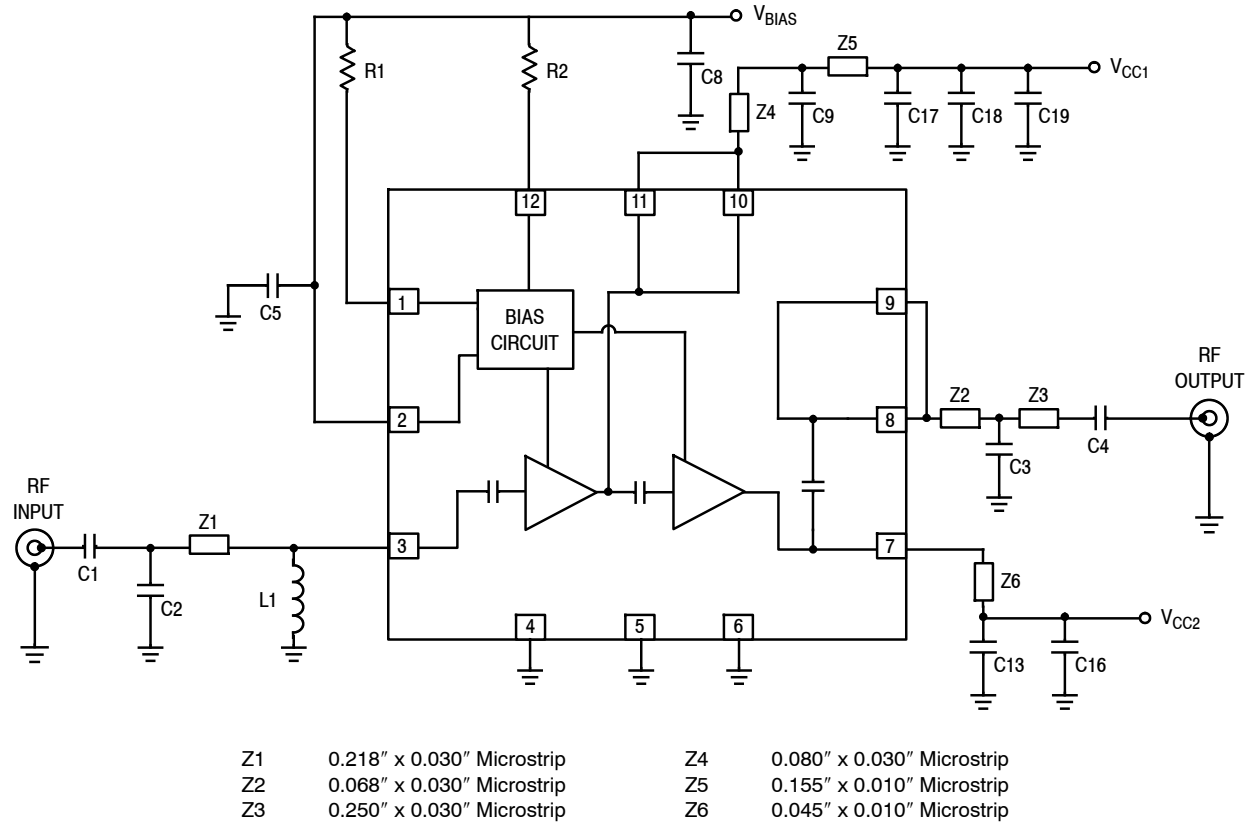
**Figure 8. ACPR versus Collector Current versus Output Power versus Temperature**



**Figure 9. Power Gain versus Power Added Efficiency versus Output Power versus Temperature**



**Figure 10. P1dB versus Frequency versus Temperature, CW**

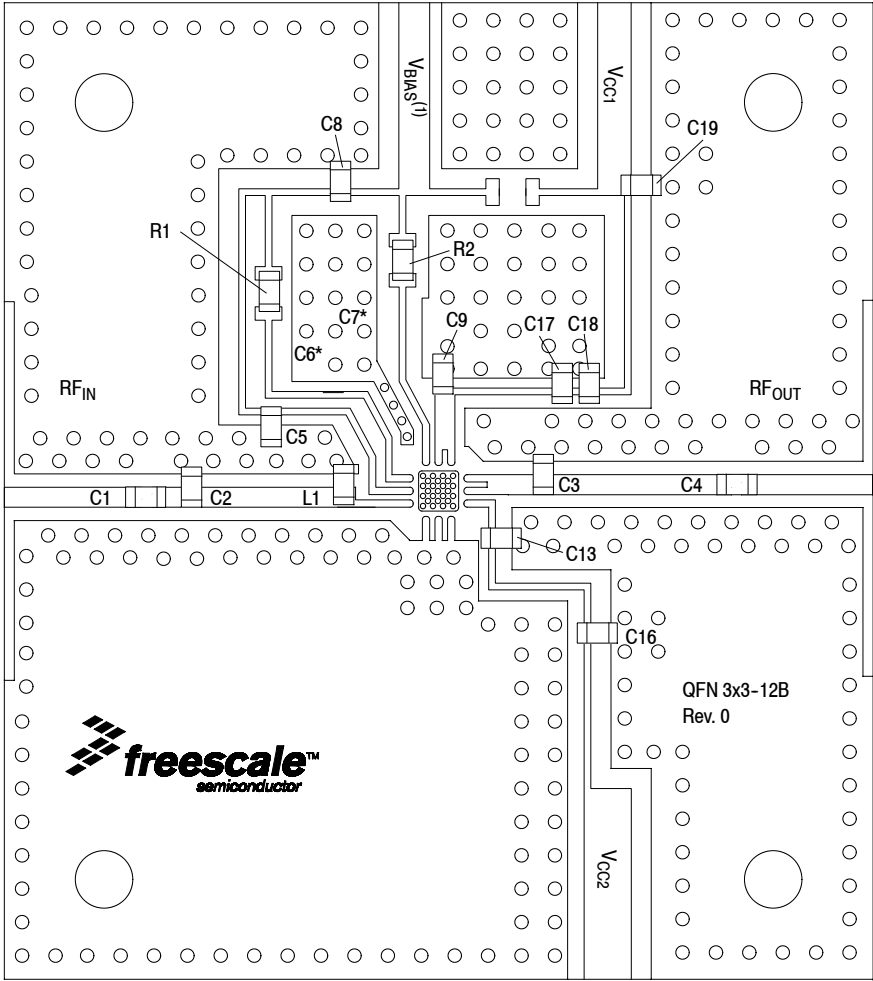


**Figure 11. MMA20312BV Test Circuit Schematic — W-CDMA, 5 Volt Operation**

**Table 8. MMA20312BV Test Circuit Component Designations and Values — W-CDMA, 5 Volt Operation**

| Part     | Description                 | Part Number       | Manufacturer |
|----------|-----------------------------|-------------------|--------------|
| C1, C5   | 22 pF Chip Capacitors       | 06033J220GBS      | AVX          |
| C2, C3   | 1.8 pF Chip Capacitors      | 06035J1R8BBS      | AVX          |
| C4       | 5.6 pF Chip Capacitor       | 06035J5R6BBS      | AVX          |
| C6, C7   | Components Not Placed       |                   |              |
| C8, C18  | 1 $\mu$ F Chip Capacitors   | GRM188R61A105KA61 | Murata       |
| C9       | 100 pF Chip Capacitor       | GRM1885C1H101JA01 | Murata       |
| C13      | 10 pF Chip Capacitor        | 06035J100GBS      | AVX          |
| C16, C19 | 10 $\mu$ F Chip Capacitors  | GRM188R60J106ME47 | Murata       |
| C17      | 0.1 $\mu$ F Chip Capacitor  | GRM188R71H104KA93 | Murata       |
| L1       | 1.8 nH Chip Inductor        | LL1608-FS1N8S     | TOKO         |
| R1       | 330 $\Omega$ Chip Resistor  | RR0816Q-331-D     | Susumu       |
| R2       | 1500 $\Omega$ Chip Resistor | RR0816Q-152-D     | Susumu       |
| PCB      | 0.01", $\epsilon_r = 3.38$  | 680-338           | Isola        |

Note: Component numbers C6 and C7 are labeled on board but not placed. C10, C11, C12, C14 and C15 are intentionally omitted.



(1) V<sub>BIAS</sub> [Board] supplies V<sub>BA1</sub>, V<sub>BA2</sub> and V<sub>BIAS</sub> [Device].  
 Note: Component numbers C6\* and C7\* are labeled on board but not placed.

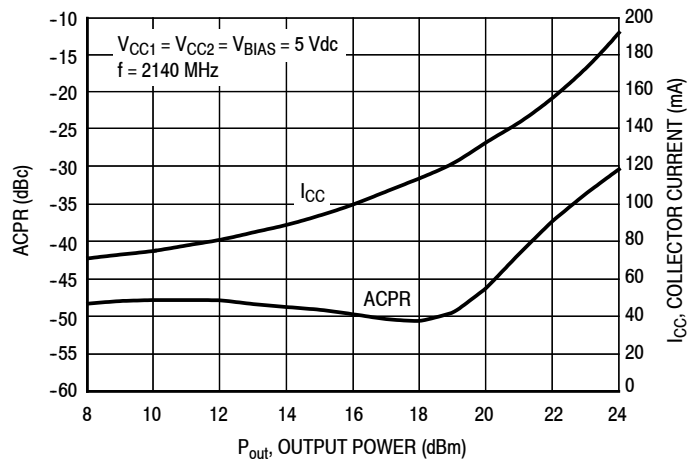
Figure 12. MMA20312BV Test Circuit Component Layout — W-CDMA, 5 Volt Operation

Table 8. MMA20312BV Test Circuit Component Designations and Values — W-CDMA, 5 Volt Operation

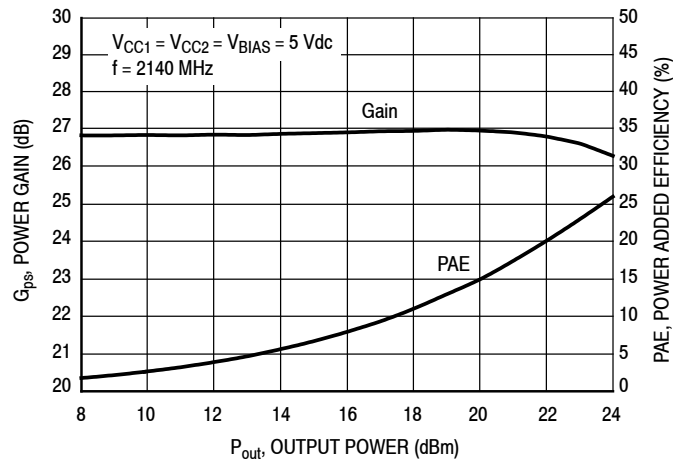
| Part     | Description                 | Part Number       | Manufacturer |
|----------|-----------------------------|-------------------|--------------|
| C1, C5   | 22 pF Chip Capacitors       | 06033J220GBS      | AVX          |
| C2, C3   | 1.8 pF Chip Capacitors      | 06035J1R8BBS      | AVX          |
| C4       | 5.6 pF Chip Capacitor       | 06035J5R6BBS      | AVX          |
| C6, C7   | Components Not Placed       |                   |              |
| C8, C18  | 1 $\mu$ F Chip Capacitors   | GRM188R61A105KA61 | Murata       |
| C9       | 100 pF Chip Capacitor       | GRM1885C1H101JA01 | Murata       |
| C13      | 10 pF Chip Capacitor        | 06035J100GBS      | AVX          |
| C16, C19 | 10 $\mu$ F Chip Capacitors  | GRM188R60J106ME47 | Murata       |
| C17      | 0.1 $\mu$ F Chip Capacitor  | GRM188R71H104KA93 | Murata       |
| L1       | 1.8 nH Chip Inductor        | LL1608-FS1N8S     | TOKO         |
| R1       | 330 $\Omega$ Chip Resistor  | RR0816Q-331-D     | Susumu       |
| R2       | 1500 $\Omega$ Chip Resistor | RR0816Q-152-D     | Susumu       |
| PCB      | 0.01", $\epsilon_r = 3.38$  | 680-338           | Isola        |

Note: Component numbers C10, C11, C12, C14 and C15 are intentionally omitted.  
 (Test Circuit Component Designations and Values table repeated for reference.)

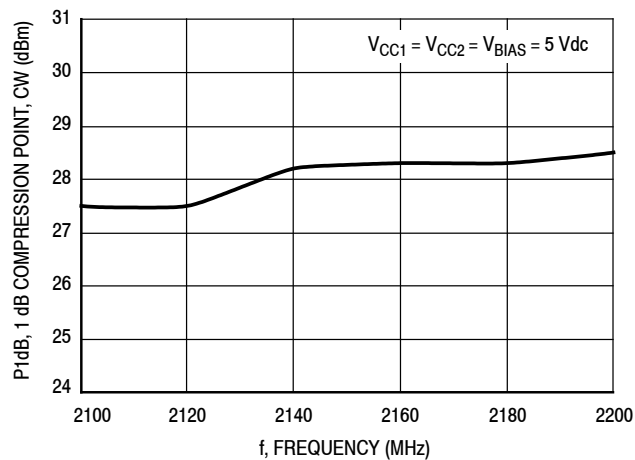
### TYPICAL CHARACTERISTICS — W-CDMA



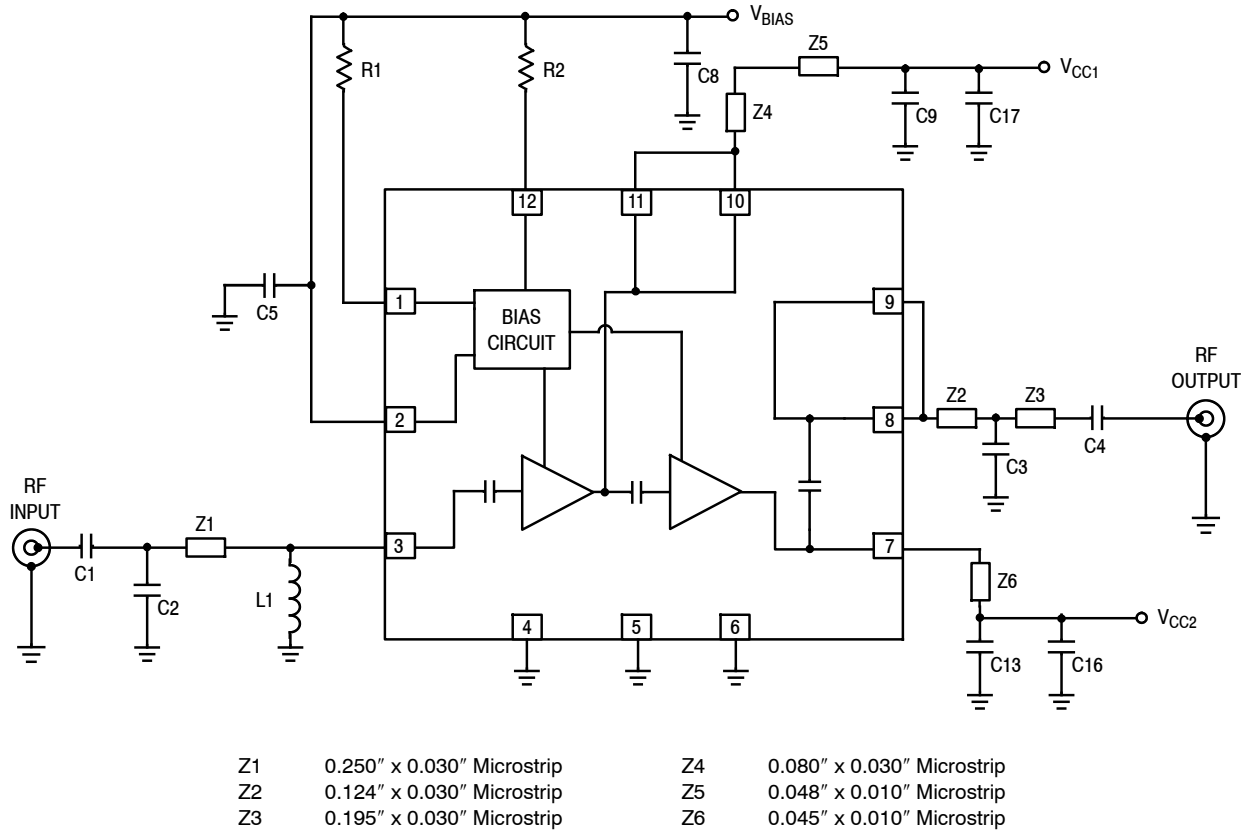
**Figure 13. ACPR versus Collector Current versus Output Power**



**Figure 14. Power Gain versus Power Added Efficiency versus Output Power**



**Figure 15. P1dB versus Frequency, CW**

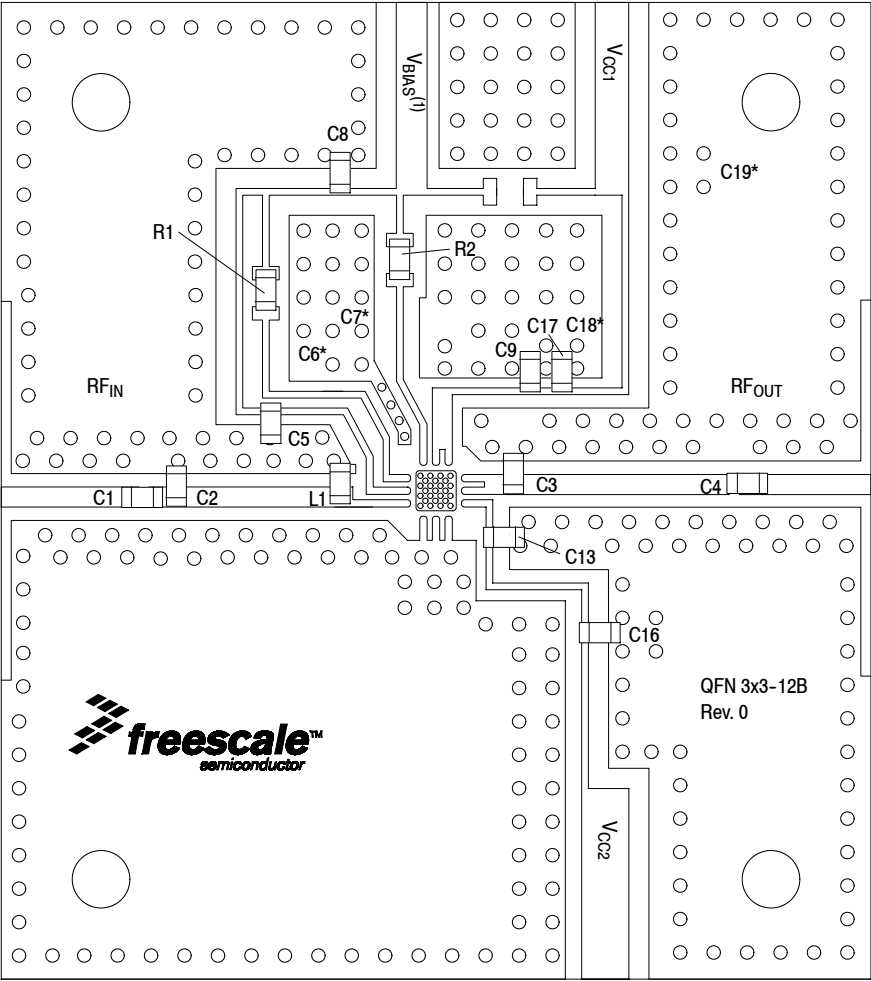


**Figure 16. MMA20312BV Test Circuit Schematic — IS-95, 3.3 Volt Operation**

**Table 9. MMA20312BV Test Circuit Component Designations and Values — IS-95, 3.3 Volt Operation**

| Part             | Description                | Part Number       | Manufacturer |
|------------------|----------------------------|-------------------|--------------|
| C1, C5, C9       | 22 pF Chip Capacitors      | 06033J220GBS      | AVX          |
| C2               | 2.2 pF Chip Capacitor      | 06035J2R2BBS      | AVX          |
| C3               | 2.4 pF Chip Capacitor      | 06035J2R4BBS      | AVX          |
| C4               | 4.7 pF Chip Capacitor      | 06035J4R7BBS      | AVX          |
| C6, C7, C18, C19 | Components Not Placed      |                   |              |
| C8, C17          | 1 $\mu$ F Chip Capacitors  | GRM188R61A105KA61 | Murata       |
| C13              | 10 pF Chip Capacitor       | 06035J100GBS      | AVX          |
| C16              | 4.7 $\mu$ F Chip Capacitor | GRM188R60J106ME47 | Murata       |
| L1               | 1.5 nH Chip Inductor       | LL1608-FS1N5S     | TOKO         |
| R1               | 82 $\Omega$ Chip Resistor  | RR0816Q-820-D     | Susumu       |
| R2               | 510 $\Omega$ Chip Resistor | RR0816Q-511-D     | Susumu       |
| PCB              | 0.01", $\epsilon_r = 3.38$ | 680-338           | Isola        |

Note: Component numbers C6, C7, C18 and C19 are labeled on board but not placed. C10, C11, C12, C14 and C15 are intentionally omitted.



(1) V<sub>BIAS</sub> [Board] supplies V<sub>BA1</sub>, V<sub>BA2</sub> and V<sub>BIAS</sub> [Device].  
 Note: Component numbers C6\*, C7\*, C18\* and C19\* are labeled on board but not placed.

Figure 17. MMA20312BV Test Circuit Component Layout — IS-95, 3.3 Volt Operation

Table 9. MMA20312BV Test Circuit Component Designations and Values — IS-95, 3.3 Volt Operation

| Part             | Description                  | Part Number       | Manufacturer |
|------------------|------------------------------|-------------------|--------------|
| C1, C5, C9       | 22 pF Chip Capacitors        | 06033J220GBS      | AVX          |
| C2               | 2.2 pF Chip Capacitor        | 06035J2R2BBS      | AVX          |
| C3               | 2.4 pF Chip Capacitor        | 06035J2R4BBS      | AVX          |
| C4               | 4.7 pF Chip Capacitor        | 06035J4R7BBS      | AVX          |
| C6, C7, C18, C19 | Components Not Placed        |                   |              |
| C8, C17          | 1 μF Chip Capacitors         | GRM188R61A105KA61 | Murata       |
| C13              | 10 pF Chip Capacitor         | 06035J100GBS      | AVX          |
| C16              | 4.7 μF Chip Capacitor        | GRM188R60J106ME47 | Murata       |
| L1               | 1.5 nH Chip Inductor         | LL1608-FS1N5S     | TOKO         |
| R1               | 82 Ω Chip Resistor           | RR0816Q-820-D     | Susumu       |
| R2               | 510 Ω Chip Resistor          | RR0816Q-511-D     | Susumu       |
| PCB              | 0.01", ε <sub>r</sub> = 3.38 | 680-338           | Isola        |

Note: Component numbers C10, C11, C12, C14 and C15 are intentionally omitted.  
 (Test Circuit Component Designations and Values table repeated for reference.)

TYPICAL CHARACTERISTICS — IS-95

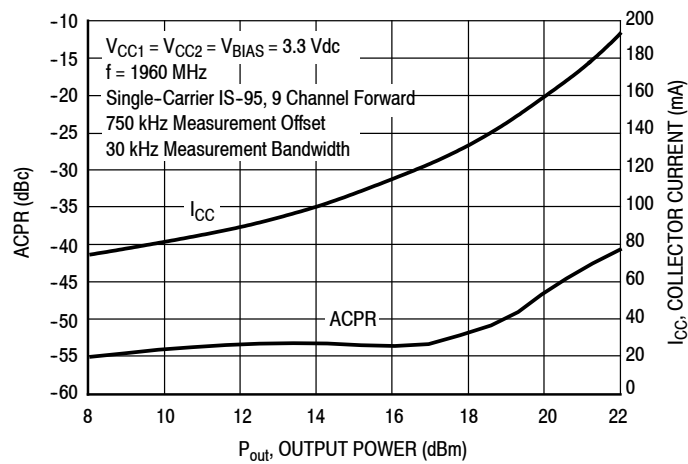


Figure 18. ACPR versus Collector Current  
 versus Output Power

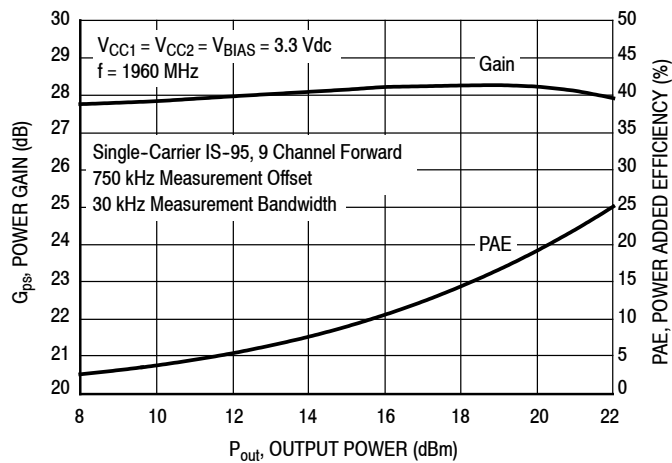


Figure 19. Power Gain versus Power Added  
 Efficiency versus Output Power

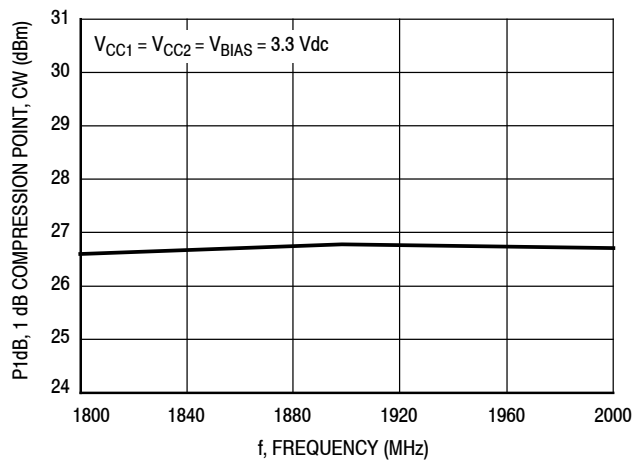
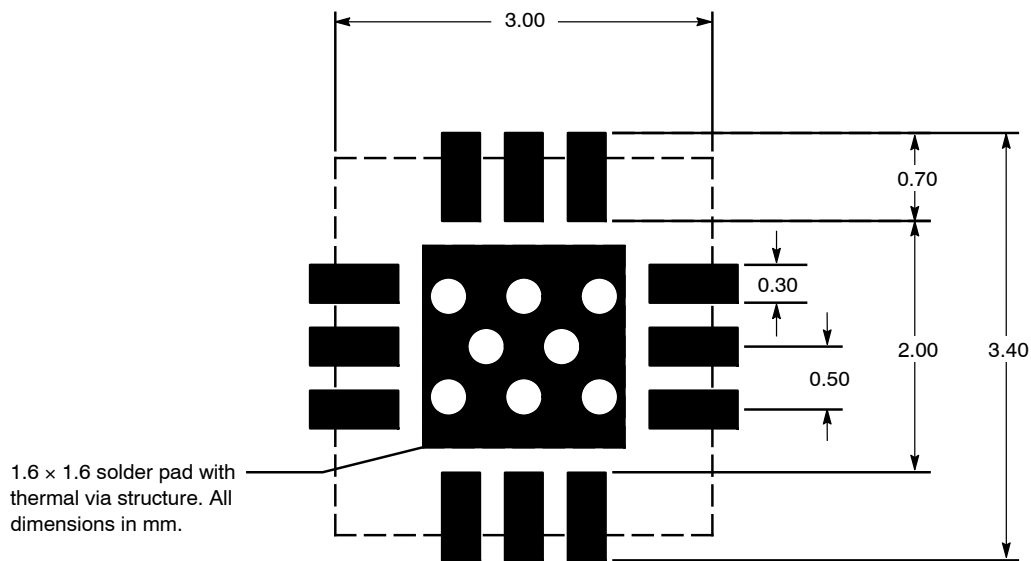


Figure 20. P1dB versus Frequency, CW

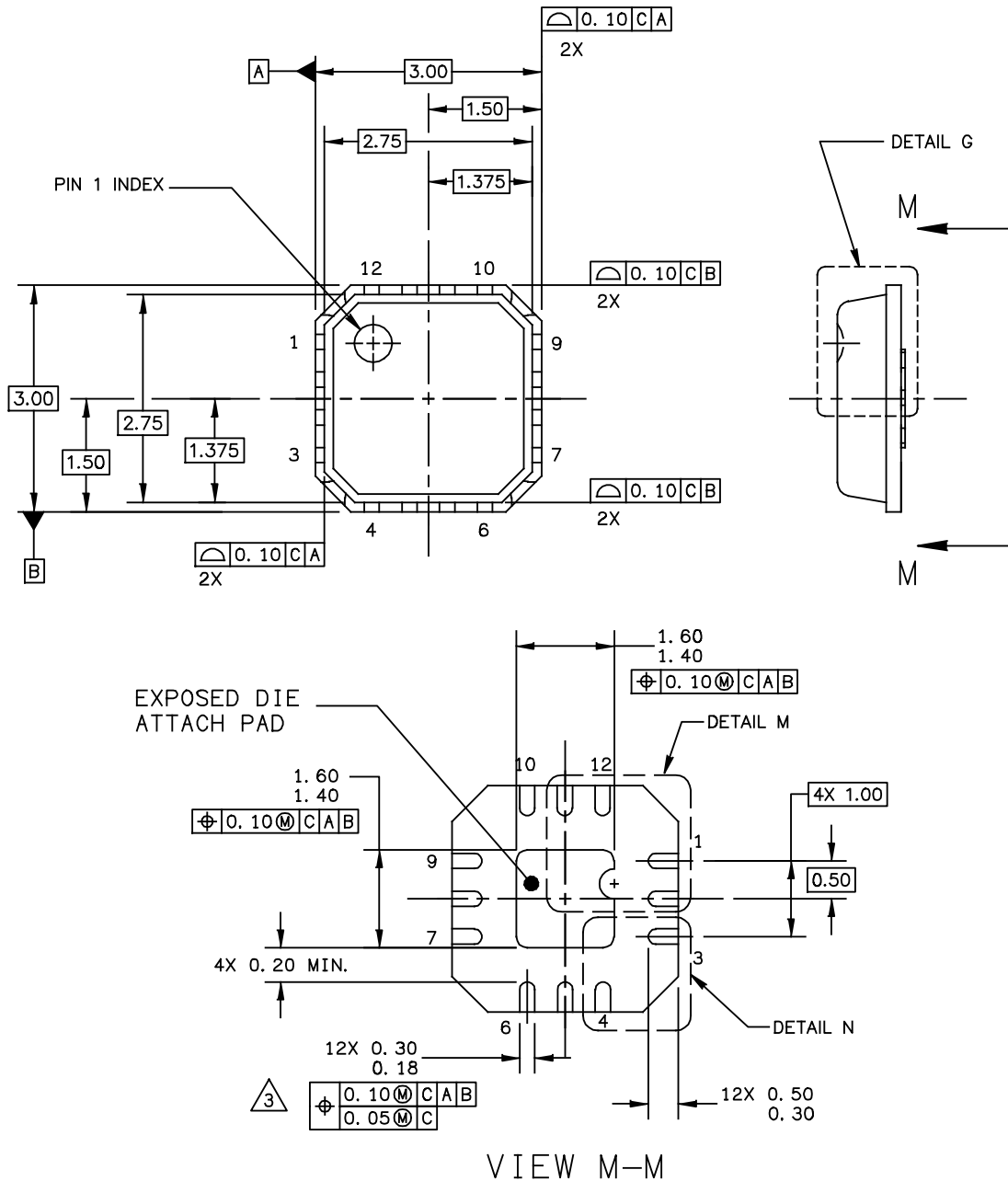


**Figure 21. PCB Pad Layout for QFN 3 x 3**

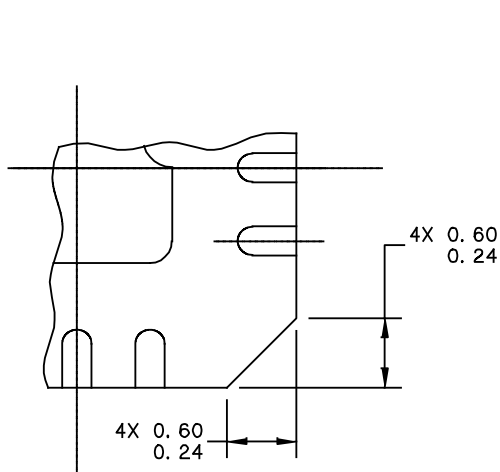


**Figure 22. Product Marking**

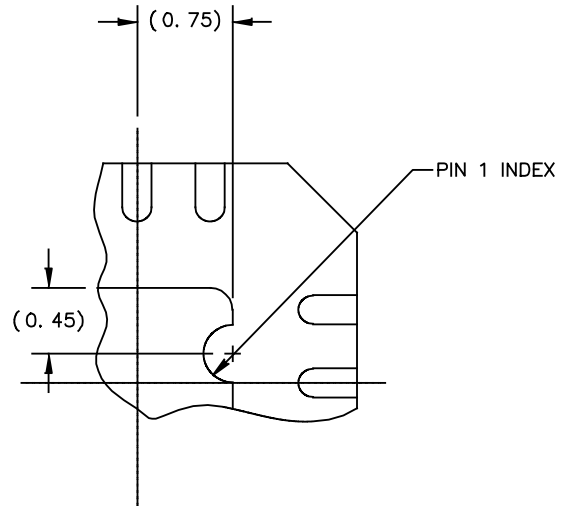
## PACKAGE DIMENSIONS



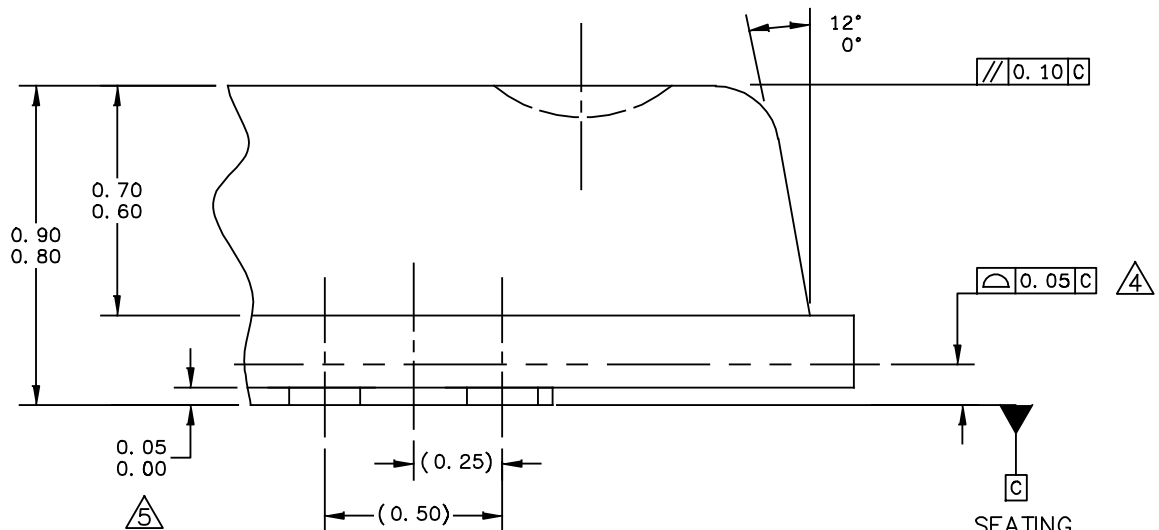
|                                                                                                         |  |                          |  |                            |  |
|---------------------------------------------------------------------------------------------------------|--|--------------------------|--|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                                                 |  | MECHANICAL OUTLINE       |  | PRINT VERSION NOT TO SCALE |  |
| TITLE:<br>THERMALLY ENHANCED QUAD<br>FLAT NON-LEADED PACKAGE (QFN)<br>12 TERMINAL, 0.5 PITCH (3X3X0.85) |  | DOCUMENT NO: 98ASA00227D |  | REV: 0                     |  |
|                                                                                                         |  | CASE NUMBER: 2131-01     |  | 14 MAY 2010                |  |
|                                                                                                         |  | STANDARD: NON-JEDEC      |  |                            |  |



DETAIL N  
CORNER CONFIGURATION



DETAIL M  
PIN 1 BACKSIDE INDEX



DETAIL G  
VIEW ROTATED 90° CW

|                                                                                                         |  |                          |  |                            |  |
|---------------------------------------------------------------------------------------------------------|--|--------------------------|--|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                                                 |  | MECHANICAL OUTLINE       |  | PRINT VERSION NOT TO SCALE |  |
| TITLE:<br>THERMALLY ENHANCED QUAD<br>FLAT NON-LEADED PACKAGE (QFN)<br>12 TERMINAL, 0.5 PITCH (3X3X0.85) |  | DOCUMENT NO: 98ASA00227D |  | REV: 0                     |  |
|                                                                                                         |  | CASE NUMBER: 2131-01     |  | 14 MAY 2010                |  |
|                                                                                                         |  | STANDARD: NON-JEDEC      |  |                            |  |

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING & TOLERANCING PER ASME Y14.5 – 2009.
3. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DIMENSION APPLIED ONLY FOR TERMINALS.

|                                                                                                         |                          |                            |             |
|---------------------------------------------------------------------------------------------------------|--------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                                                 | MECHANICAL OUTLINE       | PRINT VERSION NOT TO SCALE |             |
| TITLE:<br>THERMALLY ENHANCED QUAD<br>FLAT NON-LEADED PACKAGE (QFN)<br>12 TERMINAL, 0.5 PITCH (3X3X0.85) | DOCUMENT NO: 98ASA00227D |                            | REV: 0      |
|                                                                                                         | CASE NUMBER: 2131-01     |                            | 14 MAY 2010 |
|                                                                                                         | STANDARD: NON-JEDEC      |                            |             |

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Software

- .s2p File

### Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the "Part Number" link. Go to Software & Tools on the part's Product Summary page to download the respective tool.

## FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where Freescale is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local Freescale Sales Office.

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0        | Aug. 2011  | <ul style="list-style-type: none"> <li>• Initial Release of Data Sheet</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1        | Dec. 2011  | <ul style="list-style-type: none"> <li>• Updated minimum operating voltage from 3.3 V to 3 V to reflect actual device capability, p. 1</li> <li>• All references to "V<sub>CTRL</sub>" in the data sheet tables, test circuit schematics and component layouts is replaced with "V<sub>BIAS</sub>". V<sub>BIAS</sub> is the supply voltage which sets the internal bias conditions via pins 1, 2, and 12, pp. 1-3, 5-7, 9, 10, 12. Footnote "(1) V<sub>BIAS</sub> [Board] supplies V<sub>BA1</sub>, V<sub>BA2</sub> and V<sub>BIAS</sub> [Device]" added to test circuit component layouts, pp. 4, 8, 11.</li> </ul> |
| 2        | Sept. 2014 | <ul style="list-style-type: none"> <li>• Table 2, Maximum Ratings: updated Junction Temperature from 150°C to 175°C to reflect recent test results of the device, p. 1</li> <li>• Added Failure Analysis information, p. 17</li> </ul>                                                                                                                                                                                                                                                                                                                                                                               |

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