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Texas Instruments
TL5001CDR

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Datasheet of TL5001CDR - IC REG CTRLR PWM 8SOIC

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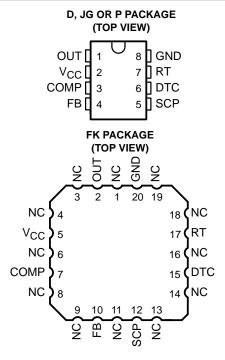
TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS084F - APRIL 1994 - REVISED JANUARY 2002

- Complete PWM Power Control
- 3.6-V to 40-V Operation
- Internal Undervoltage-Lockout Circuit
- Internal Short-Circuit Protection
- Oscillator Frequency . . . 20 kHz to 500 kHz
- Variable Dead Time Provides Control Over Total Range
- ±3% Tolerance on Reference Voltage (TL5001A)
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

description

The TL5001 and TL5001A incorporate on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5001/A contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout



(UVLO), short-circuit protection (SCP), and an open-collector output transistor. The TL5001A has a typical reference voltage tolerance of $\pm 3\%$ compared to $\pm 5\%$ for the TL5001.

The error-amplifier common-mode voltage ranges from 0 V to 1.5 V. The noninverting input of the error amplifier is connected to a 1-V reference. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low V_{CC} conditions, the UVLO circuit turns the output off until V_{CC} recovers to its normal operating range.

The TL5001C and TL5001AC are characterized for operation from -20° C to 85° C. The TL5001I and TL5001AI are characterized for operation from -40° C to 85° C. The TL5001Q and TL5001AQ are characterized for operation from -40° C to 125° C. The TL5001M and TL5001AM are characterized for operation from -55° C to 125° C.

AVAILABLE OPTIONS

		PACKAGED	DEVICES	
TA	SMALL OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)	CHIP CARRIER (FK)
-20°C to 85°C	TL5001CD	TL5001CP	_	_
-20 C 10 65 C	TL5001ACD	TL5001ACP	_	_
-40°C to 85°C	TL5001ID	TL5001IP		_
-40 C to 65 C	TL5001AID	TL5001AIP		_
-40°C to 125°C	TL5001QD		_	_
-40 C to 125 C	TL5001AQD			_
-55°C to 125°C	_	_	TL5001MJG	TL5001MFK
-55 C t0 125 C	_	_	TL5001AMJG	TL5001AMFK

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL5001CDR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



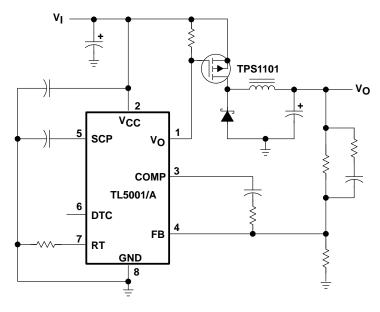
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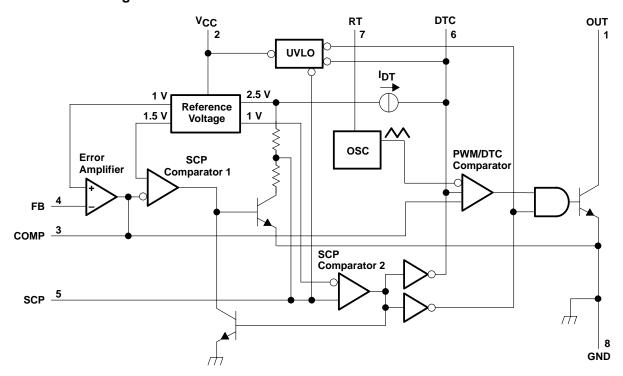
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schematic for typical application



functional block diagram





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detailed description

voltage reference

A 2.5-V regulator operating from V_{CC} is used to power the internal circuitry of the TL5001 and TL5001A and as a reference for the error amplifier and SCP circuits. A resistive divider provides a 1-V reference for the error amplifier noninverting input which typically is within 2% of nominal over the operating temperature range.

error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1-V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$$V_0 = (1 + R1/R2) (1 V)$$

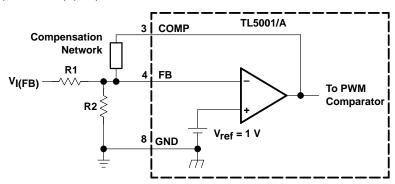


Figure 1. Error-Amplifier Gain Setting

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45 μ A, the total dc load resistance should be 100 k Ω or more.

oscillator/PWM

The oscillator frequency (f_{OSC}) can be set between 20 kHz and 500 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 k Ω to 250 k Ω . The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100 %, which is critical for boost and flyback converters. A current source generates a reference current (I_{DT}) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage (V_{DT}), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when V_{DT} is 0.7 V or less and 100% when V_{DT} is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing R_{DT} for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 (V_{OSC} max and V_{OSC} min are the maximum and minimum oscillator levels):





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dead-time control (DTC) (continued)

$$R_{DT} = (R_t + 1250) \left[D(V_{osc}max - V_{osc}min) + V_{osc}min \right]$$

Where

R_{DT} and R_t are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor (C_{DT}) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT}R_{DT} \left(1 - e^{\left(-t/R_{DT}C_{DT}\right)}\right)$$

$$c_{DT} = R_{DT} C_{DT} C_{DT}$$

$$c_{DT} = R_{DT} C_{DT} C_{DT}$$

Figure 2. Soft-Start Circuit

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant, $R_{DT}C_{DT}$, should be $t_0/3$ to $t_0/5$. The TL5001/A remains off until $V_{DT} \approx 0.7$ V, the minimum ramp value. C_{DT} is discharged every time UVLO or SCP becomes active.

undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V at 25°C) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

short-circuit protection (SCP)

The TL5001/A includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5 V. If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns off the TL5001/A output transistor.



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short-circuit protection (SCP) (continued)

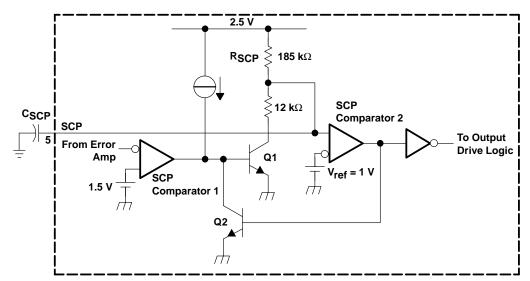


Figure 3. SCP Circuit

The timer operates by charging an external capacitor (C_{SCP}), connected between the SCP terminal and ground, towards 2.5 V through a 185-k Ω resistor (R_{SCP}). The circuit begins charging from an initial voltage of approximately 185 mV and times out when the capacitor voltage reaches 1 V. The output of SCP comparator 2 then goes high, turns on Q2, and latches the timer circuit. The expression for setting the SCP time period is derived from the following equation:

$$V_{SCP} = (2.5 - 0.185)(1 - e^{-t/\tau}) + 0.185$$

Where

$$\tau = R_{SCP}C_{SCP}$$

The end of the time-out period, t_{SCP} occurs when V_{SCP} = 1 V. Solving for C_{SCP} yields:

$$C_{SCP} = 12.46 \times t_{SCP}$$

Where

t is in seconds, C in µF.

t_{SCP} must be much longer (generally 10 to 15 times) than the converter start-up period or the converter will not start.

output transistor

The output of the TL5001/A is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)		41 V
Amplifier input voltage, V _{I(FB)}		
Output voltage, V _O , OUT		51 V
Output current, I _O , OUT		
Output peak current, I _{O(peak)} , OUT		
Continuous total power dissipation		. See Dissipation Rating Table
Operating ambient temperature range, T _A :		
	TL5001I, TL5001AI	40°C to 85°C
	TL5001Q, TL5001AQ	40°C to 125°C
	TL5001M, TL5001AM	–55°C to 125°C
Storage temperature range, T _{stq}		65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from	case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V _{CC}		3.6	40	V
Amplifier input voltage, V _{I(FB)}		0	1.5	V
Output voltage, VO, OUT			50	V
Output current, IO, OUT			20	mA
COMP source current			45	μΑ
COMP dc load resistance		100		kΩ
Oscillator timing resistor, R _t		15	250	kΩ
Oscillator frequency, fosc		20	500	kHz
	TL5001C, TL5001AC	-20	85	
Operating ambient temperature T	TL5001I, TL5001AI	-40	85	°C
Operating ambient temperature, T _A	TL5001Q, TL5001AQ	-40	125	1
	TL5001M, TL5001AM	-55	125	1



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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{OSC} = 100 kHz (unless otherwise noted)

reference

PARAMETER	TEST CONDITIONS	TL50	01C, TL5	001I	TL500	001AI	UNIT	
PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
Output voltage	COMP connected to FB	0.95	1	1.05	0.97	1	1.03	V
Input regulation	V _{CC} = 3.6 V to 40 V		2	12.5		2	12.5	mV
	$T_A = -20^{\circ}C$ to 25°C (C suffix)	-10	-1	10	-10	-1	10	
Output voltage change with temperature	$T_A = -40^{\circ}\text{C to } 25^{\circ}\text{C (I suffix)}$	-10	-1	10	-10	-1	10	mV/V
	T _A = 25°C to 85°C	-10	-2	10	-10	-2	10	

[†] All typical values are at $T_A = 25$ °C.

undervoltage lockout

PARAMETER	TEST CONDITIONS	TL50	01C, TL5	001I	TL5001	UNIT		
PARAMETER		MIN	TYP†	MAX	MIN	TYP [†]	MAX	ONII
Upper threshold voltage	T _A = 25°C		3			3		V
Lower threshold voltage	T _A = 25°C		2.8			2.8		V
Hysteresis	T _A = 25°C	100	200		100	200		mV
Reset threshold voltage	T _A = 25°C	2.1	2.55		2.1	2.55		V

[†] All typical values are at T_A = 25°C.

short-circuit protection

PARAMETER	TEST CONDITIONS	TL50	01C, TL5	001I	TL500	001AI	UNIT	
PARAMETER		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
SCP threshold voltage	T _A = 25°C	0.95	1.00	1.05	0.97	1.00	1.03	V
SCP voltage, latched	No pullup	140	185	230	140	185	230	mV
SCP voltage, UVLO standby	No pullup		60	120		60	120	mV
Input source current	T _A = 25°C	-10	-15	-20	-10	-15	-20	μΑ
SCP comparator 1 threshold voltage			1.5			1.5		V

[†] All typical values are at $T_A = 25$ °C.

oscillator

PARAMETER	TEST CONDITIONS	TL50	01C, TL5	5001I	TL500	IAC, TL5	001AI	UNIT
PARAMETER	TEGT GONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
Frequency	$R_t = 100 \text{ k}\Omega$		100			100		kHz
Standard deviation of frequency			15			15		kHz
Frequency change with voltage	V _{CC} = 3.6 V to 40 V		1			1		kHz
	$T_A = -40^{\circ}C \text{ to } 25^{\circ}C$	-4	-0.4	4	-4	-0.4	4	kHz
Frequency change with temperature	$T_A = -20^{\circ}C$ to $25^{\circ}C$	-4	-0.4	4	-4	-0.4	4	kHz
	$T_A = 25^{\circ}C \text{ to } 85^{\circ}C$	-4	-0.2	4	-4	-0.2	4	kHz
Voltage at RT			1			1		V

 $[\]uparrow$ All typical values are at T_A = 25°C.





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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

dead-time control

PARAMETER		TEST CONDITIONS	TL5001C, TL5001I			TL5001	UNIT		
		TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	ONII
Output (acurea) current	TL5001C	V _(DT) = 1.5 V	0.9 × I _{RT} ‡		$1.1 \times I_{RT}$	0.9 × I _{RT} ‡		1.1 × I _{RT}	
Output (source) current	TL5001I	V _(DT) = 1.5 V	0.9 × I _{RT} ‡		1.2 × I _{RT}	0.9 × I _{RT} ‡		1.2 × I _{RT}	μΑ
Input threshold voltage		Duty cycle = 0%	0.5	0.7		0.5	0.7		V
Input threshold voltage		Duty cycle = 100%		1.3	1.5		1.3	1.5	V

[†] All typical values are at $T_A = 25$ °C.

error amplifier

PARAMETER		TEST CONDITIONS	TL50	01C, TL5	5001I	TL5001	AC, TL	5001AI	UNIT
I ANAMETEN		TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
Input voltage		V _{CC} = 3.6 V to 40 V	0		1.5	0		1.5	V
Input bias current				-160	-500		-160	-500	nA
	Positive		1.5	2.3		1.5	2.3		V
Output voltage swing	Negative			0.3	0.4		0.3	0.4	V
Open-loop voltage amplification				80			80		dB
Unity-gain bandwidth				1.5			1.5		MHz
Output (sink) current		V _{I(FB)} = 1.2 V, COMP = 1 V	100	600		100	600		μΑ
Output (source) current		V _{I(FB)} = 0.8 V, COMP = 1 V	-45	-70		-45	-70		μΑ

[†] All typical values are at $T_A = 25$ °C.

output

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I	TL5001AC, TL5001AI	LIAUT
	TEST CONDITIONS	MIN TYP [†] MAX	MIN TYP [†] MAX	UNIT
Output saturation voltage	I _O = 10 mA	1.5 2	1.5 2	V
Off-state current	$V_{O} = 50 \text{ V}, \qquad V_{CC} = 0$	10	10	^
	V _O = 50 V	10	10	μΑ
Short-circuit output current	V _O = 6 V	40	40	mA

[†] All typical values are at $T_A = 25$ °C.

total device

PARAMETER		TEST CONDITIONS	TL50	01C, TL5	001I	TL5001AC, TL5001AI			UNIT
PARAMETER		TEST CONDITIONS		TYP†	MAX	MIN	TYP [†]	MAX	UNIT
Standby supply current	Off state			1	1.5		1	1.5	mA
Average supply current		$R_t = 100 \text{ k}\Omega$		1.4	2.1		1.4	2.1	mA

[†] All typical values are at T_A = 25°C.



[‡] Output source current at RT



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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{OSC} = 100 kHz (unless otherwise noted)

reference

PARAMETER	TEST	CONDITIONS		L5001Q, L5001M			L5001AQ L5001AN	′	UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
Output voltage	T _A = 25°C	COMP connected to FB	0.95	1.00	1.05	0.97	1.00	1.03	V
Output voltage	T _A = MIN to MAX	0.93	0.98	1.07	0.94	0.98	1.06	V	
Input regulation	T _A = MIN to MAX	V _{CC} = 3.6 V to 40 V		2	12.5		2	12.5	mV
Output voltage change with temperature	T _A = MIN to MAX	*-6	2	*6	*-6	2	*6	%	

[†] All typical values are at T_A = 25°C.

undervoltage lockout

PARAMETER	TEST CONDITIONS	TL5001Q, TL5001M	TL5001AQ, TL5001AM	UNIT
		MIN TYPT MAX	MIN TYP [†] MAX	
Lippor throubold voltage	T _A = MIN, 25°C	3.00	3.00	V
Upper threshold voltage	$T_A = MAX$	2.55	2.55	V
Lower threshold voltage	T _A = MIN, 25°C	2.8	2.8	V
Lower threshold voltage	$T_A = MAX$	2.0	2.0	V
Hysteresis	T _A = MIN to MAX	100 200	100 200	mV
Depart throughold valte as	T _A = MIN, 25°C	2.10 2.55	2.10 2.55	V
Reset threshold voltage	$T_A = MAX$	0.35 0.63	0.35 0.63	٧

 $[\]uparrow$ All typical values are at $T_A = 25^{\circ}$ C.

short-circuit protection

PARAMETER	TEST CO	NDITIONS		L5001Q [L5001M	′	T T	UNIT		
			MIN	TYP†	MAX	MIN	TYP†	MAX	
SCP threshold voltage	T _A = MIN, 25°C		0.95	1.00	1.05	0.97	1.00	1.03	V
SCF tilleshold voltage	$T_A = MAX$		0.93	0.98	1.07	0.94	0.98	1.06	V
SCP voltage, latched	$T_A = MIN \text{ to } MAX$	No pullup	140	185	230	140	185	230	mV
SCP voltage, UVLO standby	$T_A = MIN \text{ to } MAX$	No pullup		60	120		60	120	mV
Equivalent timing resistance	$T_A = MIN \text{ to } MAX$			185			185		kΩ
SCP comparator 1 threshold voltage	T _A = MIN to MAX	•		1.5			1.5		V

[†] All typical values are at $T_A = 25$ °C.



^{*}Not production tested.



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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

oscillator

PARAMETER	TEST C	ONDITIONS		L5001Q [L5001M	'	TI T	UNIT		
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Frequency	$T_A = MIN \text{ to } MAX$	$R_t = 100 \text{ k}\Omega$		100			100		kHz
Standard deviation of frequency	$T_A = MIN \text{ to } MAX$			2			2		kHz
Frequency change with voltage	$T_A = MIN \text{ to } MAX$	$V_{CC} = 3.6 \text{ V to } 40 \text{ V}$		1			1		kHz
Frequency change with	T. MINI to MAY	Q suffix	*-6	3	*6	*-6	3	*6	1411-
temperature	$T_A = MIN \text{ to MAX}$	M suffix	*-9	5	*9	*-9	5	*9	kHz
Voltage at RT	$T_A = MIN \text{ to } MAX$			1			1		V

[†] All typical values are at T_A = 25°C.

dead-time control

PARAMETER	TEST C	ONDITIONS	TL500	1Q, TL5	001M	TL5001	UNIT		
PARAMETER	lesi co	SNOTTIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
Output (source) current	T _A = MIN to MAX	V _(DT) = 1.5 V	0.9 × I _{RT} ‡		1.1 × I _{RT}	0.9 × I _{RT} ‡		1.1 × I _{RT}	μΑ
	T 25°C	Duty cycle = 0%	0.5	0.7		0.5	0.7		
Input threshold	T _A = 25°C	Duty cycle = 100%		1.3	1.5		1.3	1.5	V
voltage	T MINI to MAY	Duty cycle = 0%	0.4	0.7		0.4	0.7		V
	$T_A = MIN \text{ to MAX}$	Duty cycle = 100%		1.3	1.7		1.3	1.7	

[†] All typical values are at $T_A = 25$ °C.

error amplifier

PARAMETE	:R	TES	T CONDITIONS			L5001Q L5001M		TI T	UNIT		
					MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
Input bias current		T _A = MIN to MAX				-160	-500		-160	-500	nA
Output voltage	Positive	T _A = MIN to MAX			1.5	2.3		1.5	2.3		V
swing	Negative	IA = MIIN TO MAX				0.3	0.4		0.3	0.4	V
Open-loop voltage amplification		T _A = MIN to MAX				80			80		dB
Unity-gain bandwidth		T _A = MIN to MAX				1.5			1.5		MHz
Output (sink) current		T _A = MIN to MAX	$V_{I(FB)} = 1.2 V,$	COMP = 1 V	100	600		100	600		μΑ
Output (agurag) gurra	Output (source) current		V	COMP - 4 V	-45	-70		-45	-70		
Output (Source) curre	#IIL	$T_A = MAX$	$V_{I(FB)} = 0.8 V,$	COIVIF = 1 V	-30	-45		-30	-45		μΑ

[†] All typical values are at $T_A = 25$ °C.



^{*}Not production tested.

[‡] Output source current at RT



Datasheet of TL5001CDR - IC REG CTRLR PWM 8SOIC

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TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS084F - APRIL 1994 - REVISED JANUARY 2002

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

output

PARAMETER	TEST	CONDITIONS	1	TL5001Q TL5001M	'	TI T	UNIT		
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
Output saturation voltage	$T_A = MIN \text{ to } MAX$	I _O = 10 mA		1.5	2		1.5	2	V
Off-state current	T _A = MIN to MAX	$V_{O} = 50 \text{ V}, V_{CC} = 0$			10			10	
Oil-state current	IA = MIN TO MAX	V _O = 50 V			10			10	μΑ
Short-circuit output current	T _A = MIN to MAX	V _O = 6 V		40			40		mA

[†] All typical values are at $T_A = 25$ °C.

total device

PARAMETER		TEST CONI	TEST CONDITIONS				TI T	UNIT		
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
Standby supply current	Off state	$T_A = MIN \text{ to } MAX$			1	1.5		1	1.5	mA
Average supply current		T _A = MIN to MAX	$R_t = 100 \text{ k}\Omega$		1.4	2.1		1.4	2.1	mA

[†] All typical values are at $T_A = 25$ °C.

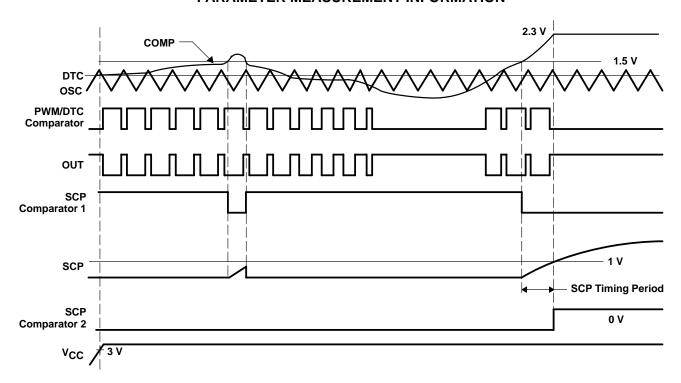


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PARAMETER MEASUREMENT INFORMATION



NOTE A: The waveforms show timing characteristics for an intermittent short circuit and a longer short circuit that is sufficient to activate SCP.

Figure 4. PWM Timing Diagram



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TYPICAL CHARACTERISTICS

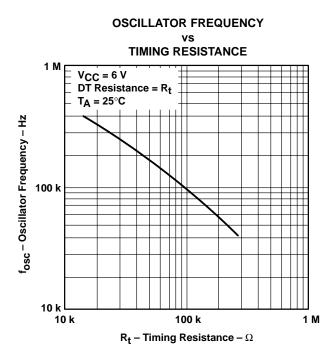


Figure 5

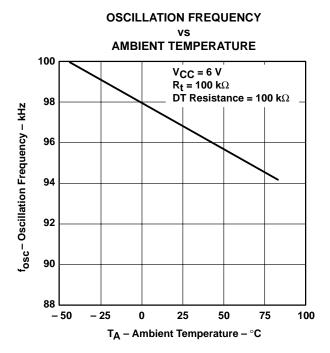


Figure 6

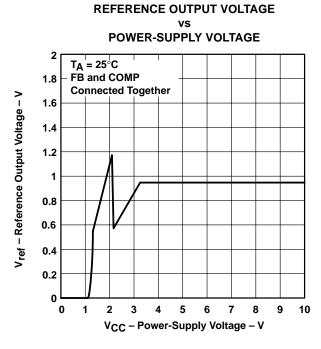


Figure 7

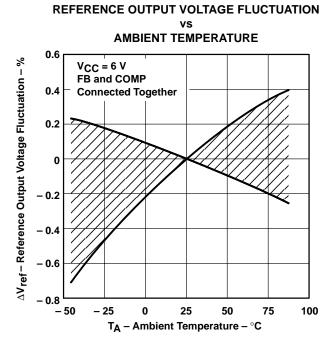


Figure 8



TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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TYPICAL CHARACTERISTICS

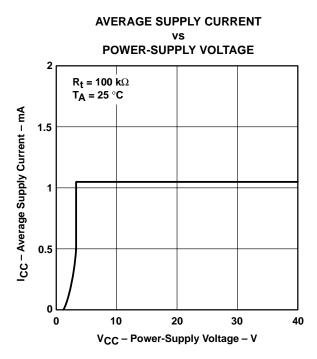


Figure 9

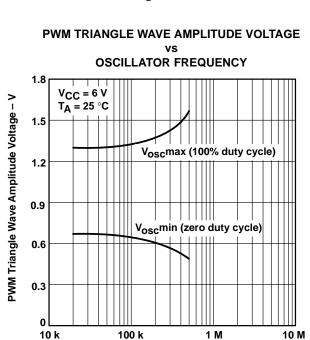


Figure 11

f_{OSC} – Oscillator Frequency – Hz

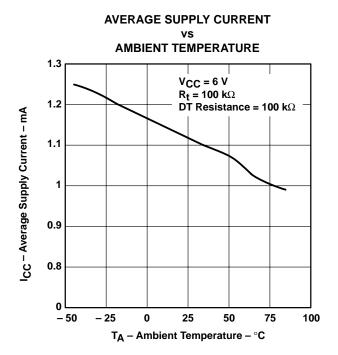


Figure 10

ERROR AMPLIFIER OUTPUT VOLTAGE ٧S **OUTPUT (SINK) CURRENT**

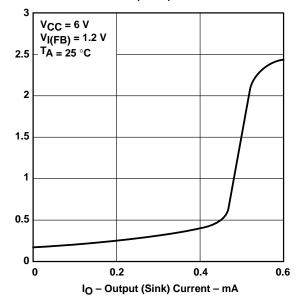


Figure 12



V_O - Error Amplifier Output Voltage - V

0

TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OUTPUT VOLTAGE OUTPUT (SOURCE) CURRENT VCC = 6 V $V_{I(FB)} = 0.8 V$ T_A = 25 °C V_O - Error Amplifier Output Voltage - V 2.5 2 1.5 1 0.5 0

Figure 13

60

 I_O – Output (Source) Current – μ A

80

100

120

40

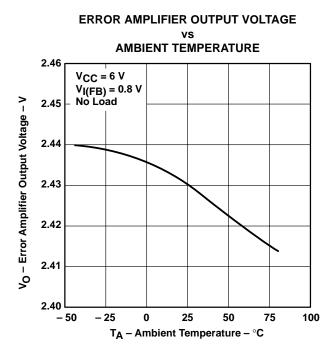


Figure 14

ERROR AMPLIFIER OUTPUT VOLTAGE AMBIENT TEMPERATURE 240 **VCC = 6 V** Vo - Error Amplifier Output Voltage - mV $V_{I(FB)} = 1.2 V$ Nò Lóad 220 200 180 160 140 120 - 50 - 25 100 T_A – Ambient Temperature – °C

Figure 15

ERROR AMPLIFIER OPEN-LOOP GAIN AND PHASE SHIFT

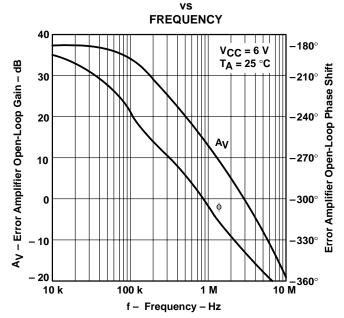


Figure 16



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TYPICAL CHARACTERISTICS

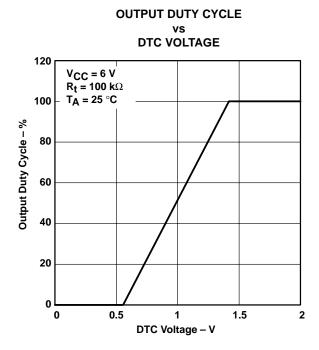


Figure 17

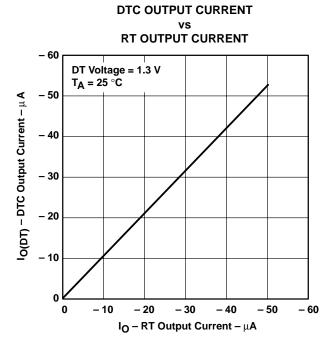


Figure 19

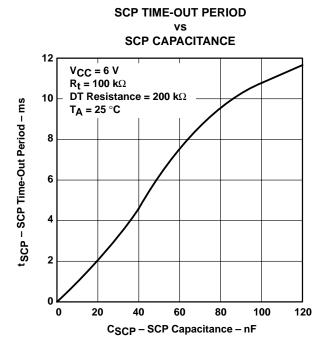


Figure 18

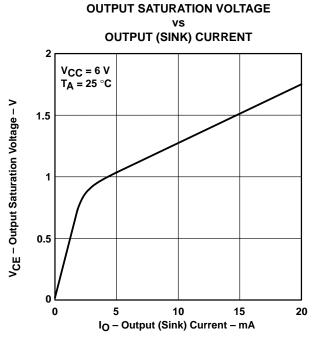


Figure 20



TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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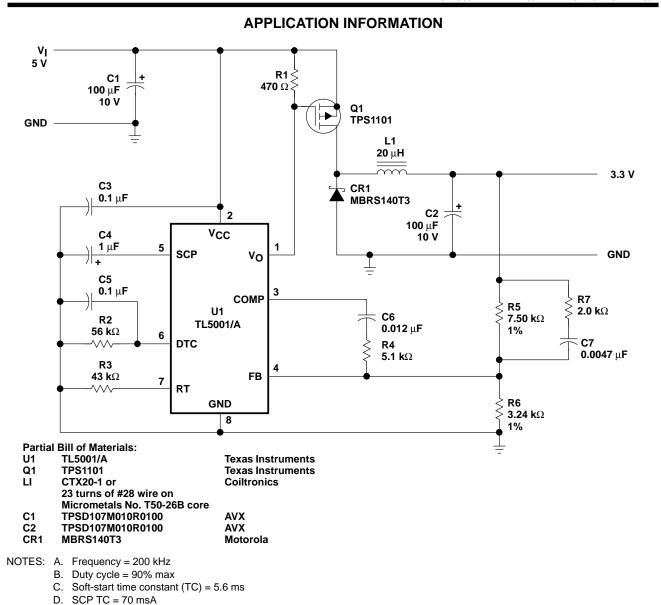


Figure 21. Step-Down Converter



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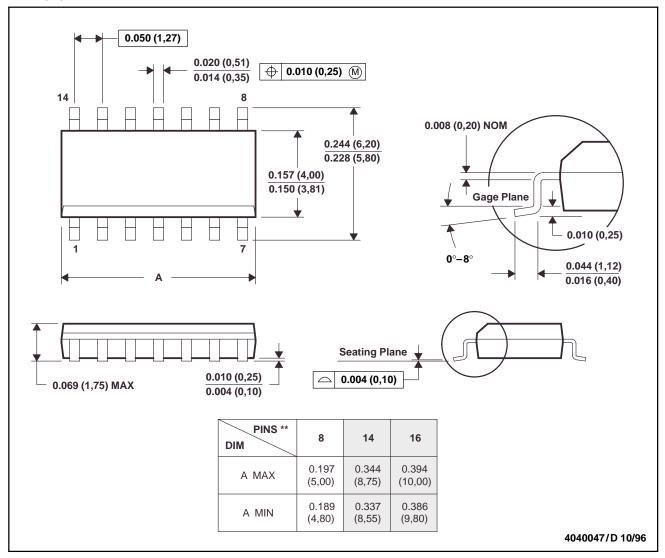
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MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



NOTES: B. All linear dimensions are in inches (millimeters).

- C. This drawing is subject to change without notice.
- D. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- E. Falls within JEDEC MS-012



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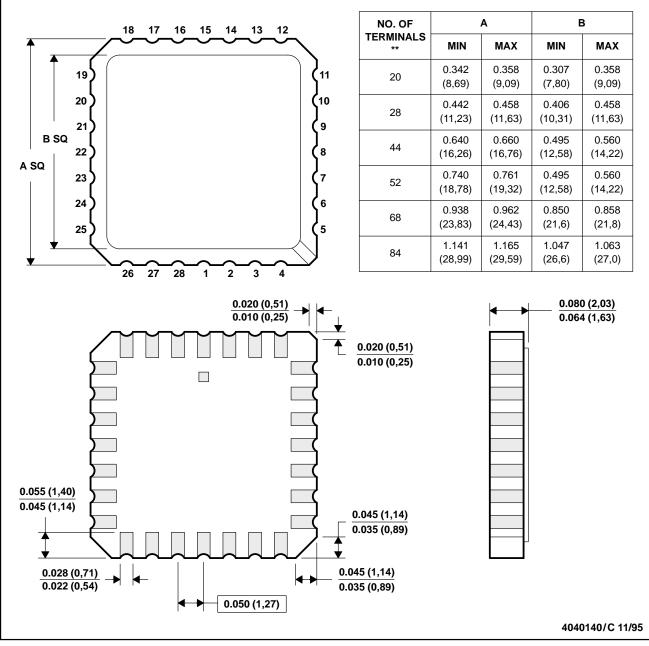
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MECHANICAL DATA

FK (S-CQCC-N**)

28 TERMINALS SHOWN

LEADLESS CERAMIC CHIP CARRIER



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold-plated.
 - E. Falls within JEDEC MS-004





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PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

Orderable Device	Status	Package Type		Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
5962-9958301QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9958301QPA TL5001M	Samples
5962-9958302Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9958302Q2A TL5001 AMFKB	Samples
5962-9958302QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9958302QPA TL5001AM	Samples
TL5001ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	Samples
TL5001ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	Samples
TL5001ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	Samples
TL5001ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	Samples
TL5001AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	Samples
TL5001AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	Samples
TL5001AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	Samples
TL5001AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	Samples
TL5001AIP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5001AIP	Samples
TL5001AIPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5001AIP	Samples
TL5001AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9958302Q2A TL5001 AMFKB	Samples
TL5001AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9958302QPA TL5001AM	Samples



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samp
TL5001AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001AQ	Samp
TL5001AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		5001AQ	Samp
TL5001AQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001AQ	Samp
TL5001AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		5001AQ	Samp
TL5001CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	Sam
TL5001CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	Sam
TL5001CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	Sam
TL5001CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	Sam
TL5001CP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	TL5001CP	Sam
TL5001CPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	TL5001CP	Sam
TL5001CPS	ACTIVE	SO	PS	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		T5001	Sam
TL5001CPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI			
TL5001CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	T5001	Sam
TL5001CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	T5001	Sam
TL5001ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	50011	Sam
TL5001IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	50011	Sam
TL5001IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	50011	Sam
TL5001IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	50011	Sam



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Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TL5001IP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5001IP	Samples
TL5001IPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5001IP	Samples
TL5001IPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Z5001	Samples
TL5001MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL5001MJG	Samples
TL5001MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9958301QPA TL5001M	Samples
TL5001QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001Q	Samples
TL5001QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		5001Q	Samples
TL5001QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001Q	Samples
TL5001QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		5001Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design. PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): Tl's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above

Green (ROHS & no Sb/Br): TI defines "Green" to mean Pb-Free (ROHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TL5001, TL5001A, TL5001AM, TL5001M:

- Automotive: TL5001A-Q1, TL5001A-Q1
- Military: TL5001M, TL5001AM

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

Datasheet of TL5001CDR - IC REG CTRLR PWM 8SOIC

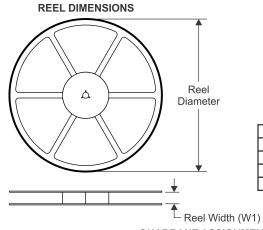
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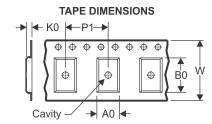


PACKAGE MATERIALS INFORMATION

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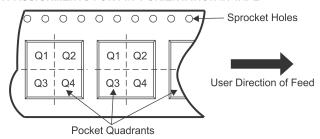
TAPE AND REEL INFORMATION





- A0 Dimension designed to accommodate the component width
- B0 Dimension designed to accommodate the component length
- K0 Dimension designed to accommodate the component thickness
- W Overall width of the carrier tape
- P1 Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL5001ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001AQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001AQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL5001IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001IPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL5001QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

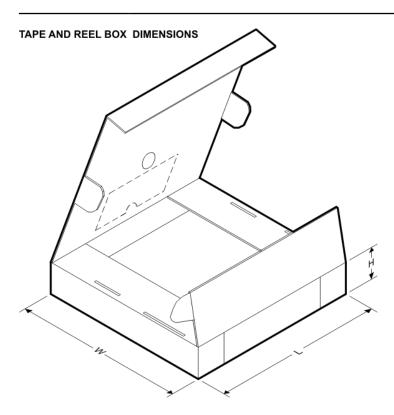
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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL5001ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001AQDR	SOIC	D	8	2500	367.0	367.0	38.0
TL5001AQDRG4	SOIC	D	8	2500	367.0	367.0	38.0
TL5001CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL5001IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001IPSR	SO	PS	8	2000	367.0	367.0	38.0
TL5001QDR	SOIC	D	8	2500	367.0	367.0	38.0
TL5001QDRG4	SOIC	D	8	2500	367.0	367.0	38.0



Datasheet of TL5001CDR - IC REG CTRLR PWM 8SOIC

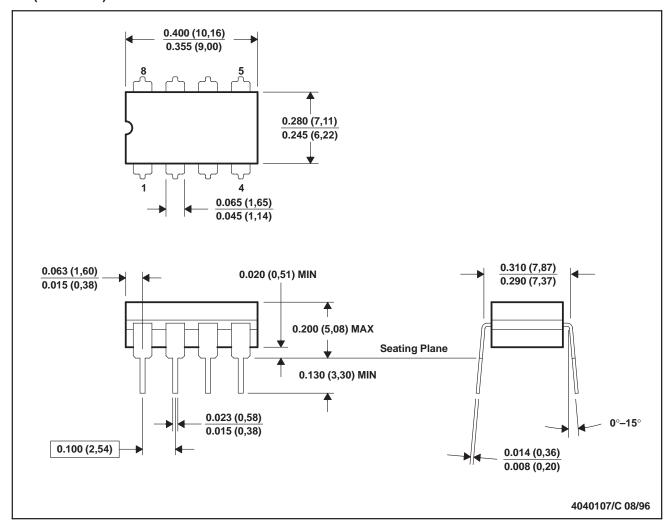
Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

MECHANICAL DATA

MCER001A - JANUARY 1995 - REVISED JANUARY 1997

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8





Datasheet of TL5001CDR - IC REG CTRLR PWM 8SOIC

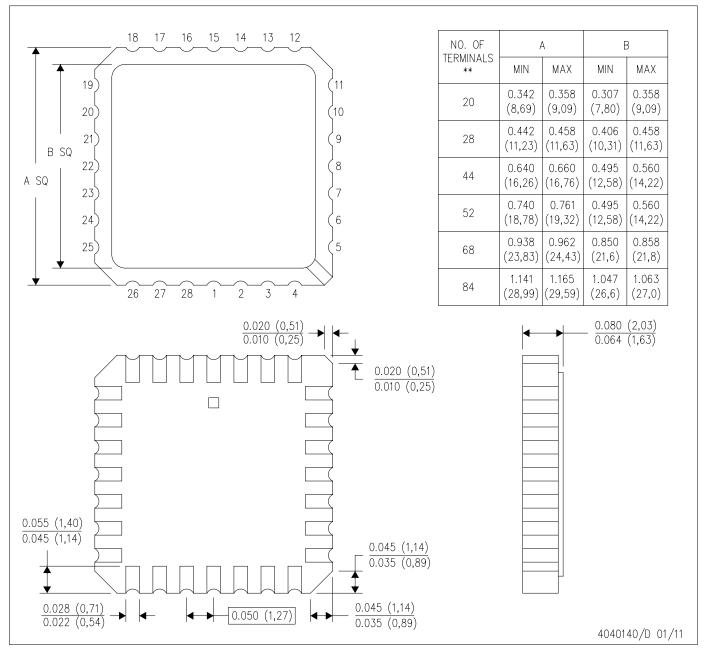
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MECHANICAL DATA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

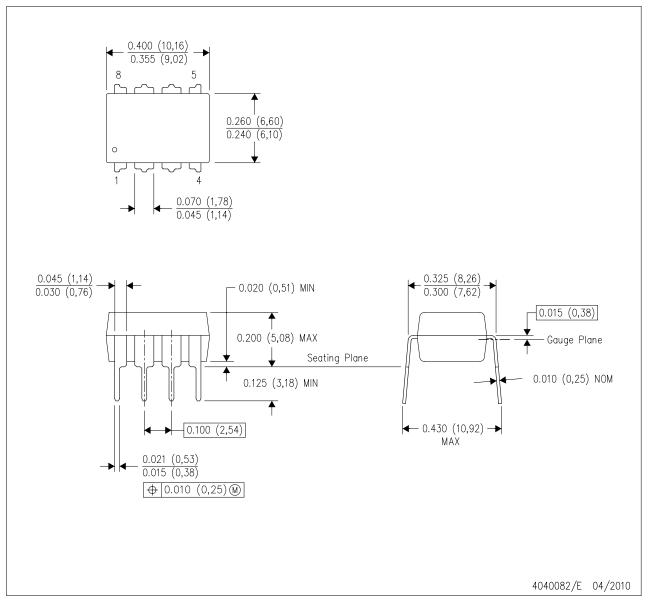




MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.

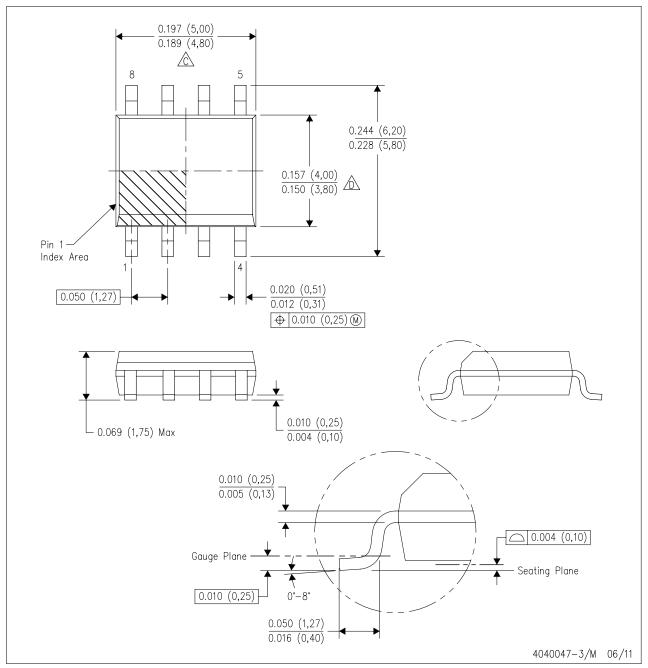




MECHANICAL DATA

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



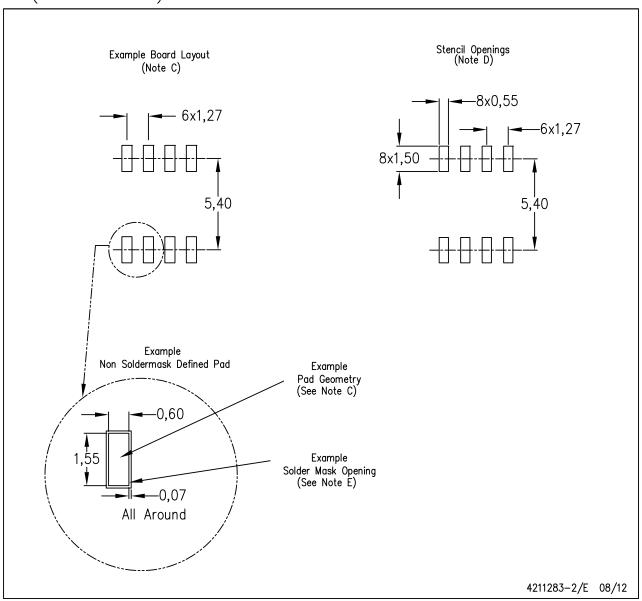




LAND PATTERN DATA

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

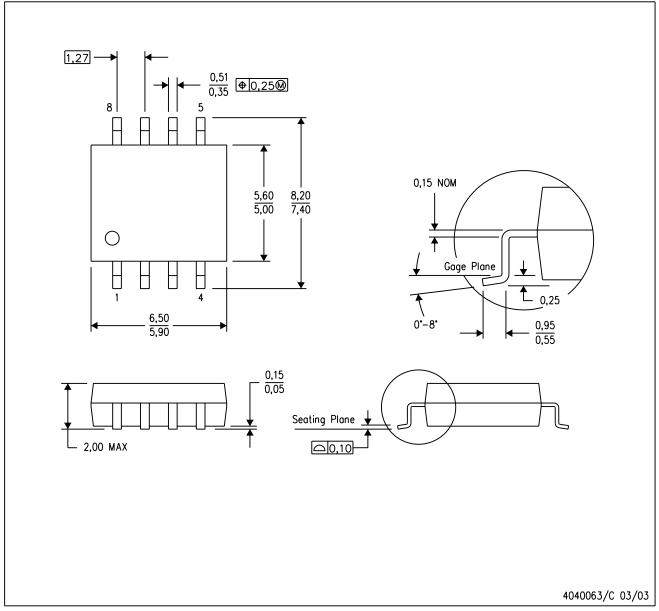




MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.





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