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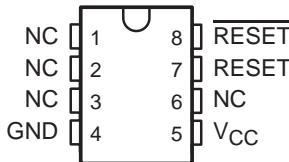
[TL7759CPWR](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Precision Input Threshold Voltage . . . 4.55 V  $\pm$ 120 mV
- Low Standby Current . . . 20  $\mu$ A
- Reset Outputs Defined When  $V_{CC}$  Exceeds 1 V
- True and Complementary Reset Outputs
- Wide Supply-Voltage Range . . . 1 V to 7 V

**D, P, OR PW PACKAGE  
(TOP VIEW)**



NC – No internal connection

### description

The TL7759 is a supply-voltage supervisor designed for use as a reset controller in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power up, when the supply voltage,  $V_{CC}$ , attains a value approaching 1 V, the RESET and  $\overline{\text{RESET}}$  outputs become active (high and low, respectively) to prevent undefined operation. If the supply voltage drops below the input threshold voltage level ( $V_{IT-}$ ), the reset outputs go to the reset active state until the supply voltage has returned to its nominal value (see timing diagram).

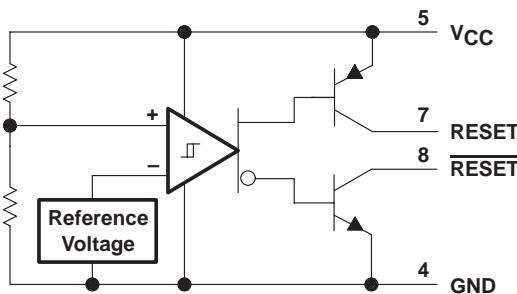
The TL7759C is characterized for operation from 0°C to 70°C.

## AVAILABLE OPTIONS

TA	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	SHRINK SMALL OUTLINE (PW)	
0°C to 70°C	TL7759CD	TL7759CP	TL7759CPW	TL7759Y

The D and PW packages are available taped and reeled. Add the suffix R to the device type (e.g., TL7759CDR). Chip forms are tested at 25°C.

## functional block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PRODUCTION DATA** information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**TL7759**

## SUPPLY-VOLTAGE SUPERVISORS

SLVS042D – JANUARY 1991 – REVISED JULY 1999

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$ (see Note 1)	20 V
Off-state output voltage range: $\overline{RESET}$ voltage	–0.3 V to 20 V
RESET voltage	–0.3 V to 20 V
Low-level output current, $I_{OL}$ ( $\overline{RESET}$ )	30 mA
High-level output current, $I_{OH}$ ( $RESET$ )	–10 mA
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): D package	97°C/W
P package	127°C/W
PW package	149°C/W
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.

2. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$		1	7	V
Output voltage, $V_O$ (see Note 4)	Transistor off $\overline{RESET}$ voltage	15	V	
	Transistor off RESET voltage	0		
Low-level output current, $I_{OL}$	RESET	24	mA	
High-level output current, $I_{OH}$	RESET	–8	mA	
Operating free-air temperature, $T_A$	TL7759C	0	70	°C

NOTE 4: RESET output must not be pulled down below GND potential.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL7759C			UNIT
		MIN	TYP <sup>‡</sup>	MAX	
$V_{OL}$ Low-level output voltage	$V_{CC} = 4.3$ V	$I_{OL} = 24$ mA	0.4	0.8	V
$V_{OH}$ High-level output voltage		$I_{OH} = -8$ mA	$V_{CC}-1$		V
$V_{IT-}$ Input threshold voltage (negative-going $V_{CC}$ )	$T_A = 25^\circ\text{C}$		4.43	4.55	V
	$T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$		4.4	4.7	
$V_{res}^§$ Power-up reset voltage	$R_L = 2.2$ k $\Omega$	$T_A = 25^\circ\text{C}$	0.8	1	V
		$T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$		1.2	
$V_{hys}^¶$ Hysteresis at $V_{CC}$ input	$T_A = 25^\circ\text{C}$		40	50	mV
	$T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$		30	70	
$I_{OH}$ High-level output current	$V_{CC} = 7$ V, See Figure 1	$V_{OH} = 15$ V		1	$\mu\text{A}$
$I_{OL}$ Low-level output current		$V_{OL} = 0$ V		–1	$\mu\text{A}$
$I_{CC}$ Supply current	No load	$V_{CC} = 4.3$ V	1400	2000	$\mu\text{A}$
		$V_{CC} = 5.5$ V		40	

<sup>†</sup> Typical values are at  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> This is the lowest voltage at which  $\overline{RESET}$  becomes active,  $V_{CC}$  slew rate  $\leq 5$  V/ $\mu\text{s}$ .

<sup>¶</sup> This is the difference between positive-going input threshold voltage,  $V_{IT+}$ , and negative-going input threshold voltage,  $V_{IT-}$ .



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**TL7759**  
**SUPPLY-VOLTAGE SUPERVISORS**

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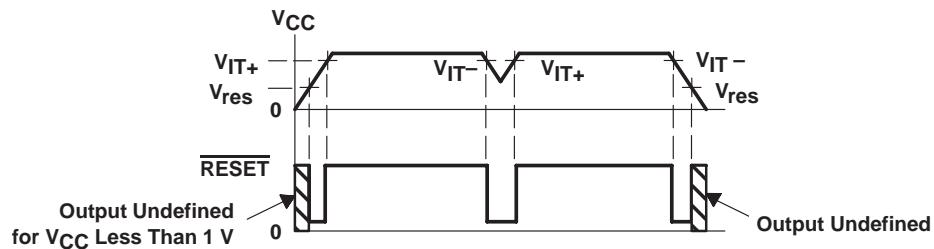
**electrical characteristics,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TL7759Y			UNIT
		MIN	TYP	MAX	
$V_{OL}$	Low-level output voltage RESET	$V_{CC} = 4.3 \text{ V}$ , $I_{OL} = 24 \text{ mA}$		0.4	V
$V_{IT-}$	Input threshold voltage (negative-going $V_{CC}$ )			4.55	V
$V_{res}^\dagger$	Power-up reset voltage	$R_L = 2.2 \text{ k}\Omega$		0.8	V
$V_{hys}^\ddagger$	Hysteresis at $V_{CC}$ input			50	mV
$I_{CC}$	Supply current	$V_{CC} = 4.3 \text{ V}$ , No load		1400	$\mu\text{A}$

<sup>†</sup> This is the lowest voltage at which RESET becomes active,  $V_{CC}$  slew rate  $\leq 5 \text{ V}/\mu\text{s}$ .

<sup>‡</sup> This is the difference between positive-going input threshold voltage,  $V_{IT+}$ , and negative-going input threshold voltage,  $V_{IT-}$ .

**timing diagram**



**switching characteristics at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7759C		UNIT
				MIN	MAX	
$t_{PLH}$	Propagation delay time, low-to high-level output	$V_{CC}$	RESET	See Figures 2 and 3 <sup>§</sup>	5	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high-to low-level output	$V_{CC}$	<u>RESET</u>	See Figures 2 and 4	5	$\mu\text{s}$
$t_r$	Rise time		<u>RESET</u>	See Figures 2 and 4 <sup>§</sup>	1	$\mu\text{s}$
$t_f$	Fall time		<u>RESET</u>	See Figures 2 and 4	1	$\mu\text{s}$
$t_w(\text{min})$	Minimum pulse duration	$V_{CC}$	<u>RESET</u>	See Figures 2 and 4	5	$\mu\text{s}$

<sup>§</sup>  $V_{CC}$  slew rate  $\leq 5 \text{ V}/\mu\text{s}$

**TL7759**

## SUPPLY-VOLTAGE SUPERVISORS

SLVS042D – JANUARY 1991 – REVISED JULY 1999

### PARAMETER MEASUREMENT INFORMATION

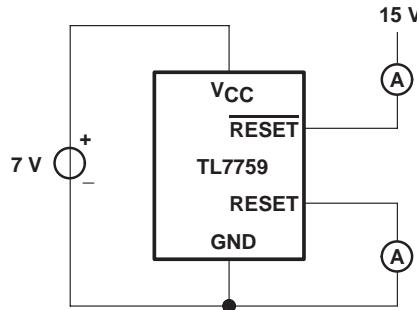
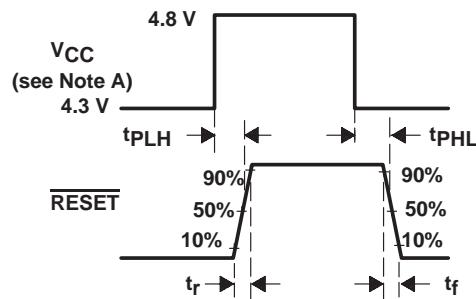
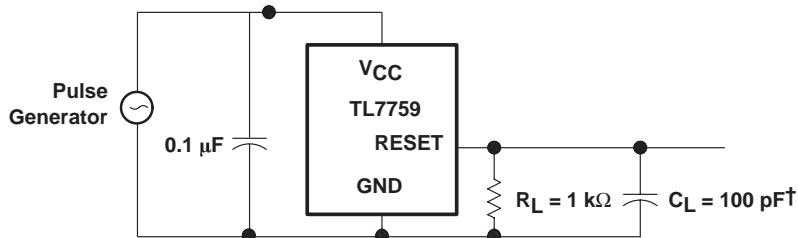


Figure 1. Test Circuit for Output Leakage Current



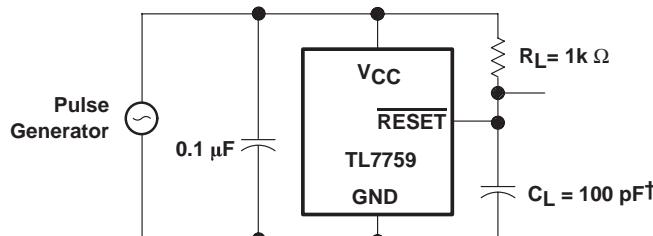
NOTE A:  $V_{CC}$  slew rate  $\leq 5 \text{ V}/\mu\text{s}$ .

Figure 2. Switching Diagram



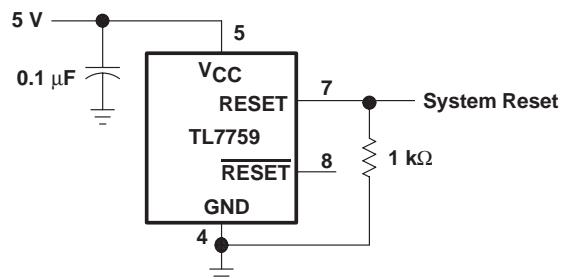
†  $C_L$  Includes jig and probe capacitance.

Figure 3. Test Circuit for RESET Output Switching Characteristics



†  $C_L$  Includes jig and probe capacitance.

Figure 4. Test Circuit for RESET Output Switching Characteristics

**APPLICATION INFORMATION****Figure 5. Power-Supply System Reset Generation**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7759CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7759C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TL7759CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7759C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TL7759CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7759CP	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TL7759CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T7759	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TL7759CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TL7759CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7759C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TL7759CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7759C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

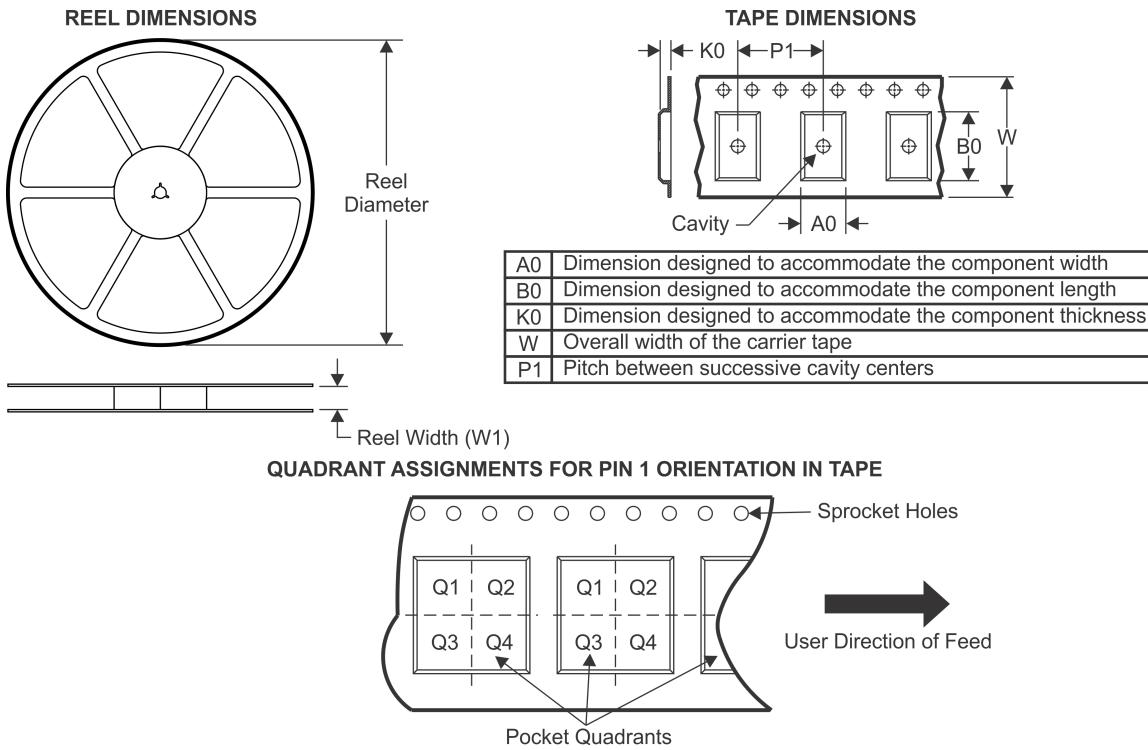
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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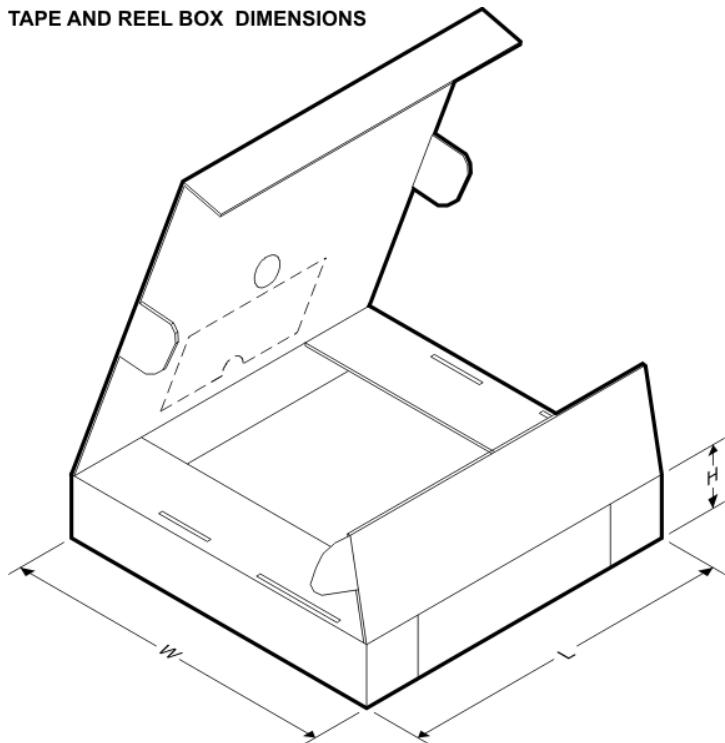
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7759CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7759CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL7759CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



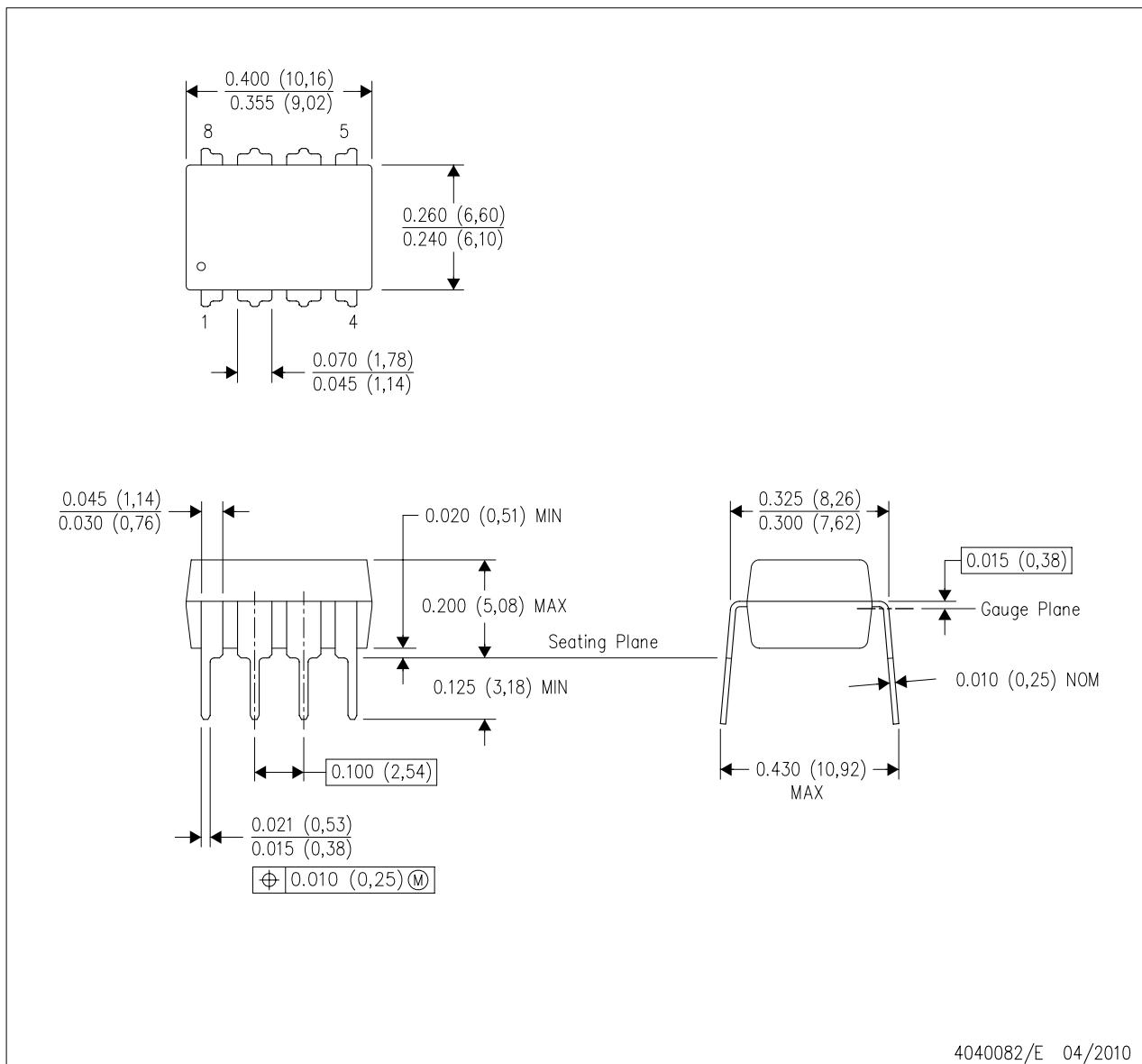
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7759CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7759CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL7759CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

## MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.

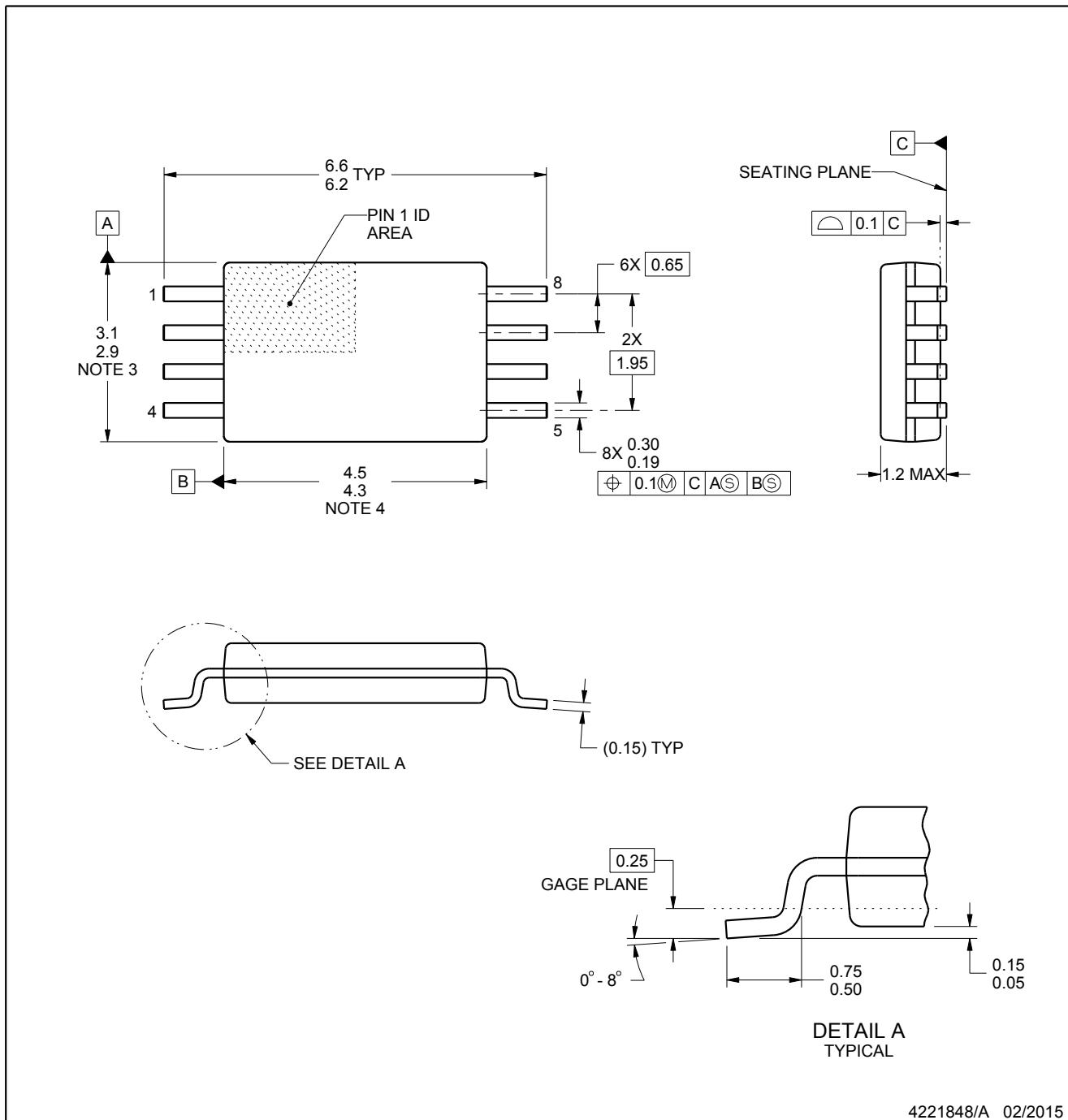


## PACKAGE OUTLINE

**PW0008A**

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4221848/A 02/2015

**NOTES:**

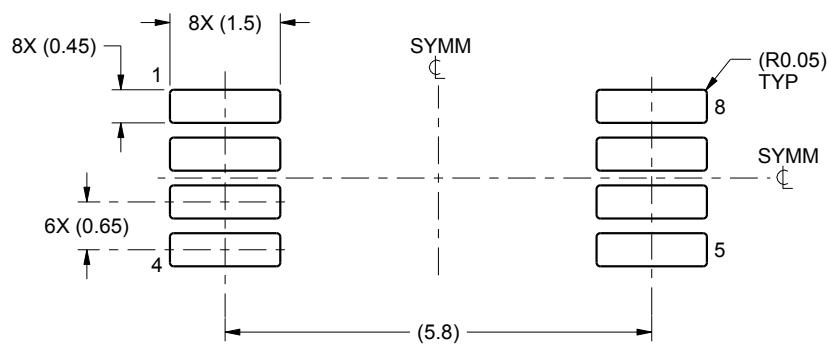
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

## EXAMPLE BOARD LAYOUT

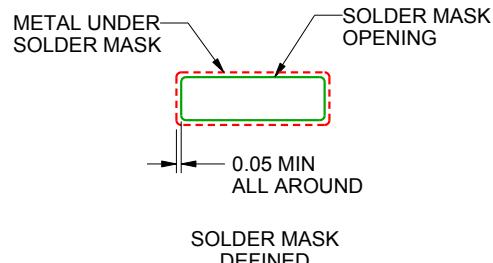
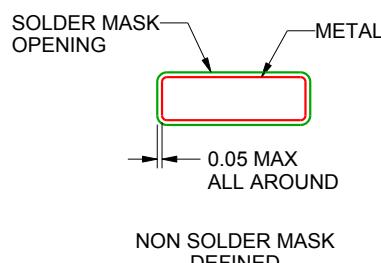
**PW0008A**

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

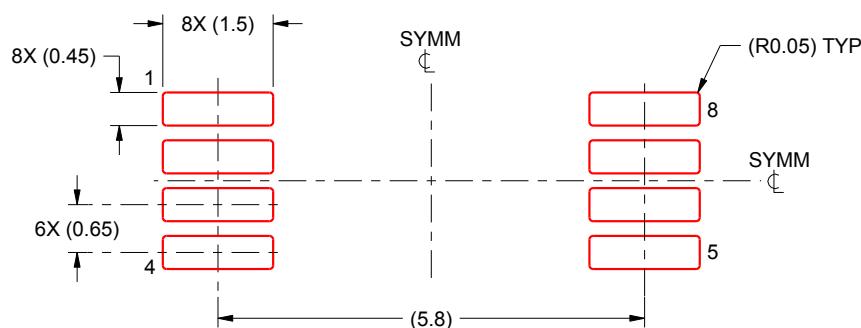
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**PW0008A**

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

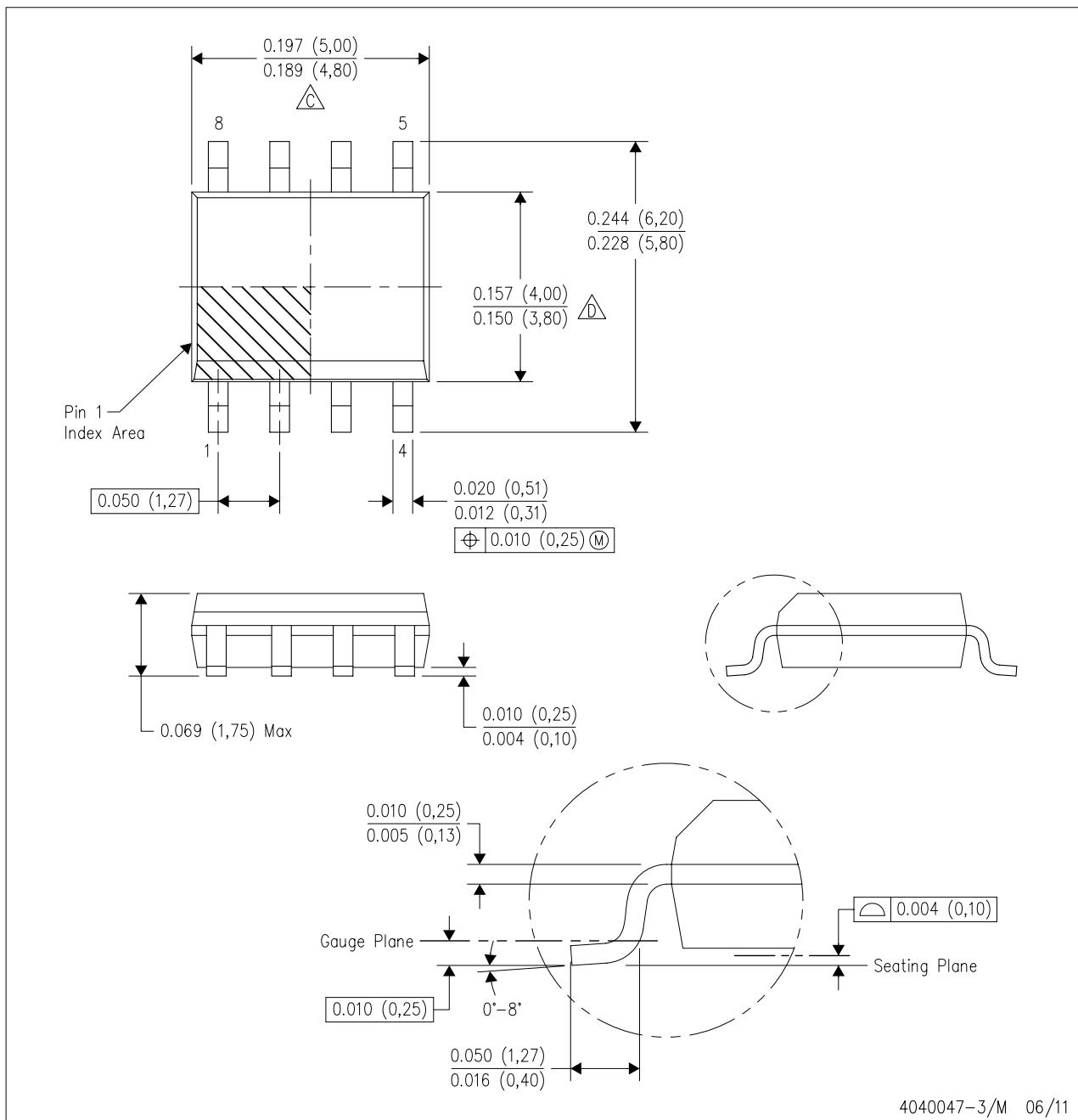
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

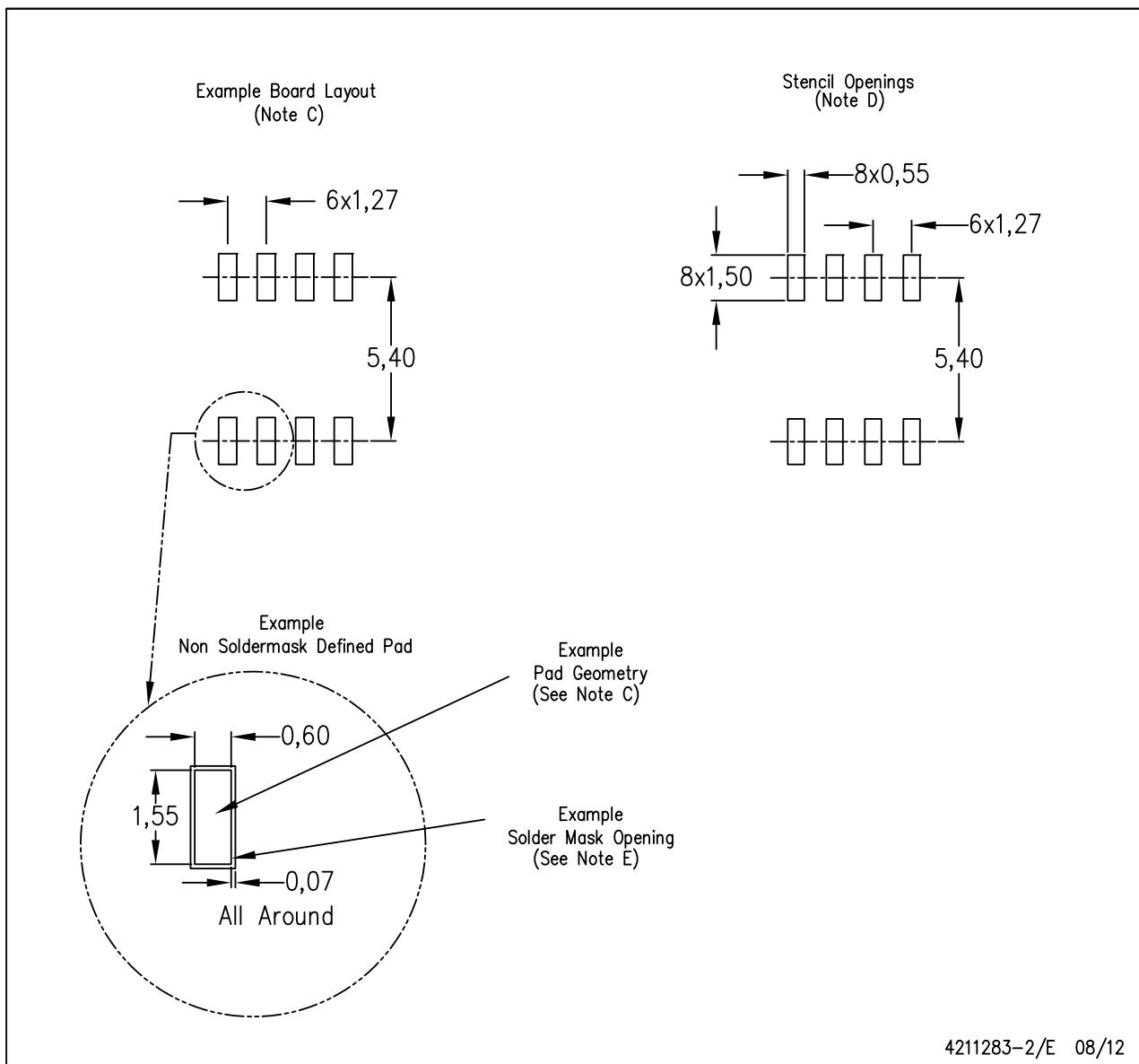
Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AA.

## LAND PATTERN DATA

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



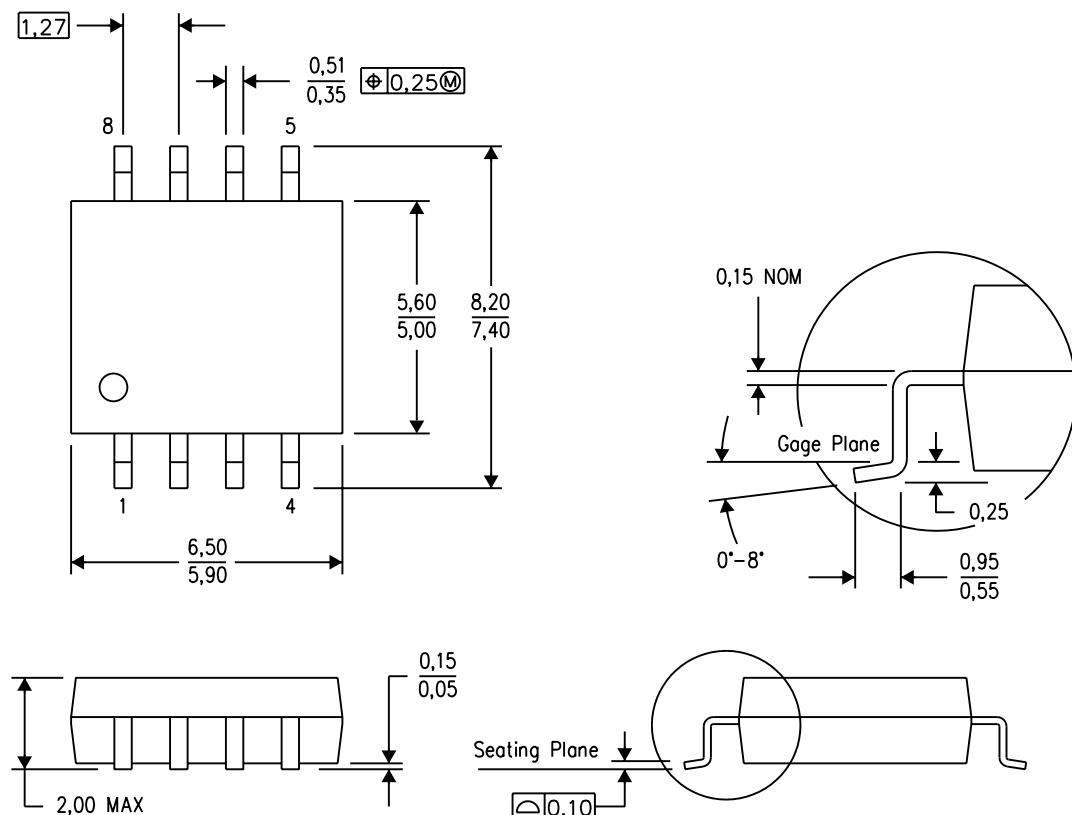
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4040063/C 03/03

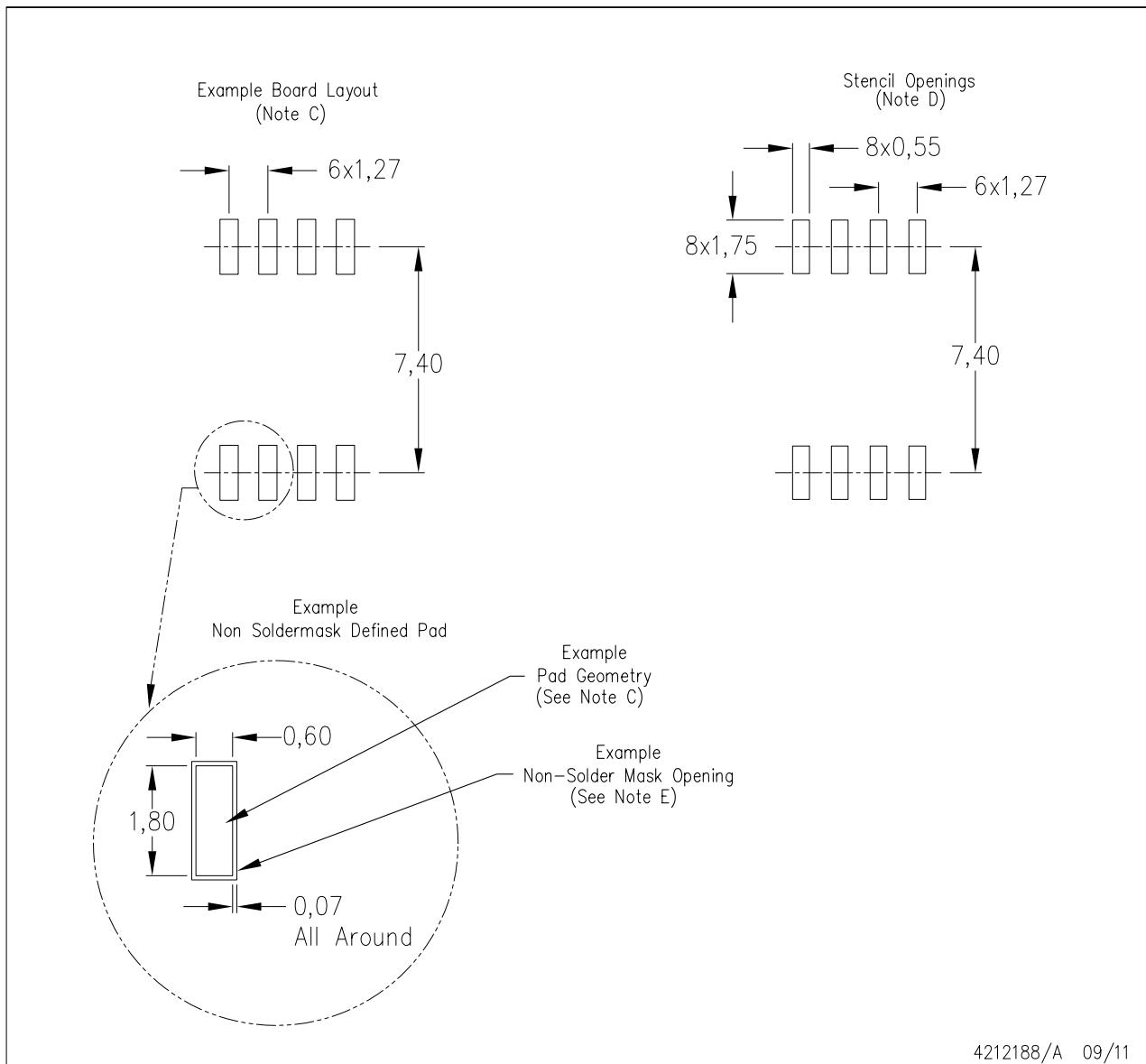
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

LAND PATTERN DATA

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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