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Diodes Incorporated
DMN62D0SFD-7

For any questions, you can email us directly:
sales@integrated-circuit.com

DIODES INCORPORATED

Lead-free Green

DMN62D0SFD

N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D T_A = 25°C
60V	2Ω @ V_{GS} = 10V	540mA
	3Ω @ V_{GS} = 5V	430mA

Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate to 2kV
- **Lead Free/RoHS Compliant (Note 1)**
- **Green Device (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description and Applications

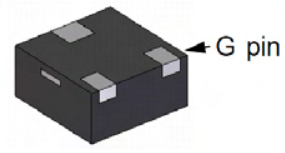
This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- DC-DC Converters
- Power management functions
- Battery Operated Systems and Solid-State Relays
- Load switch

Mechanical Data

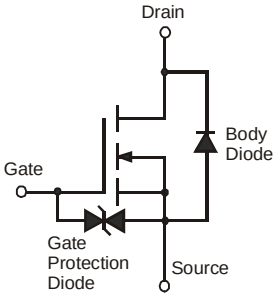
- Case: X1-DFN1212-3
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Solderable per MIL-STD-202, Method 208
- Terminals: Finish – NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Weight: 0.005 grams (approximate)

ESD PROTECTED TO 2kV

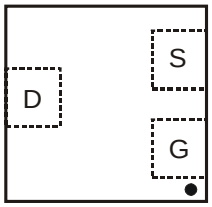


Top View

Bottom View



Equivalent Circuit



Top view
Pin-out

Ordering Information (Note 3)

Part Number	Case	Packaging
DMN62D0SFD-7	X1-DFN1212-3	3000/Tape & Reel

Notes: 1. No purposefully added lead.
2. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com
3. For packaging details, go to our website at http://www.diodes.com

Marking Information

K62 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: Y = 2011)
M = Month (ex: 9 = September)

Date Code Key

Year	2007	2008	2009	2010	2011	2012
Code	U	V	W	X	Y	Z

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = 10V	Steady State	T_A = 25°C T_A = 70°C	I_D	540 430	mA
	t<10s	T_A = 25°C T_A = 70°C	I_D	630 500	mA
Continuous Drain Current (Note 5) V_{GS} = 5V	Steady State	T_A = 25°C T_A = 70°C	I_D	430 340	mA
	t<10s	T_A = 25°C T_A = 70°C	I_D	510 410	mA
Pulsed Drain Current (10µs pulse, duty cycle = 1%)			I_{DM}	1.0	A
Maximum Body Diode Forward Current (Note 5)			I_S	1.0	A

Thermal Characteristics @T_A = 25°C unless otherwise specified

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 4)		P_D	0.43	W
Thermal Resistance, Junction to Ambient (Note 4)	Steady state	$R_{\theta JA}$	260	°C/W
	t<10s		182	°C/W
Total Power Dissipation (Note 5)		P_D	0.89	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	140	°C/W
	t<10s		98	°C/W
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	112	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	-	-	V	V_{GS} = 0V, I_D = 10µA
Zero Gate Voltage Drain Current T_J = 25°C	I_{DSS}	-	-	100	nA	V_{DS} = 60V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	10	µA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.6	2.5	V	V_{DS} = 10V, I_D = 1mA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	-	2	Ω	V_{GS} = 10V, I_D = 500mA
		-	-	3		V_{GS} = 5V, I_D = 50mA
Forward Transfer Admittance	$\|Y_{fs}\|$	-	130	-	mS	V_{DS} = 3V, I_D = 30mA
Diode Forward Voltage	V_{SD}	-	0.8	1.2	V	V_{GS} = 0V, I_S = 300mA
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	-	30.2	-	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	4.4	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	2.8	-	pF	
Gate Resistance	R_g	-	131	-	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	-	0.39	-	nC	V_{DS} = 10V, I_D = 1A
Total Gate Charge (V_{GS} = 10.0V)	Q_g	-	0.87	-	nC	
Gate-Source Charge	Q_{gs}	-	0.14	-	nC	
Gate-Drain Charge	Q_{gd}	-	0.09	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	3.95	-	ns	V_{DS} = 30V, I_D = 200mA V_{GS} = 10V, R_G = 25Ω
Turn-On Rise Time	t_r	-	3.81	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	16.0	-	ns	
Turn-Off Fall Time	t_f	-	9.04	-	ns	

Notes: 4. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate
6 .Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to production testing.

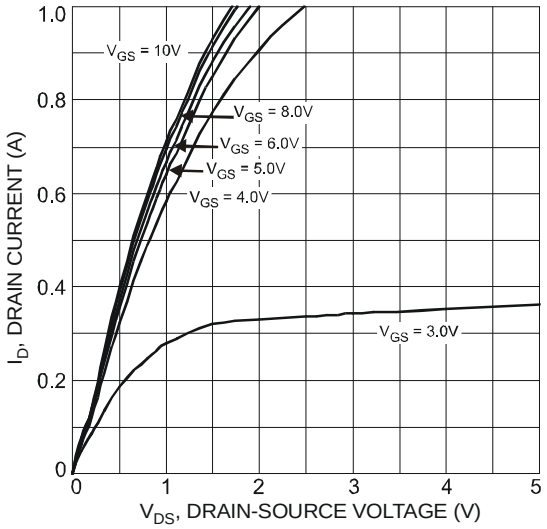


Fig.1 Typical Output Characteristic

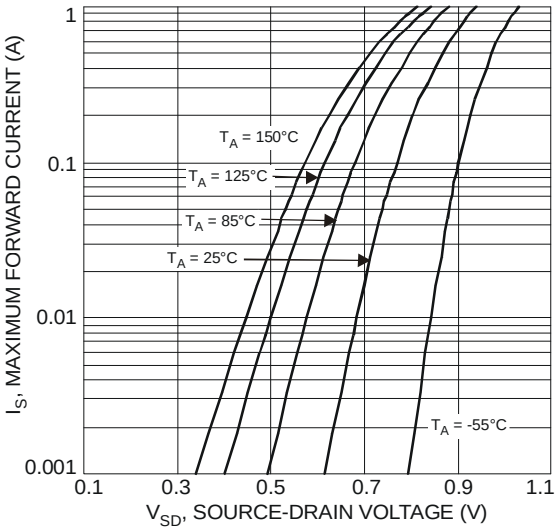


Fig. 2 Maximum Forward Current vs. Source-Drain Voltage

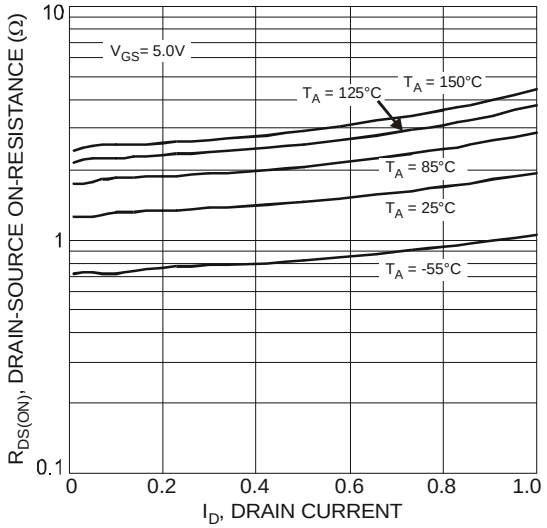


Fig. 3 Typical On-Resistance vs. Drain Current and Temperature

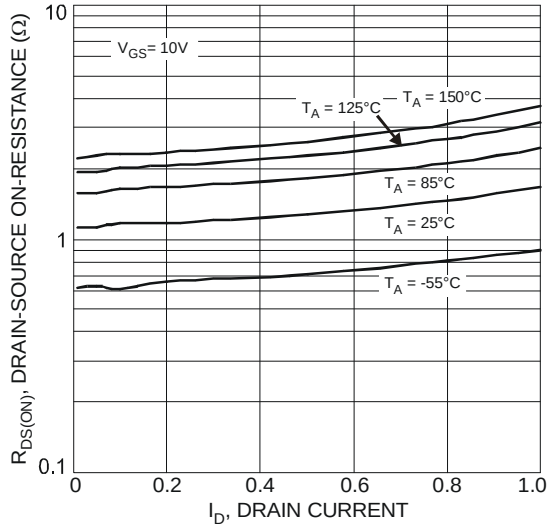


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

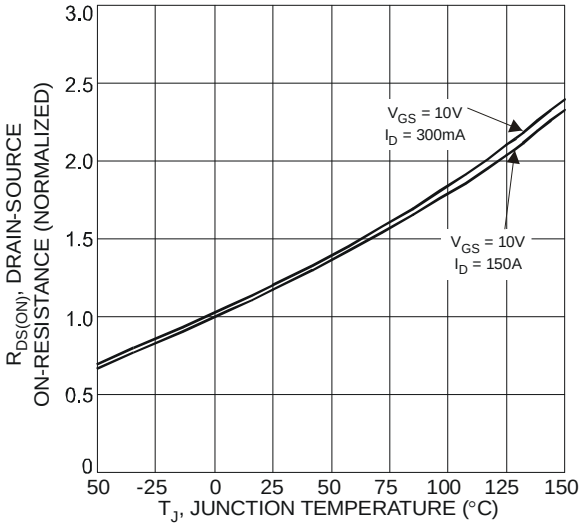


Fig. 5 On-Resistance Variation with Temperature

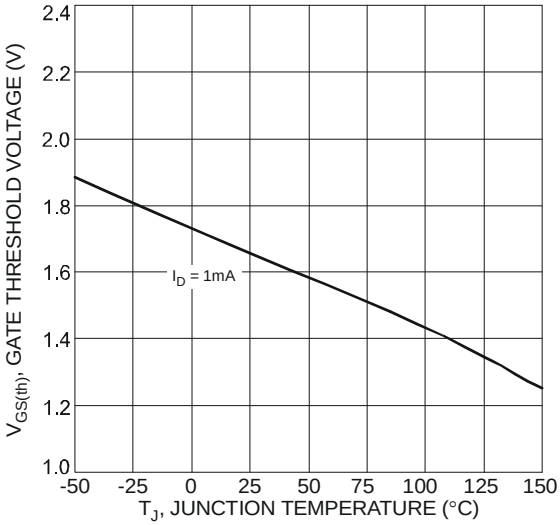


Fig. 6 Gate Threshold Variation vs. Ambient Temperature

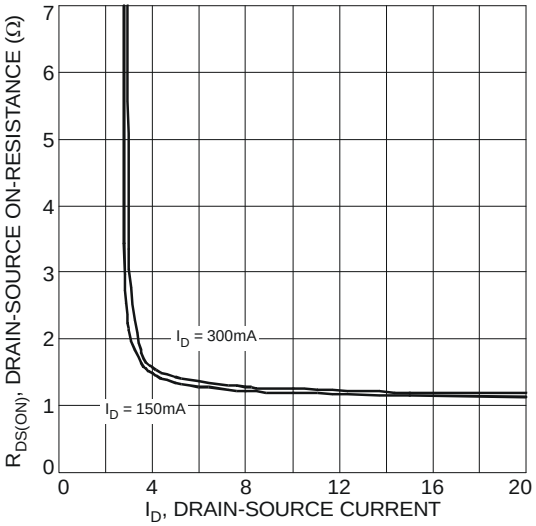


Fig. 7 Typical On-Resistance vs. Drain Current

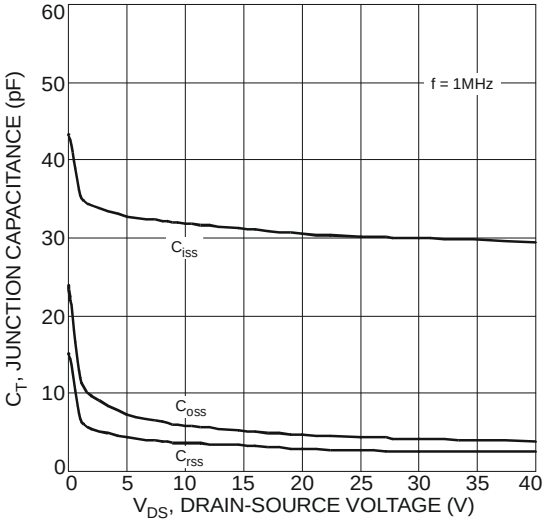


Fig. 8 Typical Junction Capacitance

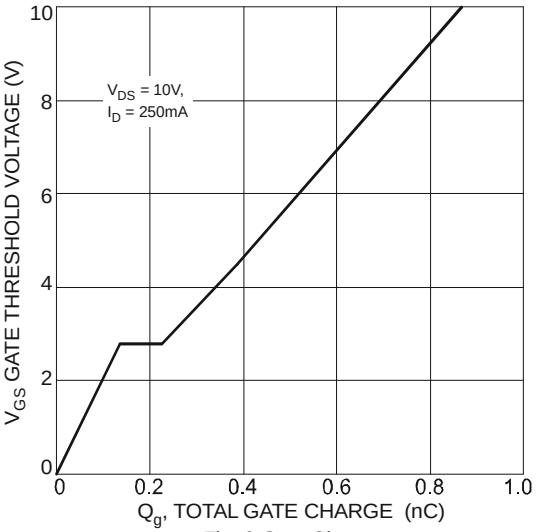


Fig. 9 Gate Charge

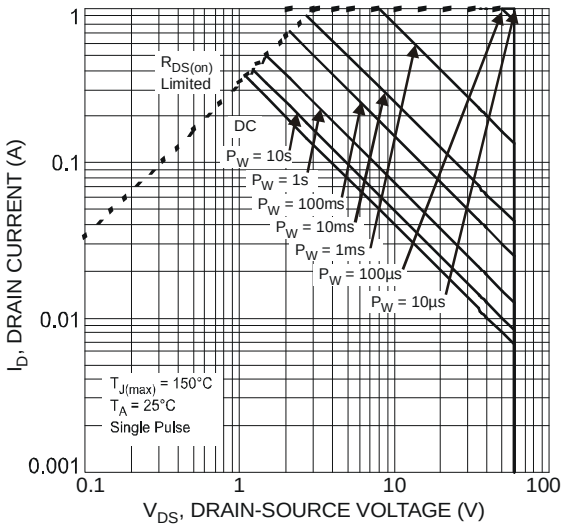


Fig. 10 SOA, Safe Operation Area

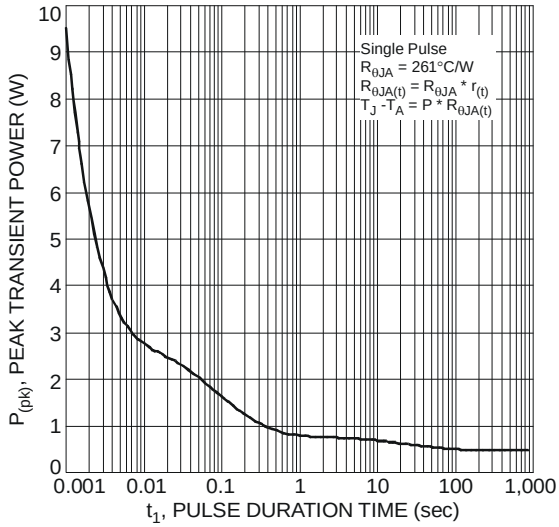


Fig. 11 Single Pulse Maximum Power Dissipation

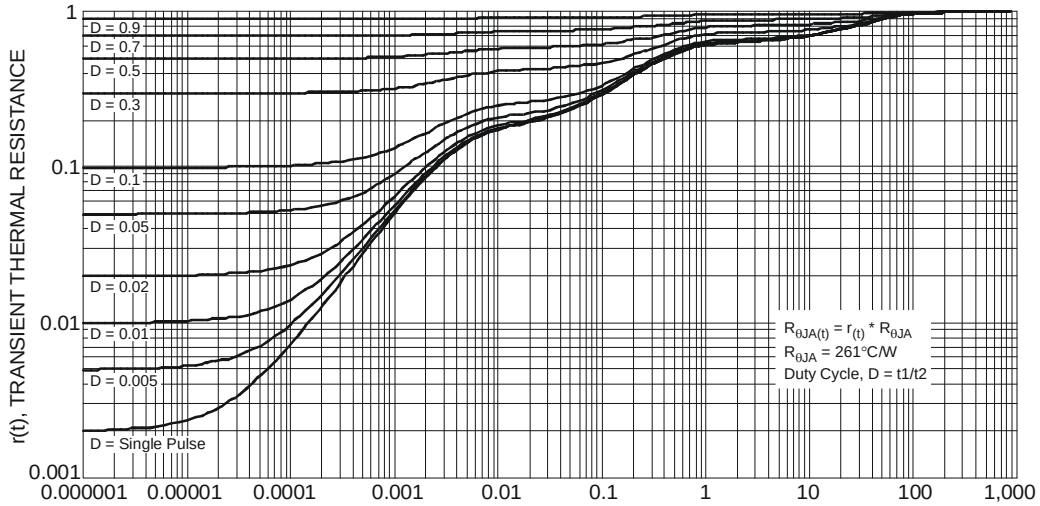
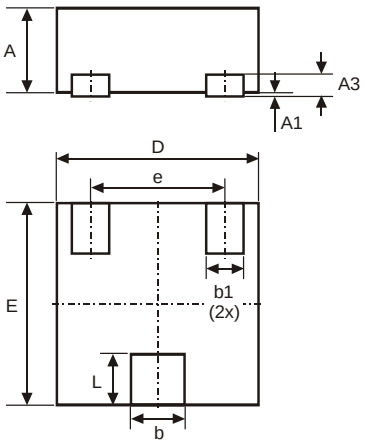


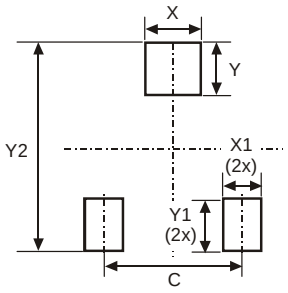
Fig. 12 Transient Thermal Resistance

Package Outline Dimensions



X1-DFN1212-3			
Dim	**Min**	**Max**	**Typ**
A	0.47	0.53	0.50
A1	0	0.05	0.02
A3	-	-	0.13
b	0.27	0.37	0.32
b1	0.17	0.27	0.22
D	1.15	1.25	1.20
E	1.15	1.25	1.20
e	-	-	0.80
L	0.25	0.35	0.30
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.80
X	0.42
X1	0.32
Y	0.50
Y1	0.50
Y2	1.50

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