# Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

NXP Semiconductors
P5020DS-PA

For any questions, you can email us directly:
sales@integrated-circuit.com

ommunications Platforms

# P Series

# QorIQ P5020 and P5010 communications processors

## Overview

The QorIQ P5 family delivers scalable 64-bit processing with single-, dual- and quad-core devices. With frequencies scaling up to 2.0 GHz, a tightly coupled cache hierarchy for low latency and integrated hardware acceleration, the P5020 (dual-core) and P5010 (single-core) devices are ideally suited for compute intensive, power-conscious control plane applications.

## Target Markets and Applications

The P5020 is designed for high-performance, power-constrained control plane applications and provides an ideal combination of core performance, integrated accelerators and advanced I/O required for the following compute-intensive applications:

- Enterprise equipment: Router, switch, services
- Data center: Server appliance, SAN storage controller, iSCSI controller, FCoE bridging
- Aerospace and defense
- Industrial computing: Single-board computers, test/measurement, robotics

## e5500 Core

The P5020 is based on the 64-bit e5500 Power Architecture® core. The e5500 core uses a seven-stage pipeline for low latency response to unpredictable code execution paths, boosting its single-threaded performance. Key features:

- Supports up to 2 GHz core frequencies
- Tightly coupled low latency cache hierarchy: 32 KB I/D (L1), 512 KB L2 per core
- Up to 2 MB of shared platform cache (L3)
- 3 DMIPS/MHz per core
- Up to 64 GB of addressable memory space
- Hybrid 32-bit mode to support legacy software and seamless transition to 64-bit architecture

## Virtualization

The P5020 includes support for hardware-assisted virtualization. The e5500 core offers an extra core privilege level (hypervisor). Virtualization software for the P5 family includes kernel-based virtual machine (KVM), Linux® containers, Freescale hypervisor and commercial virtualization software from Green Hills® Software and Enea®.

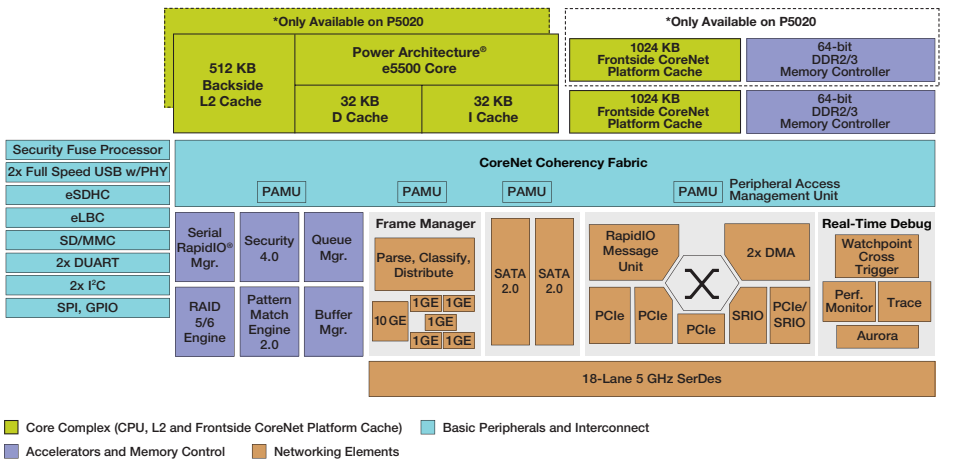
## DPAA Hardware Accelerators

| | |
|---|---|
| Frame manager (FMAN) | 12 Gb/s classify, parse and distribute |
| Buffer manager (BMAN) | 64 buffer pools |
| Queue manager (QMAN) | Up to $2^{24}$ queues |
| Security (SEC) | 17 Gb/s: 3 DES, AES |
| Pattern matching engine (PME) | 10 Gb/s aggregate |
| RapidIO® manager | Supports Type 9 and Type 11 messaging |
| RAID5/6 engine | Calculates parity for network attached storage and direct attached storage applications |

## Data Path Acceleration Architecture (DPAA)

The P5020 integrates QorIQ DPAA, an innovative multicore infrastructure for scheduling work to cores (physical and virtual), hardware accelerators and network interfaces. The FMAN, a primary element of the DPAA, parses headers from incoming packets and classifies and selects data buffers with optional policing and congestion management. The FMAN passes its work to the QMAN, which assigns it to cores or accelerators with a multi-level scheduling hierarchy. The P5020 also offers accelerators for cryptography, enhanced regular expression pattern matching and RAID5/6 offload.

## QorIQ P5020/P5010 Processors Block Diagram



## P5 Family Comparison Chart

| | P5020/P5010 | P5040/P5021 |
|---|---|---|
| CPU cores | 2x 64-bit e5500, 1x (P5010) | 4x 64-bit e5500, 2x (P5021) |
| Threads | 2/1 (single thread per core) | 4/2 (single thread per core) |
| Max core frequency | 1.6 to 2 GHz | 1.8 to 2.2 GHz |
| L2 | 512 KB per core | 512 KB per core |
| L3/Platform | 2 MB (P5020)/1 MB (P5010) | 2 MB (both P5040 and P5021) |
| DDR I/F | 2x 64-bit DDR3 (up to 1333 MT/s)<br>1x 64-bit DDR3 (P5010) | 2x 64-bit DDR3 (up to 1600 MT/s) |
| PCI Express® | 4x PCIe v2.0 | 3x PCIe v2.0 (incl. 1 x 8) |
| GbE, 10 GbE | 5x 1 GbE, 1x 10 GbE | 10x 1 GbE, 2x 10 GbE |
| SRIO | 2x SRIO v2.1 (supports Type 9 and 11 messaging) | N/A |
| SerDes lanes | 18 lanes | 20 lanes |
| Package | 1295-pin 37.5 x 37.5 mm FC-PBGA | 1295-pin 37.5 x 37.5 mm FC-PBGA |

## System Peripherals and Networking

For networking, the FMAN supports one 10 Gb/s and 5x 1 Gb/s MAC controllers that connect to PHYs, switches and backplanes over RGMII, SGMII and XAUI. High-speed system expansion is supported through four PCI Express v2.0 controllers that support a variety of lane widths. Other peripherals include SATA, SD/MMC, I²C, UART, SPI, NOR/NAND controller, GPIO and dual 1333 MT/s DDR3/3L controllers.

## Software and Tool Support

- Enea: Real-time operating system support and virtualization software
- Green Hills: Comprehensive portfolio of software and hardware development tools, trace tools, real-time operating systems and virtualization software
- Mentor Graphics®: Commercial-grade Linux solution
- QNX®: Real-time OS and development tool support
- QorIQ P5020 development system (P5020DS)

## P5020/P5010 Features List

| | |
|---|---|
| Two (P5020) or one (P5010) single threaded e5500 cores built on Power Architecture® technology | • Up to 2 GHz with 64-bit ISA support (Power Architecture V2.06 compliant)<br>• Three levels of instruction: User, supervisor, hypervisor<br>• Hybrid 32-bit mode to support legacy software and transition to 64-bit architecture |
| CoreNet platform cache (CPC) | • 2 MB configured as dual 1 MB blocks (1 MB only for P5010) |
| Hierarchical interconnect fabric | • CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet endpoints<br>• QMAN fabric supporting packet-level queue management and quality of service scheduling |
| Two 64-bit DDR3/3L SDRAM memory controllers with ECC and interleaving support | • Up to 1333 MT/s<br>• Memory pre-fetch engine |
| DPAA incorporating acceleration for the following functions | • Packet parsing, classification and distribution (FMAN)<br>• QMAN for scheduling, packet sequencing and congestion management<br>• Hardware BMAN for buffer allocation and de-allocation<br>• Cryptography acceleration (SEC 4.2) at up to 40 Gb/s<br>• RegEx pattern matching acceleration (PME 2.1) at up to 10 Gb/s |
| SerDes | • 18 lanes at up to 5 Gb/s<br>• Supports SGMII, XAUI, PCIe rev1.1/2.0, SATA |
| Ethernet interfaces | • One 10 Gb/s Ethernet MACs<br>• 5x 1 Gb/s Ethernet MACs |
| High-speed peripheral interfaces | • Four PCI Express 2.0 controllers<br>• Two Serial RapidIO controllers/ports (sRIO port) V1.3-compliant with features of V2.1<br>• Two serial ATA (SATA 2.0) controllers |
| Additional peripheral interfaces | • Two USB 2.0 Full-Speed controllers with integrated PHY<br>• Enhanced secure digital host controller (SD/MMC/eMMC)<br>• Enhanced serial peripheral interface<br>• Four I²C controllers<br>• Four UARTs<br>• Integrated flash controller supporting NAND and NOR flash |
| DMA | • Dual four channel |
| Support for hardware virtualization and partitioning enforcement | • Extra privileged level for hypervisor support |
| QorIQ trust architecture 1.1 | • Secure boot, secure debug, tamper detection, volatile key storage |

**For more information, please visit freescale.com/QorIQ**



Document Number: QP5020FS REV 6