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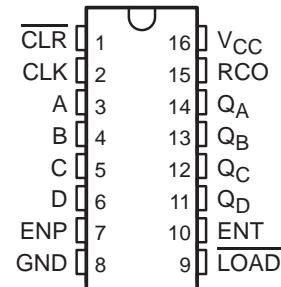
sales@integrated-circuit.com

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) DIPs

**SN54ALS161B, SN54ALS162B, SN54ALS163B,
SN54AS161, SN54AS163 . . . J PACKAGE**
**SN74ALS161B, SN74AS161,
SN74AS163 . . . D OR N PACKAGE**
SN74ALS163B . . . D, DB, OR N PACKAGE
(TOP VIEW)



description

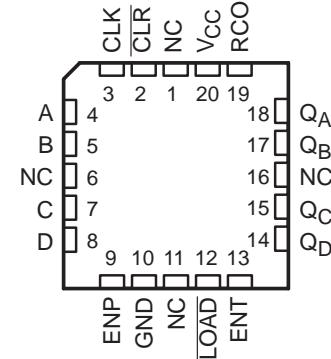
These synchronous, presetable, 4-bit decade and binary counters feature an internal carry look-ahead circuitry for application in high-speed counting designs. The SN54ALS162B is a 4-bit decade counter. The 'ALS161B, 'ALS163B, 'AS161, and 'AS163 devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; they can be preset to any number between 0 and 9 or 15. Because presetting is synchronous, setting up a low level at the load (LOAD) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'ALS161B and 'AS161 devices is asynchronous. A low level at the clear (CLR) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, LOAD, or enable inputs. The clear function for the SN54ALS162B, 'ALS163B, and 'AS163 devices is synchronous, and a low level at CLR sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to CLR to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP and ENT inputs and a ripple-carry (RCO) output are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled,

**SN54ALS161B, SN54ALS162B, SN54ALS163B,
SN54AS161, SN54AS163 . . . FK PACKAGE**
(TOP VIEW)



NC – No internal connection



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SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163

SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163

SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

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description (continued)

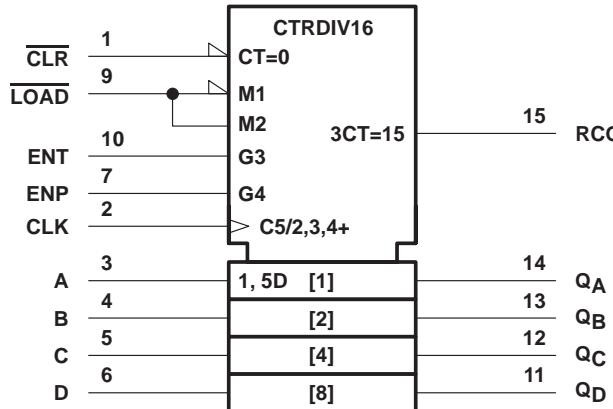
produces a high-level pulse while the count is maximum (9 or 15, with Q_A high). The high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

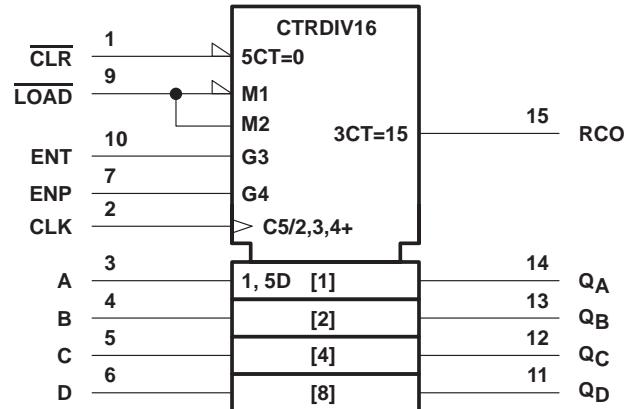
The SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, and SN54AS163 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS161B, SN74ALS163B, SN74AS161, and SN74AS163 are characterized for operation from 0°C to 70°C .

logic symbols†

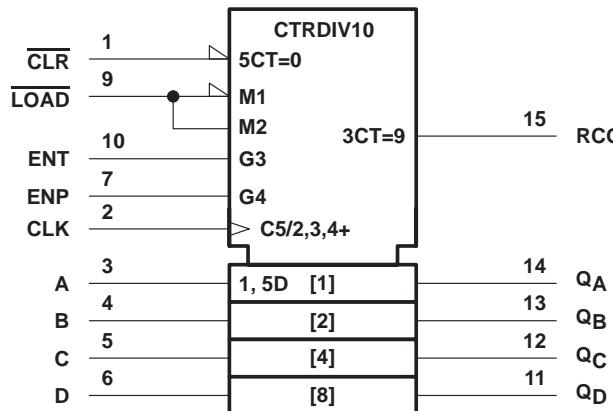
'ALS161B AND 'AS161 BINARY COUNTERS
WITH DIRECT CLEAR



'ALS163B AND 'AS163 BINARY COUNTERS
WITH SYNCHRONOUS CLEAR



SN54ALS162B DECADE COUNTER
WITH SYNCHRONOUS CLEAR

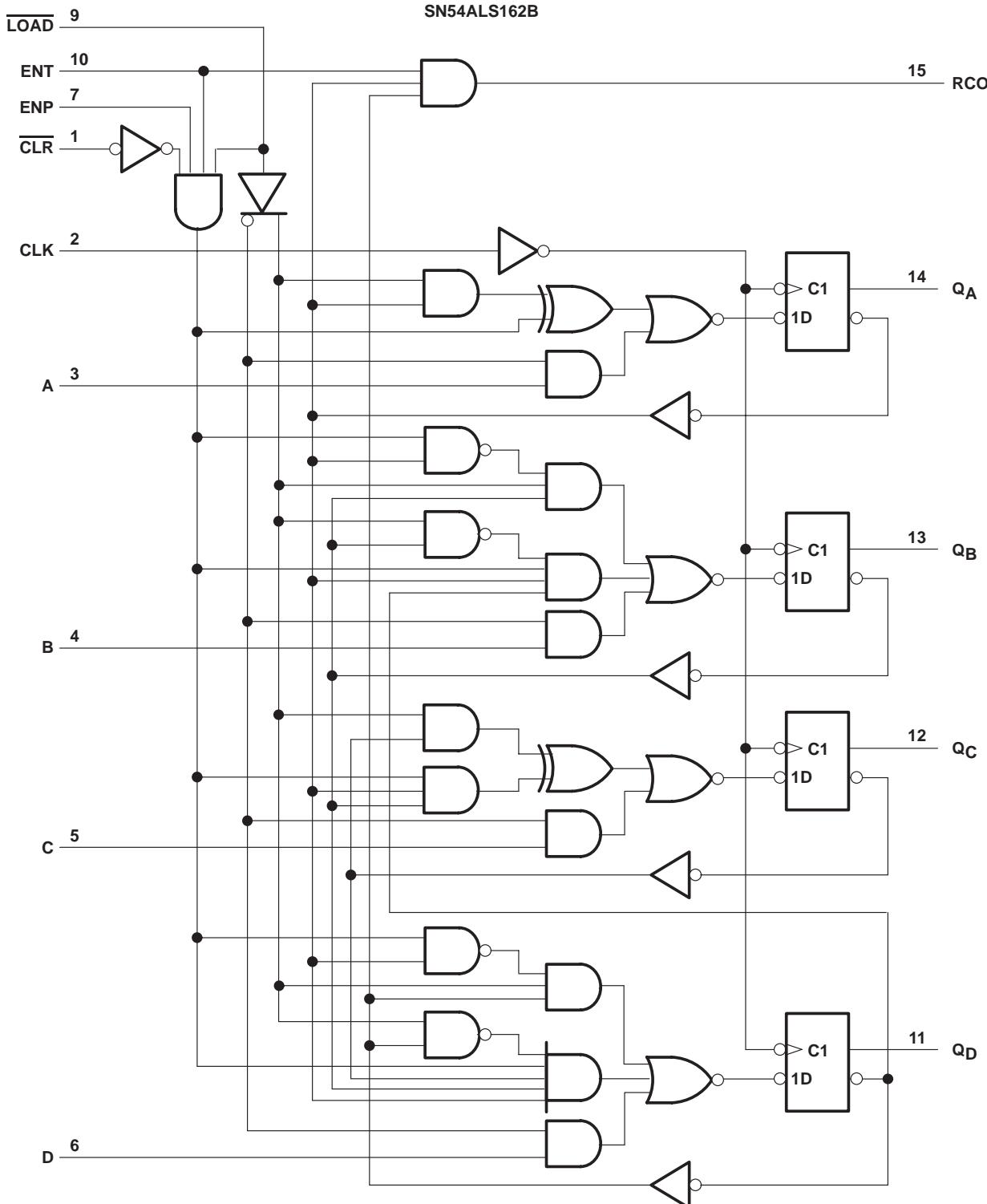


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the D, DB, J, and N packages.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

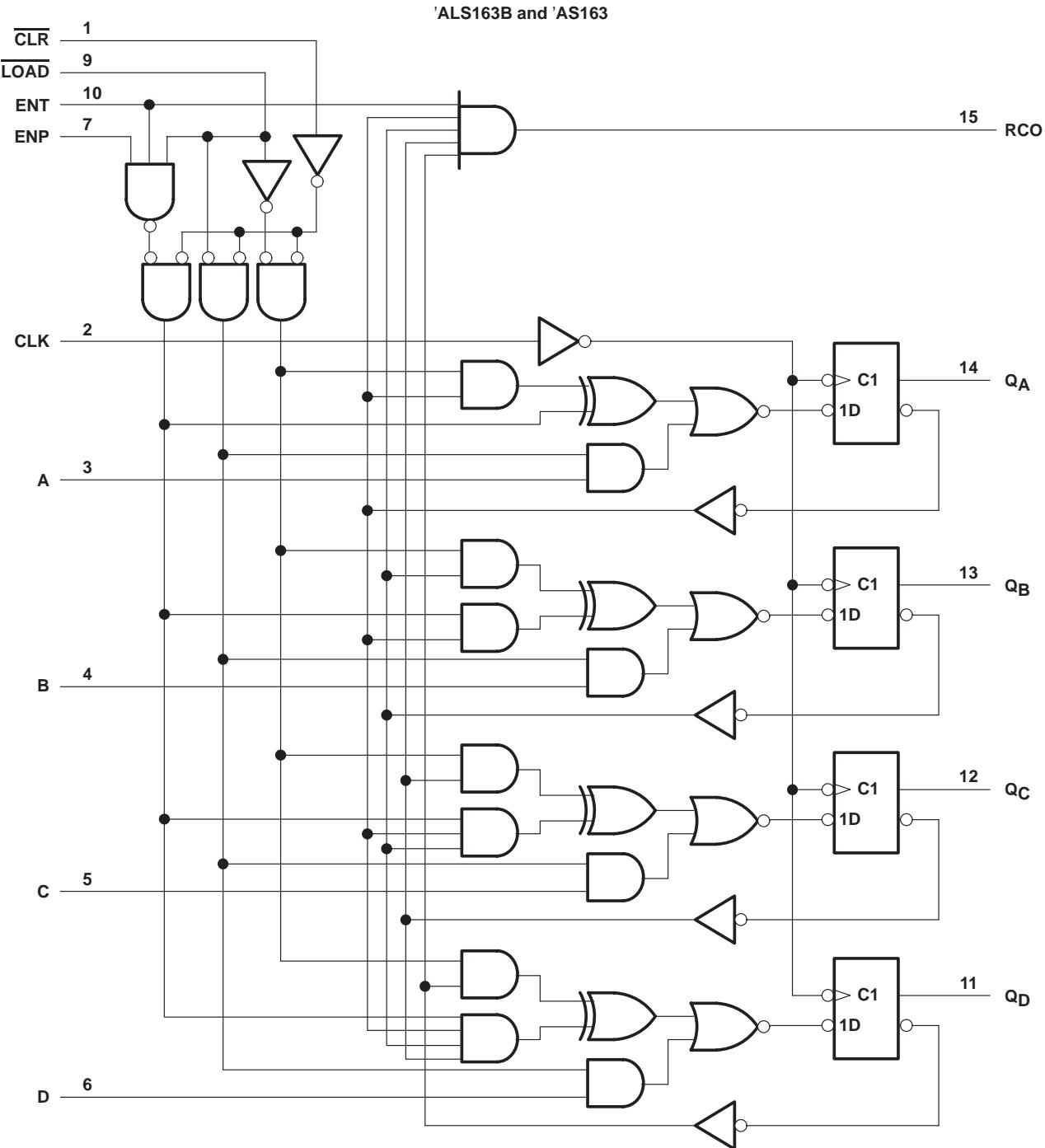
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logic diagram (positive logic)



SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS
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logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and N packages.

'ALS161B and 'AS161 synchronous binary counters are similar; however, $\overline{\text{CLR}}$ is asynchronous.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163

SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163

SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

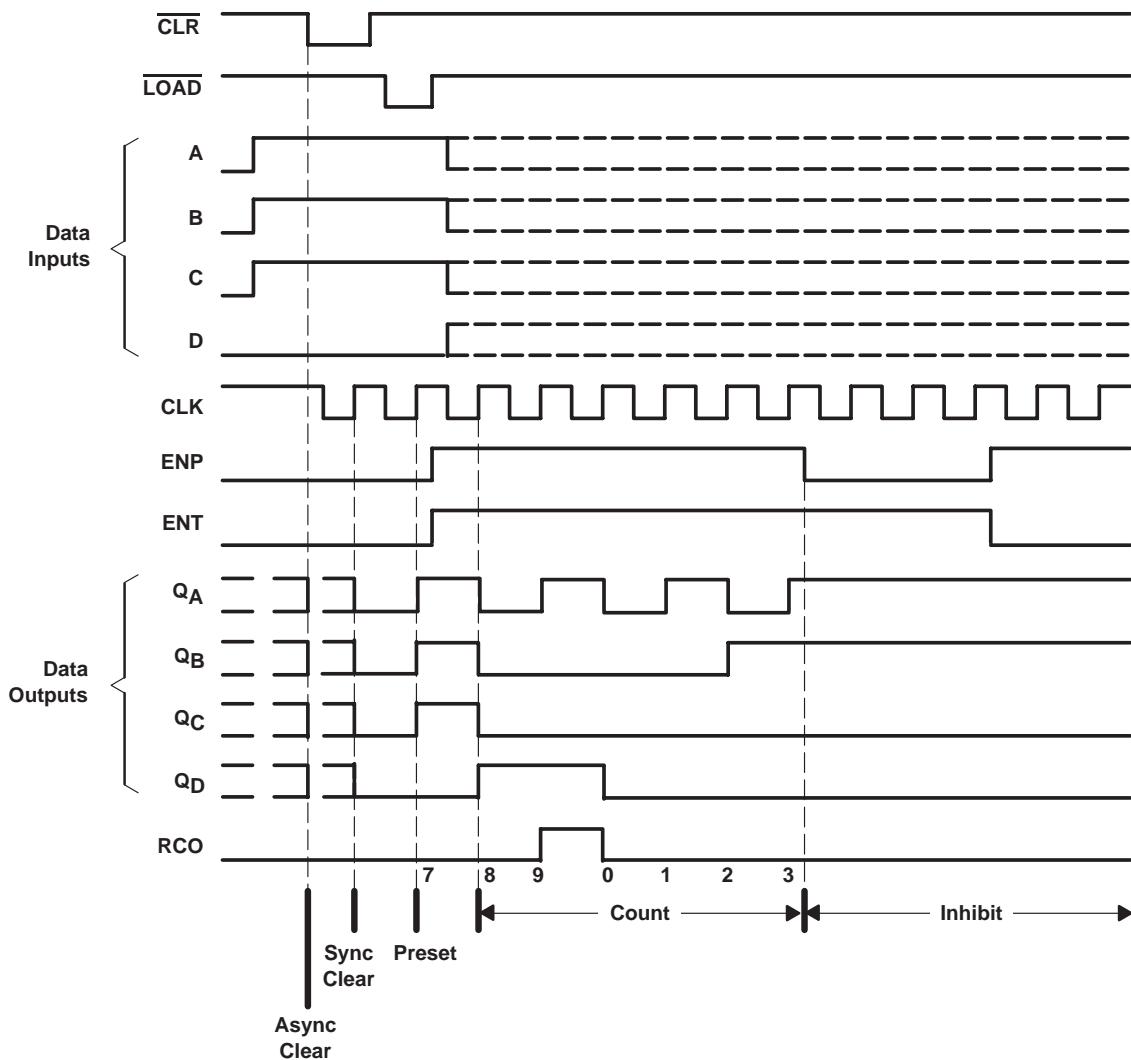
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typical clear, preset, count, and inhibit sequences

SN54ALS162B

The following sequence is illustrated below:

1. Clear outputs to zero (SN54ALS162B is synchronous)
2. Preset to BCD 7
3. Count to 8, 9, 0, 1, 2, and 3
4. Inhibit



SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163

SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163

SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

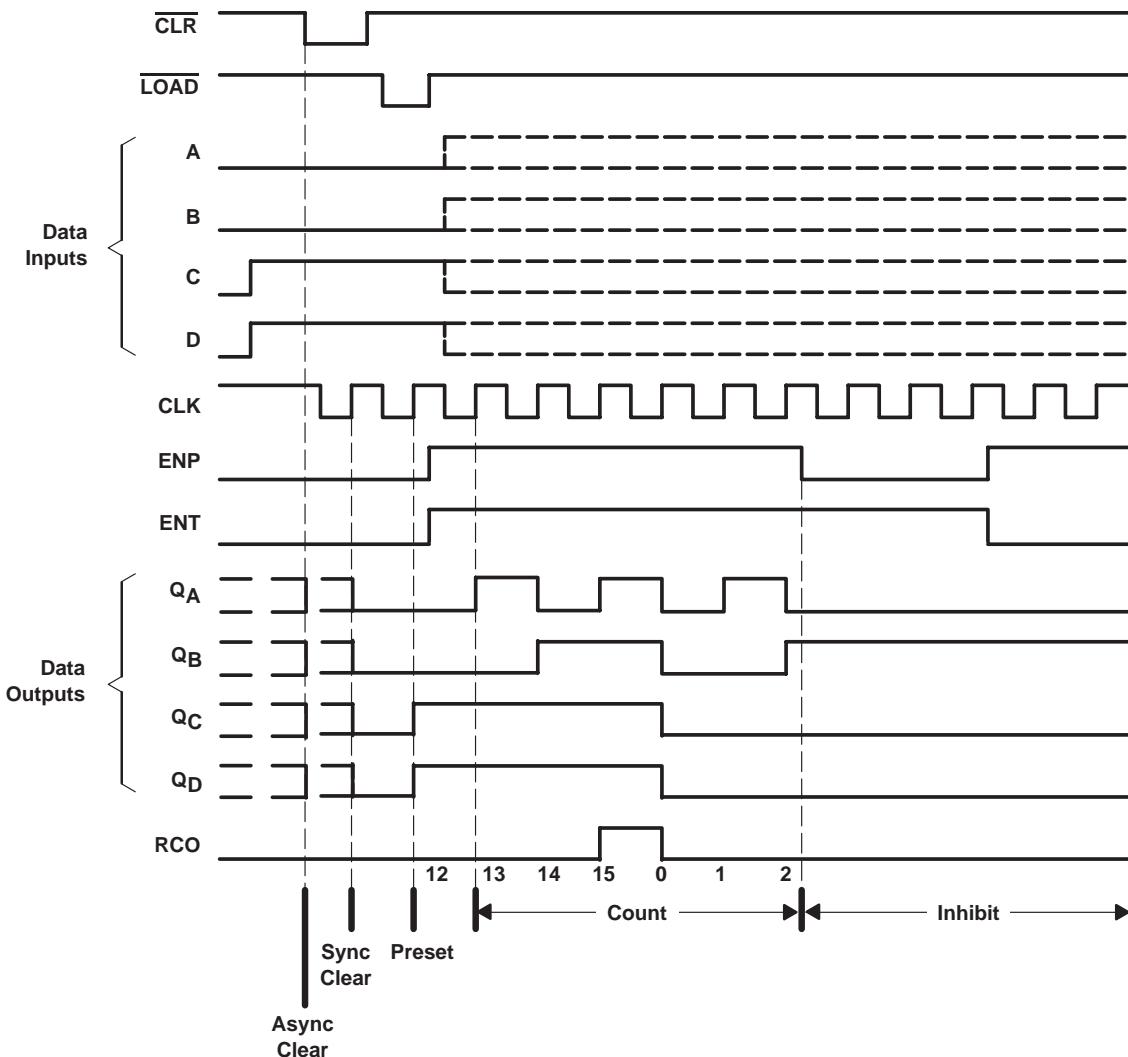
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typical clear, preset, count, and inhibit sequences

'ALS161B, 'AS161, 'ALS163B, and 'AS163

The following sequence is illustrated below:

1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous.)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

| | | SN54ALS161B | | | SN74ALS161B | | | UNIT | | |
|-----------------|--------------------------------|-------------|-----|-----|-------------|-----|-----|------|--|--|
| | | SN54ALS162B | | | SN74ALS163B | | | | | |
| | | MIN | NOM | MAX | MIN | NOM | MAX | | | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V | | |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V | | |
| V _{IL} | Low-level input voltage | 0.7 | | | 0.8 | | | V | | |
| I _{OH} | High-level output current | -0.4 | | | -0.4 | | | mA | | |
| I _{OL} | Low-level output current | 4 | | | 8 | | | mA | | |
| T _A | Operating free-air temperature | -55 | | | 125 | | | 0 | | |
| | | | | | 70 | | | °C | | |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54ALS161B | | | SN74ALS161B | | | UNIT |
|-----------|----------------------------------------------------------------------------|-------------------------|------|------|--------------|------|------|---------------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | $V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$ | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | V |
| V_{OL} | $V_{CC} = 4.5 \text{ V}$ | $I_{OL} = 4 \text{ mA}$ | | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | $I_{OL} = 8 \text{ mA}$ | | | | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$ | | | 0.1 | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$ | | | 20 | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$ | | | -0.2 | | | -0.2 | mA |
| $I_O\$$ | $V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$ | -20 | | -112 | -30 | | -112 | mA |
| I_{CC} | $V_{CC} = 5.5 \text{ V}$ | | 12 | 21 | | 12 | 21 | mA |

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163

SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163

SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

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timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 1)

| | | | | SN54ALS161B SN54ALS162B SN54ALS163B | SN74ALS161B SN74ALS163B | UNIT |
|-------------|-------------------------------------------------------|-----------------------|--------------|-------------------------------------------|----------------------------|------|
| | | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | | | 22 | 40 | MHz |
| t_w | Pulse duration | CLR high or low | | 20 | 12.5 | ns |
| | | 'ALS161B | CLR low | 20 | 15 | |
| t_{su} | Setup time, before $CLK\uparrow$ | A, B, C, D | | 50 | 15 | |
| | | LOAD | | 20 | 15 | |
| | | 'ALS161B | ENP, ENT | 25 | 15 | |
| | | SN54ALS162B, 'ALS163B | | 20 | 15 | |
| | | 'ALS161B | CLR inactive | 10 | 10 | |
| | | | CLR low | 20 | 15 | |
| | | SN54ALS162B, 'ALS163B | CLR high | 20 | 10 | |
| t_h | Hold time, all synchronous inputs after $CLK\uparrow$ | | | 0 | 0 | ns |

switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALS161B | SN74ALS161B | UNIT |
|-----------|-----------------|----------------|-------------|-------------|------|
| | | | MIN | MAX | |
| f_{max} | | | 22 | 40 | MHz |
| t_{PLH} | CLK | RCO | 5 | 34 | 5 |
| t_{PHL} | | | 5 | 27 | 20 |
| t_{PLH} | CLK | Any Q | 4 | 19 | 4 |
| t_{PHL} | | | 6 | 25 | 15 |
| t_{PLH} | ENT | RCO | 3 | 18 | 6 |
| t_{PHL} | | | 3 | 17 | 20 |
| t_{PHL} | CLR | Any Q | 8 | 27 | 3 |
| | | RCO | 11 | 32 | 13 |
| | | | | | ns |

switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALS162B SN54ALS163B | SN74ALS163B | UNIT |
|-----------|-----------------|----------------|----------------------------|-------------|------|
| | | | MIN | MAX | |
| f_{max} | | | 22 | 40 | MHz |
| t_{PLH} | CLK | RCO | 5 | 25 | 5 |
| t_{PHL} | | | 5 | 25 | 20 |
| t_{PLH} | CLK | Any Q | 4 | 18 | 4 |
| t_{PHL} | | | 6 | 25 | 15 |
| t_{PLH} | ENT | RCO | 3 | 16 | 6 |
| t_{PHL} | | | 3 | 16 | 20 |
| | | | | | ns |

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

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recommended operating conditions

| | | SN54AS161 | | | SN74AS161 | | | UNIT | |
|-----------------|--------------------------------|-----------|-----|-----|-----------|-----|-----|------|--|
| | | SN54AS163 | | | SN74AS163 | | | | |
| | | MIN | NOM | MAX | MIN | NOM | MAX | | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V | |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V | |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V | |
| I _{OH} | High-level output current | | | -2 | | | -2 | mA | |
| I _{OL} | Low-level output current | | | 20 | | | 20 | mA | |
| T _A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C | |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54AS161 | | | SN74AS161 | | | UNIT |
|------------------|-----------------------------------------------------------|-------------------------------------------------|------|------|---------------------|------|------|------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | | -1.2 | V |
| V _{OH} | V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA | V _{CC} - 2 | | | V _{CC} - 2 | | | V |
| V _{OL} | V _{CC} = 4.5 V, I _{OL} = 20 mA | 0.25 | 0.5 | | 0.25 | 0.5 | | V |
| I _I | LOAD | | | 0.3 | | | 0.3 | mA |
| | ENT | V _{CC} = 5.5 V, V _I = 7 V | | 0.2 | | | 0.2 | |
| | All others | | | 0.1 | | | 0.1 | |
| I _{IH} | LOAD | V _{CC} = 5.5 V, V _I = 2.7 V | | 60 | | | 60 | μA |
| | ENT | | | 40 | | | 40 | |
| | All others | | | 20 | | | 20 | |
| I _{IIL} | LOAD | V _{CC} = 5.5 V, V _I = 0.4 V | | -1.5 | | | -1.5 | mA |
| | ENT | | | -1 | | | -1 | |
| | All others | | | -0.5 | | | -0.5 | |
| I _O ‡ | V _{CC} = 5.5 V, V _O = 2.25 V | -30 | -112 | | -30 | -112 | | mA |
| I _{CC} | V _{CC} = 5.5 V | 35 | 53 | | 35 | 53 | | mA |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163

SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163

SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

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timing requirements over recommended operating conditions (see Figure 1)

| | | | | SN54AS161 | SN74AS161 | UNIT | |
|-------------|----------------------------------------------|-----------------|---------------------|-----------|-----------|------|-----|
| | | | | MIN | MAX | MIN | MAX |
| f_{clock} | Clock frequency | | | | 65 | 75 | MHz |
| t_w | Pulse duration | CLR high or low | | 7.7 | 6.7 | ns | |
| | | 'AS161 | CLR low | 10 | 8 | | |
| t_{su} | Setup time, before CLK↑ | A, B, C, D | | 10 | 8 | ns | |
| | | LOAD | | 10 | 8 | | |
| | | ENP, ENT | | 10 | 8 | | |
| | | 'AS161 | CLR inactive | 10 | 8 | | |
| | | 'AS163 | CLR low | 14 | 12 | | |
| | | | CLR high (inactive) | 10 | 9 | | |
| t_h | Hold time, all synchronous inputs after CLK↑ | | | 2 | 0 | ns | |

switching characteristics over recommended operating conditions (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54AS161 | SN74AS161 | UNIT | |
|-----------|-----------------|----------------------|-----------|-----------|------|------|
| | | | MIN | MAX | | |
| f_{max} | | | 65* | 75 | MHz | |
| t_{PLH} | CLK | RCO (with LOAD high) | 1 | 8.5 | 1 | 8 |
| | | RCO (with LOAD low) | 3 | 17.5 | 3 | 16.5 |
| t_{PHL} | CLK | RCO | 2 | 14 | 2 | 12.5 |
| t_{PLH} | CLK | Any Q | 1 | 7.5 | 1 | 7 |
| | | | 2 | 14 | 2 | 13 |
| t_{PLH} | ENT | RCO | 1.5 | 10 | 1.5 | 9 |
| | | | 1 | 9.5 | 1 | 8.5 |
| t_{PHL} | CLR | Any Q | 2 | 14 | 2 | 13 |
| | | RCO | 2 | 14 | 2 | 12.5 |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating conditions (see Figure 1)

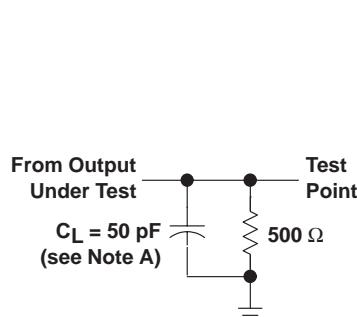
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54AS163 | SN74AS163 | UNIT | |
|-----------|-----------------|----------------------|-----------|-----------|------|------|
| | | | MIN | MAX | | |
| f_{max} | | | 65* | 75 | MHz | |
| t_{PLH} | CLK | RCO (with LOAD high) | 1 | 8.5 | 1 | 8 |
| | | RCO (with LOAD low) | 3 | 17.5 | 3 | 16.5 |
| t_{PHL} | CLK | RCO | 2 | 14 | 2 | 12.5 |
| t_{PLH} | CLK | Any Q | 1 | 7.5 | 1 | 7 |
| | | | 2 | 14 | 2 | 13 |
| t_{PLH} | ENT | RCO | 1.5 | 10 | 1.5 | 9 |
| | | | 1 | 9.5 | 1 | 8.5 |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

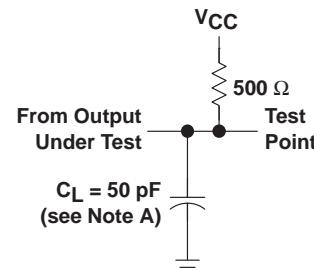
SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

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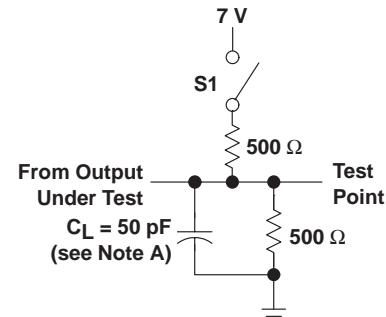
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



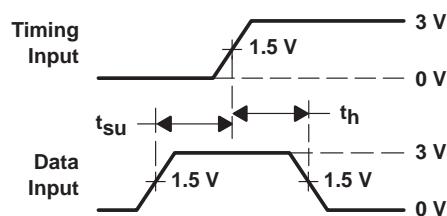
LOAD CIRCUIT FOR
BI-STATE TOTEM-POLE OUTPUTS



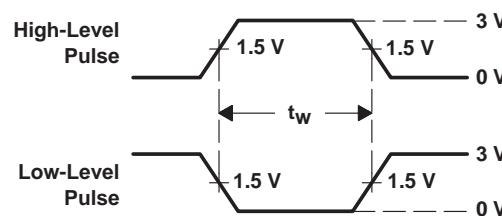
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



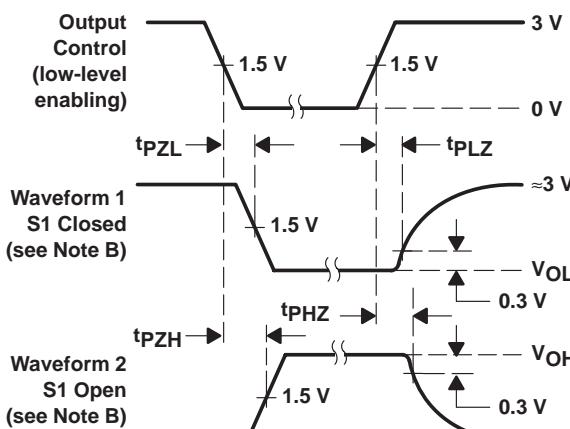
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



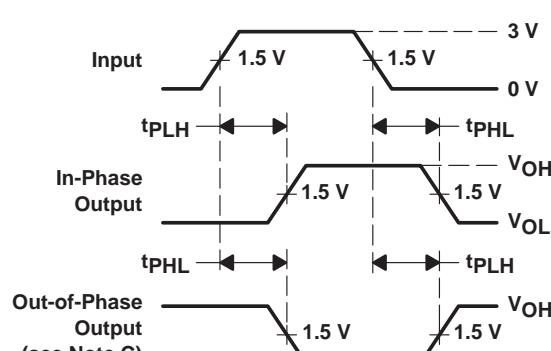
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- When measuring propagation delay items of 3-state outputs, switch S1 is open.
- All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163

SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163

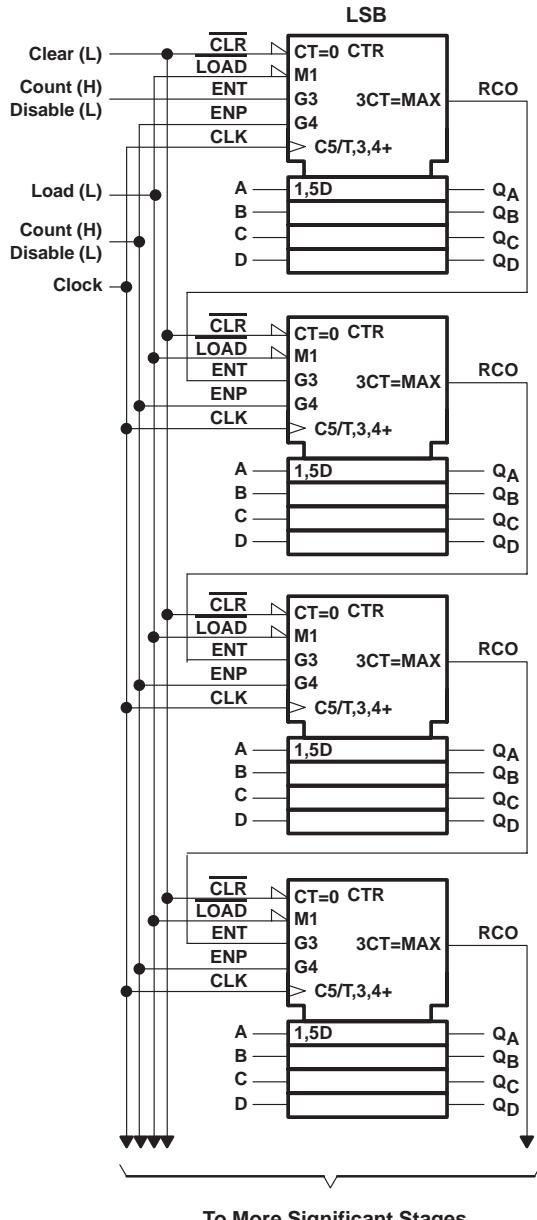
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

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APPLICATION INFORMATION

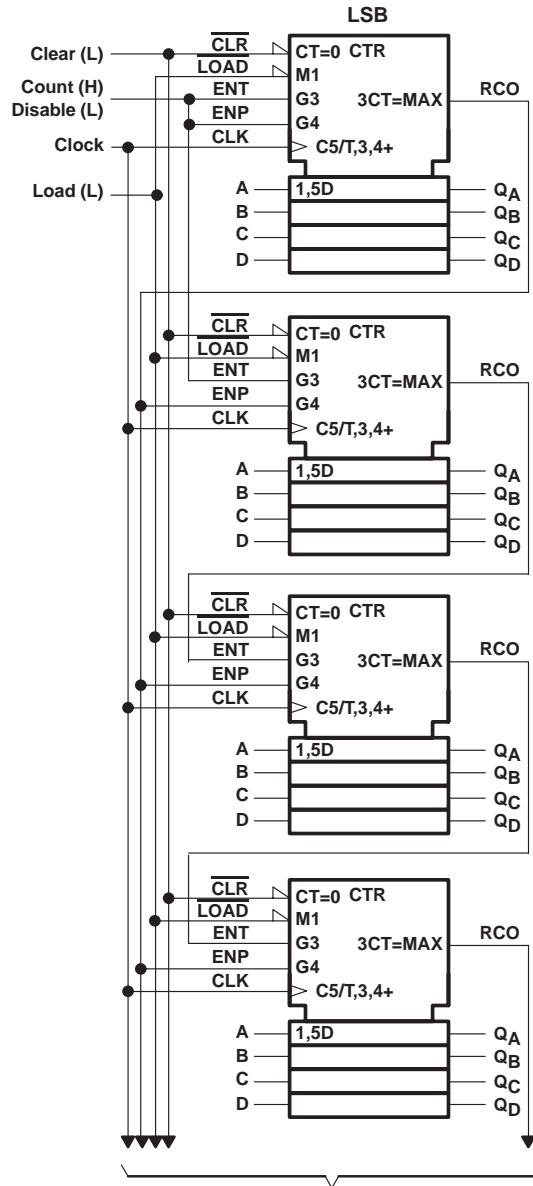
n-bit synchronous counters

This application demonstrates how the ripple-mode carry circuit (see Figure 2) and the carry look-ahead circuit (see Figure 3) can be used to implement a high-speed n-bit counter. The SN54ALS162B counts in BCD. The 'ALS161B, 'AS161, 'ALS163B, and 'AS163 devices count in binary. When additional stages are added, the f_{max} decreases in Figure 2, but remains unchanged in Figure 3.



$$f_{max} = 1/(CLK to RCO t_{PLH}) + (ENT to RCO t_{PLH}) (N - 2) + (ENT t_{SU})$$

Figure 2. Ripple-Mode Carry Circuit



$$f_{max} = 1/(CLK to RCO t_{PLH}) + (ENP t_{SU})$$

Figure 3. Carry Look-Ahead Circuit

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|-------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 83022012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 83022012A SNJ54ALS 161BFK | Samples |
| 8302201EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8302201EA SNJ54ALS161BJ | Samples |
| 8302201FA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8302201FA SNJ54ALS161BW | Samples |
| 83022022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 83022022A SNJ54ALS 163BFK | Samples |
| 8302202EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8302202EA SNJ54ALS163BJ | Samples |
| 8302202FA | OBsolete | CFP | W | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |
| JM38510/38001B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 38001B2A | Samples |
| JM38510/38001BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 38001BEA | Samples |
| JM38510/38002B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 38002B2A | Samples |
| JM38510/38002BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 38002BEA | Samples |
| M38510/38001B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 38001B2A | Samples |
| M38510/38001BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 38001BEA | Samples |
| M38510/38002B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 38002B2A | Samples |
| M38510/38002BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 38002BEA | Samples |
| SN54ALS161BJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54ALS161BJ | Samples |
| SN54ALS163BJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54ALS163BJ | Samples |
| SN54AS163J | OBsolete | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-------------------------|-------------------------|----------------------|--------------|---------------------------------|-------------------------|
| SN74ALS161BD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS161B | Samples |
| SN74ALS161BDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS161B | Samples |
| SN74ALS161BDRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS161B | Samples |
| SN74ALS161BN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS161BN | Samples |
| SN74ALS161BN3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74ALS161BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS161B | Samples |
| SN74ALS163BD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS163B | Samples |
| SN74ALS163BDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS163B | Samples |
| SN74ALS163BDRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS163B | Samples |
| SN74ALS163BN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS163BN | Samples |
| SN74ALS163BN3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74ALS163BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS163B | Samples |
| SN74AS161N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS161N | Samples |
| SN74AS161NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS161 | Samples |
| SN74AS163D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS163 | Samples |
| SN74AS163N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS163N | Samples |
| SN74AS163NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS163N | Samples |
| SNJ54ALS161BFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 83022012A SNJ54ALS 161BFK | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|-------------------------|----------------------|--------------|--------------------------------|----------------|
| SNJ54ALS161BJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8302201EA SNJ54ALS161BJ | Samples |
| SNJ54ALS161BW | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8302201FA SNJ54ALS161BW | Samples |
| SNJ54ALS163BFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 8302202A SNJ54ALS 163BFK | Samples |
| SNJ54ALS163BJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8302202EA SNJ54ALS163BJ | Samples |
| SNJ54AS161J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54AS161J | Samples |
| SNJ54AS163J | OBsolete | CDIP | J | 16 | | TBD | Call TI | Call TI | -55 to 125 | | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS161B, SN54ALS163B, SN54AS161, SN54AS163, SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 :

• Catalog: [SN74ALS161B](#), [SN74ALS163B](#), [SN74AS161](#), [SN74AS163](#)

• Military: [SN54ALS161B](#), [SN54ALS163B](#), [SN54AS161](#), [SN54AS163](#)

NOTE: Qualified Version Definitions:

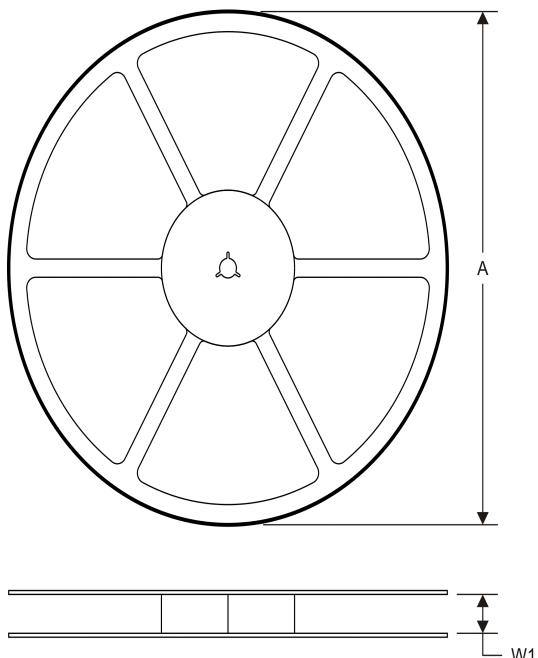
• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

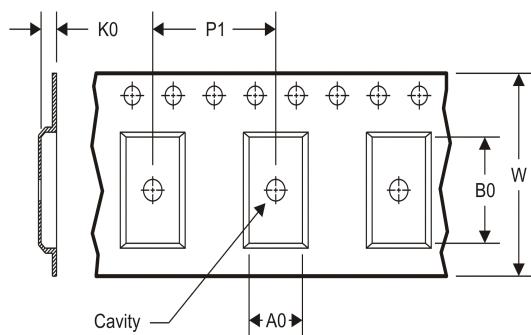
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



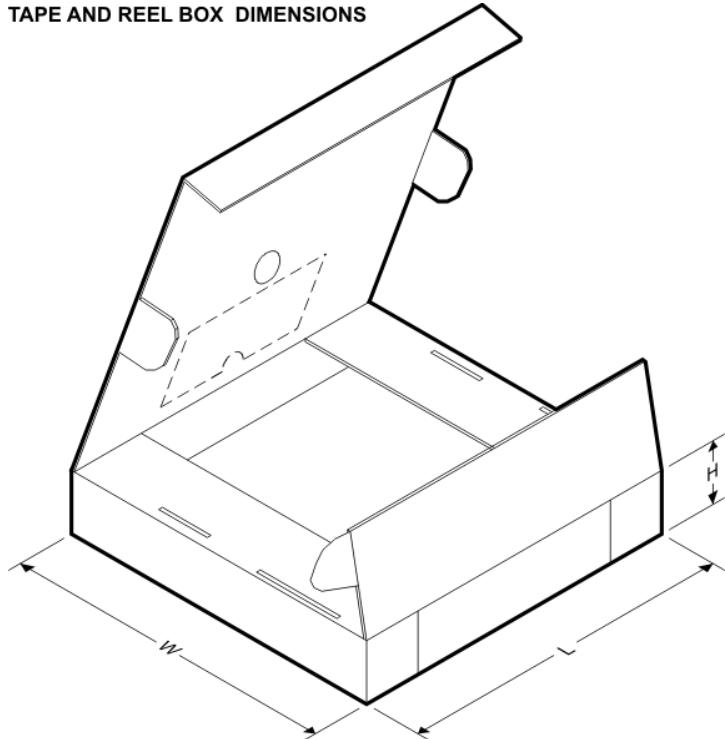
| | |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS161BDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS161BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ALS163BDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS163BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AS161NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



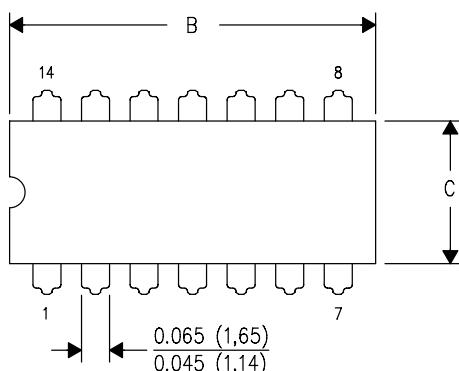
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS161BDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74ALS161BNSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74ALS163BDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74ALS163BNSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AS161NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

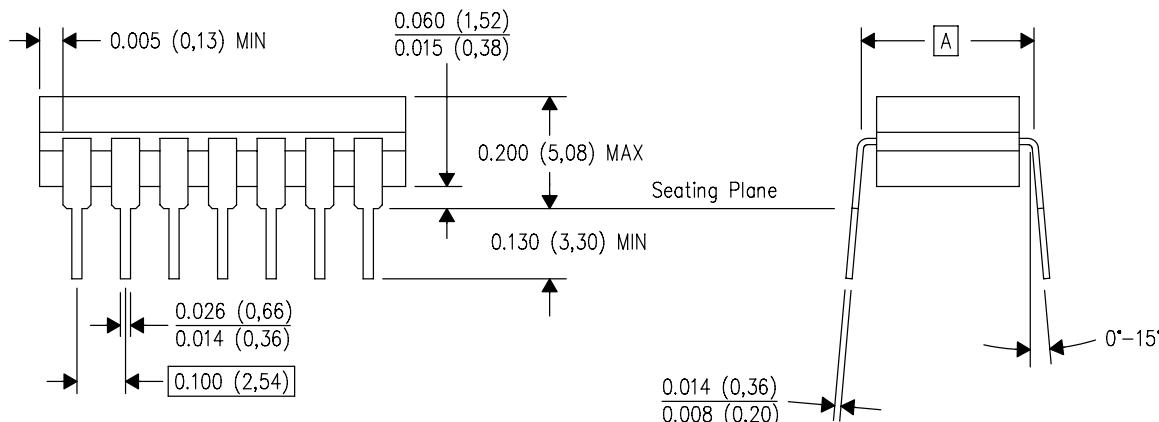
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM | PINS ** | 14 | 16 | 18 | 20 |
|-------|---------|------------------|------------------------|------------------------|------------------------|
| | | A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | | — | — | — | — |
| C MAX | | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

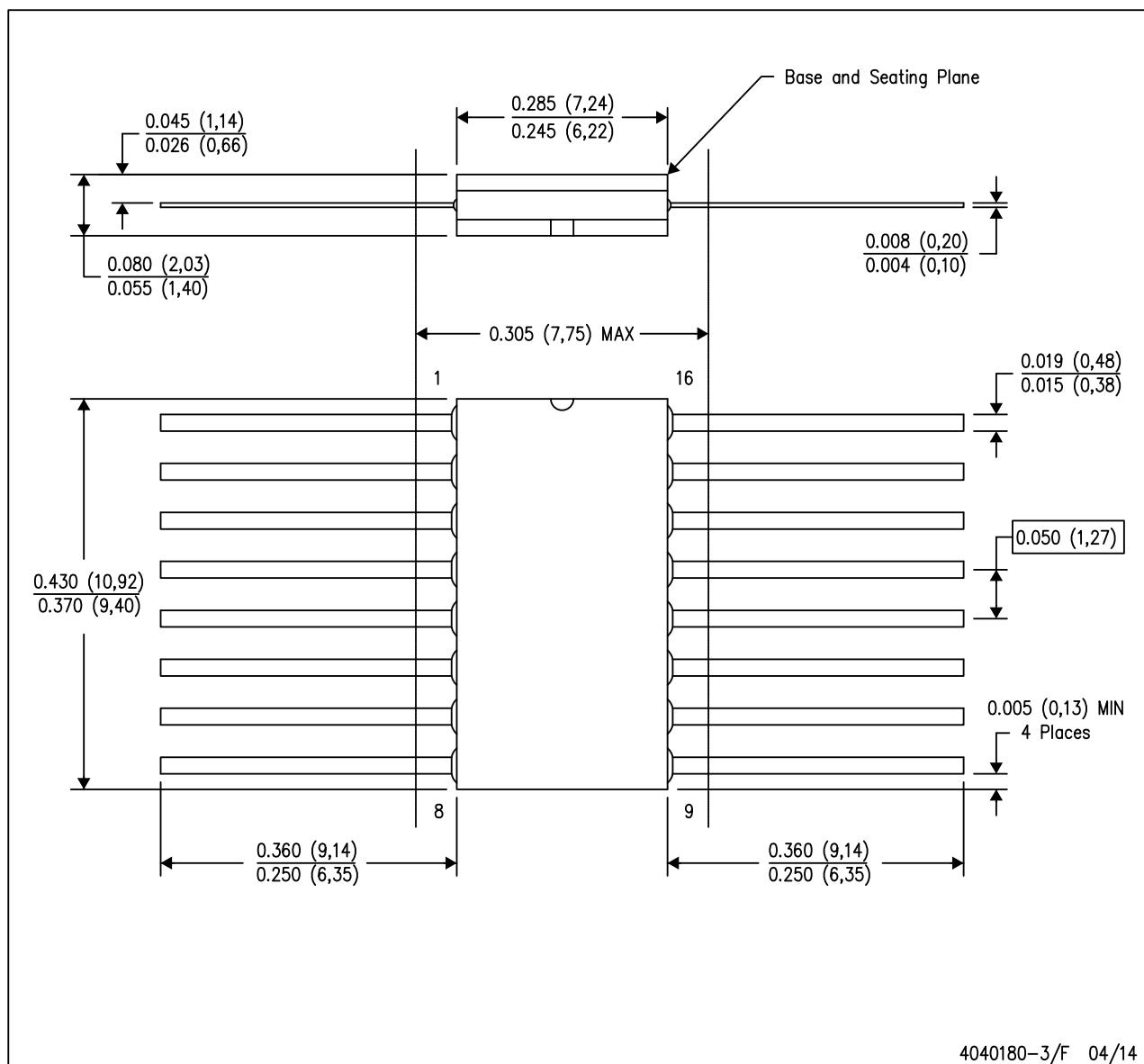
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



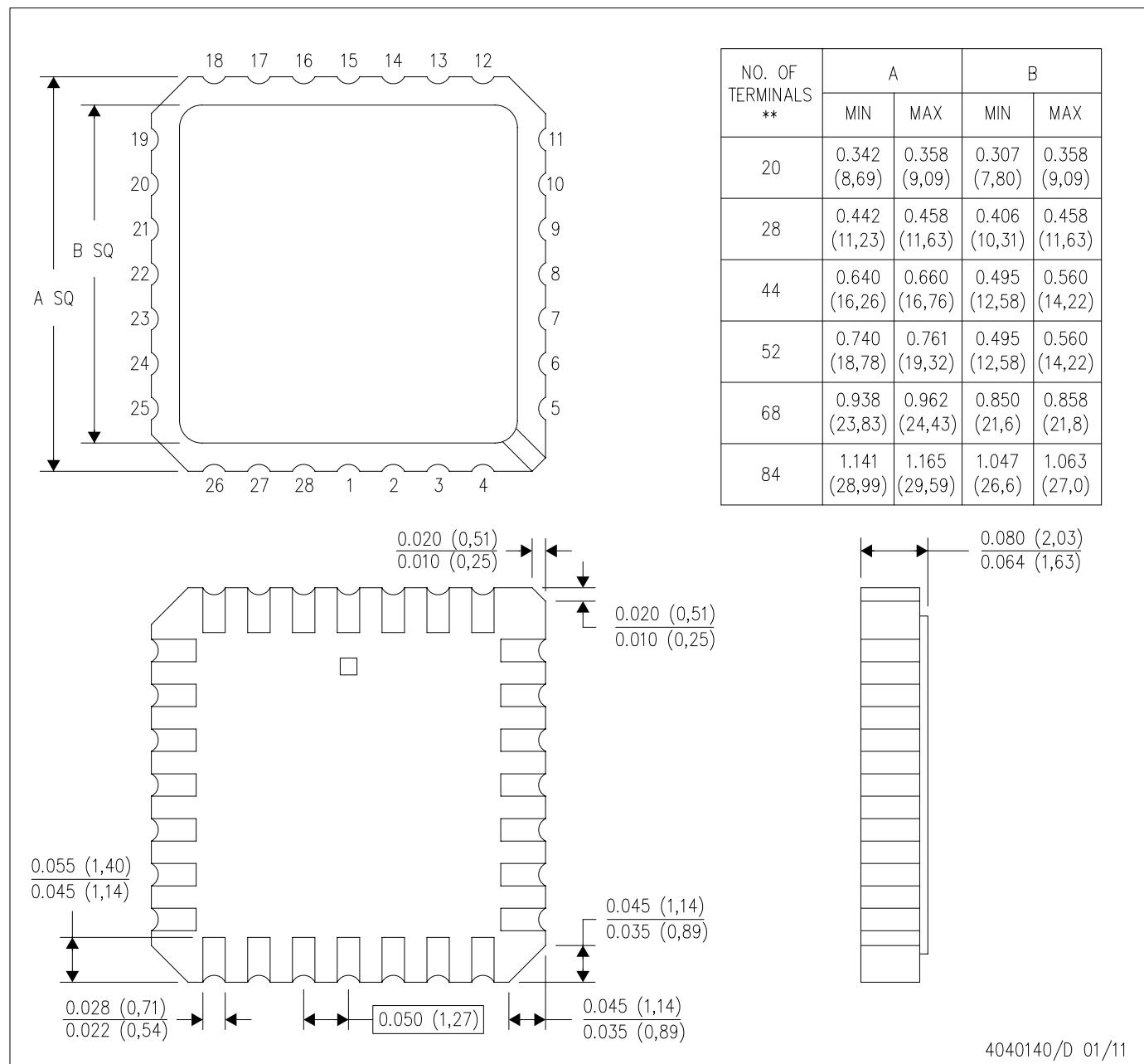
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL STD 1835 GDFP2-F16

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. Falls within JEDEC MS-004

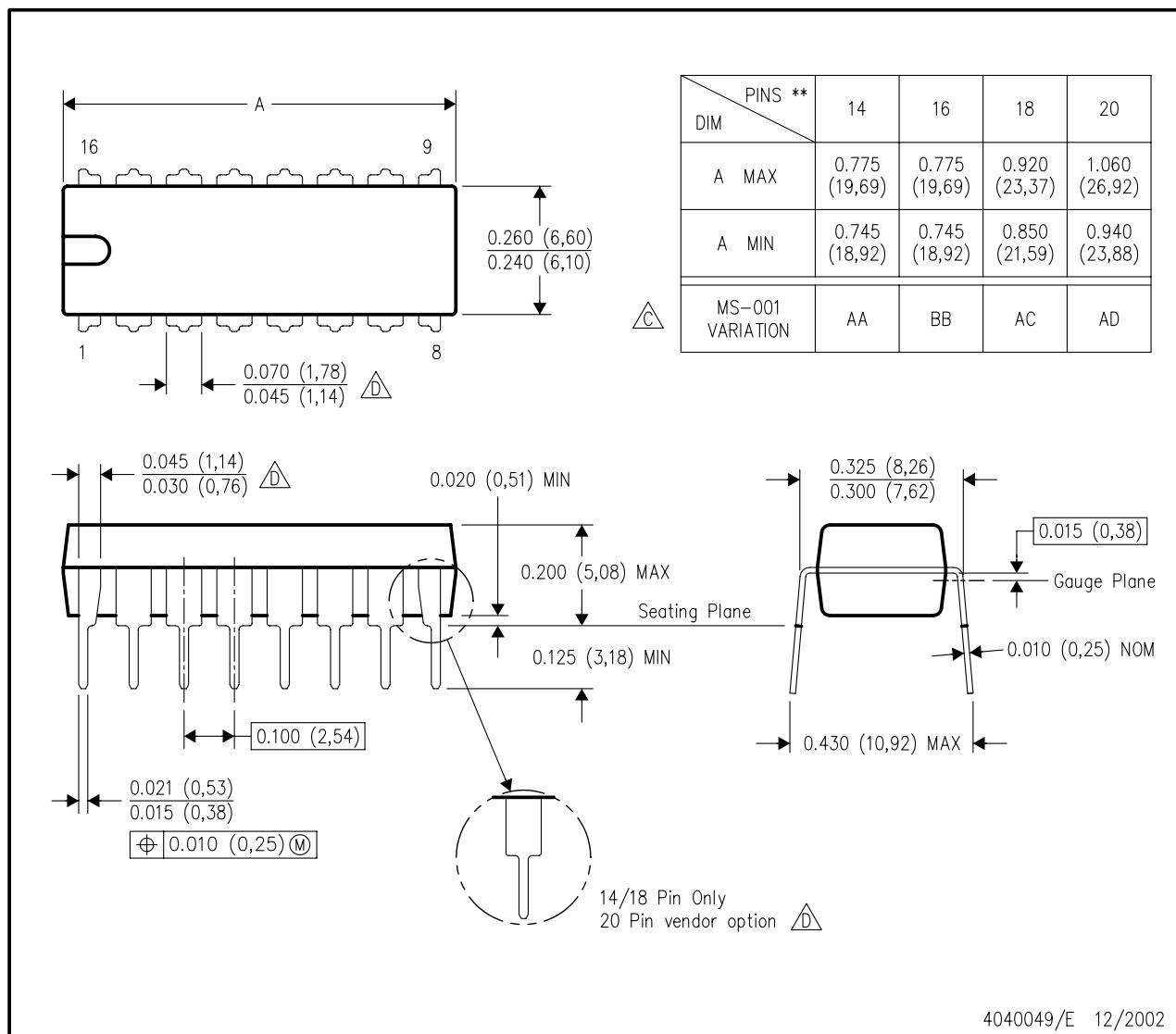
4040140/D 01/11

MECHANICAL DATA

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

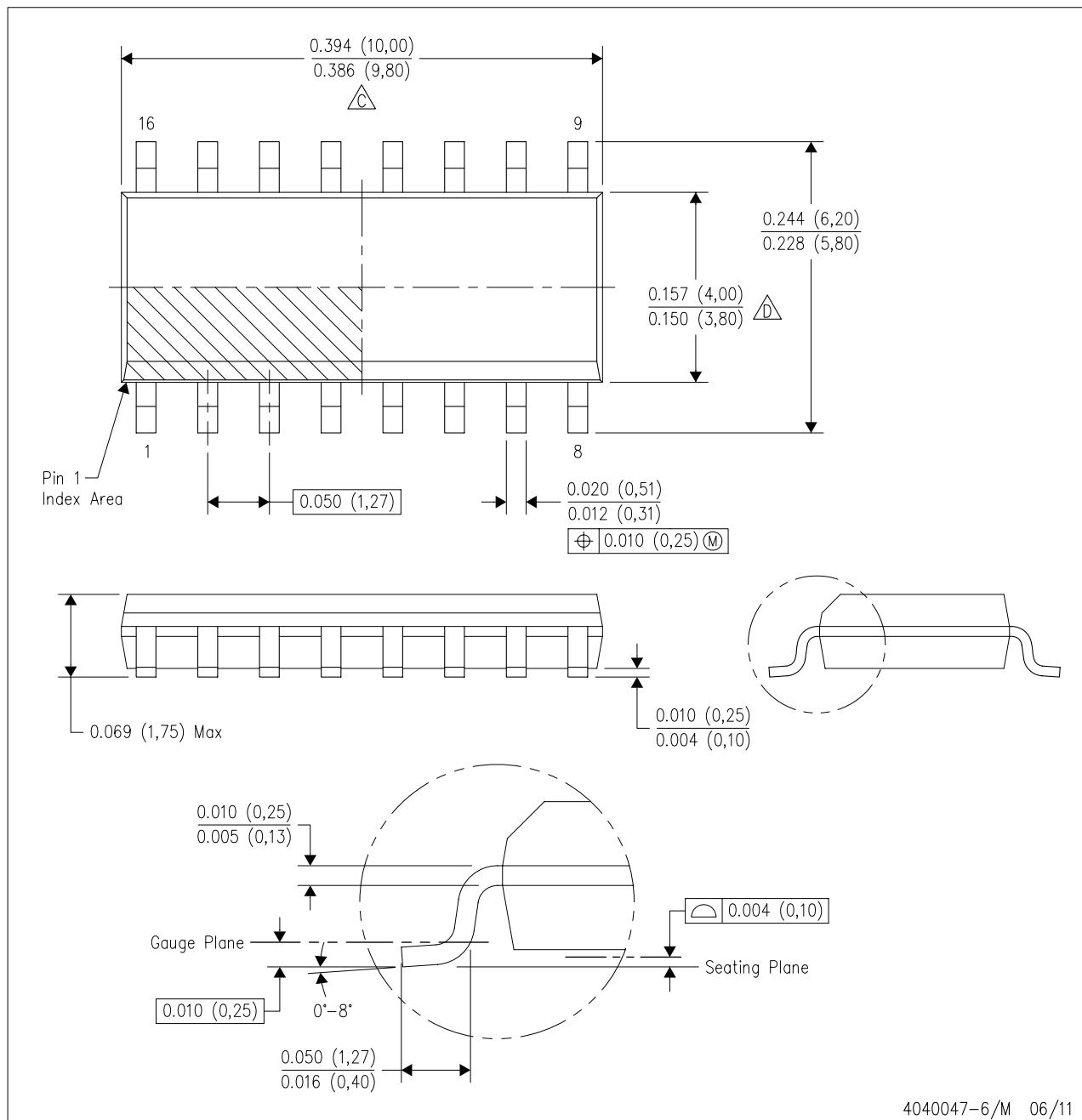
Symbol A: Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

Symbol D: The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.

△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

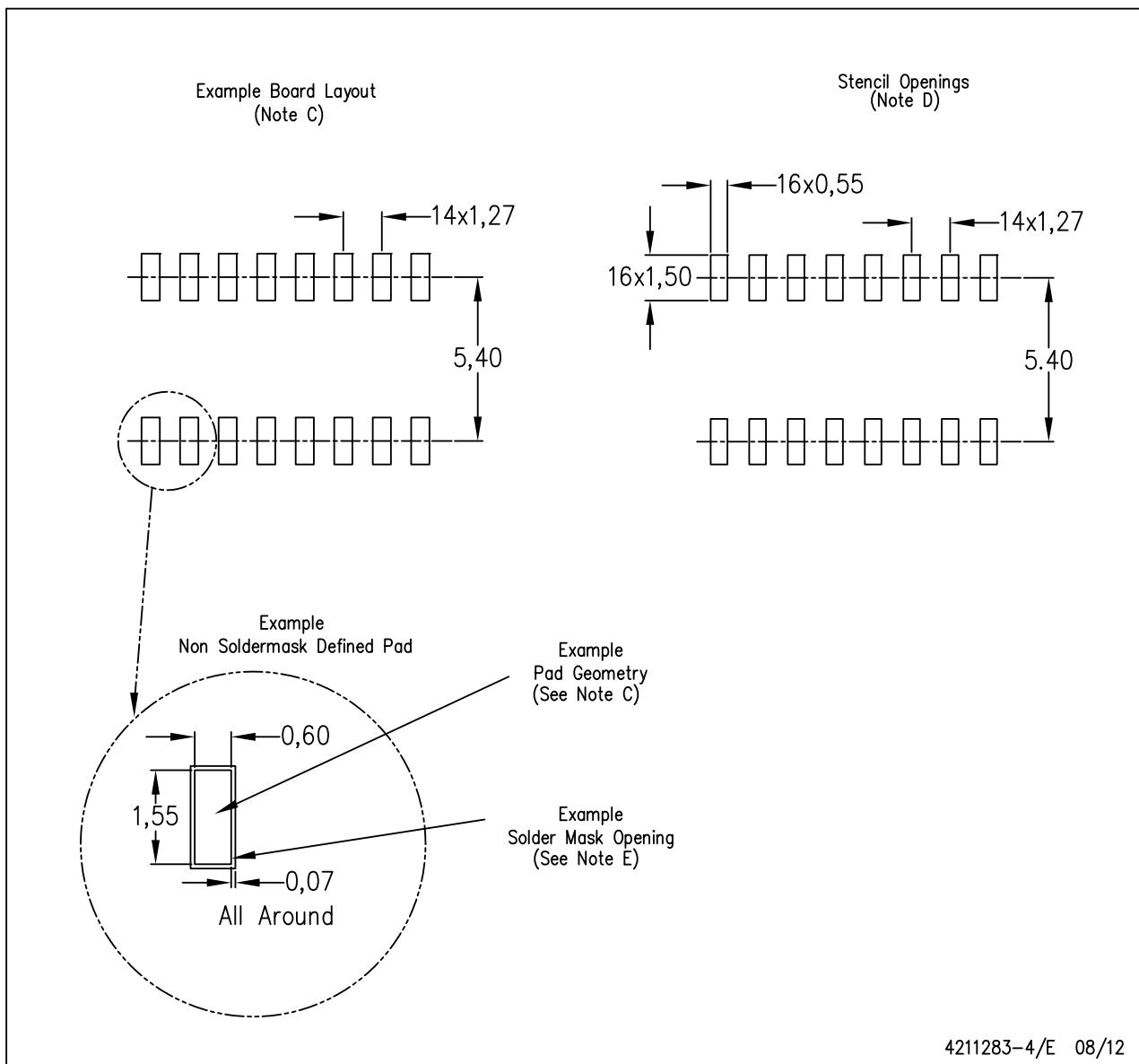
△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

LAND PATTERN DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

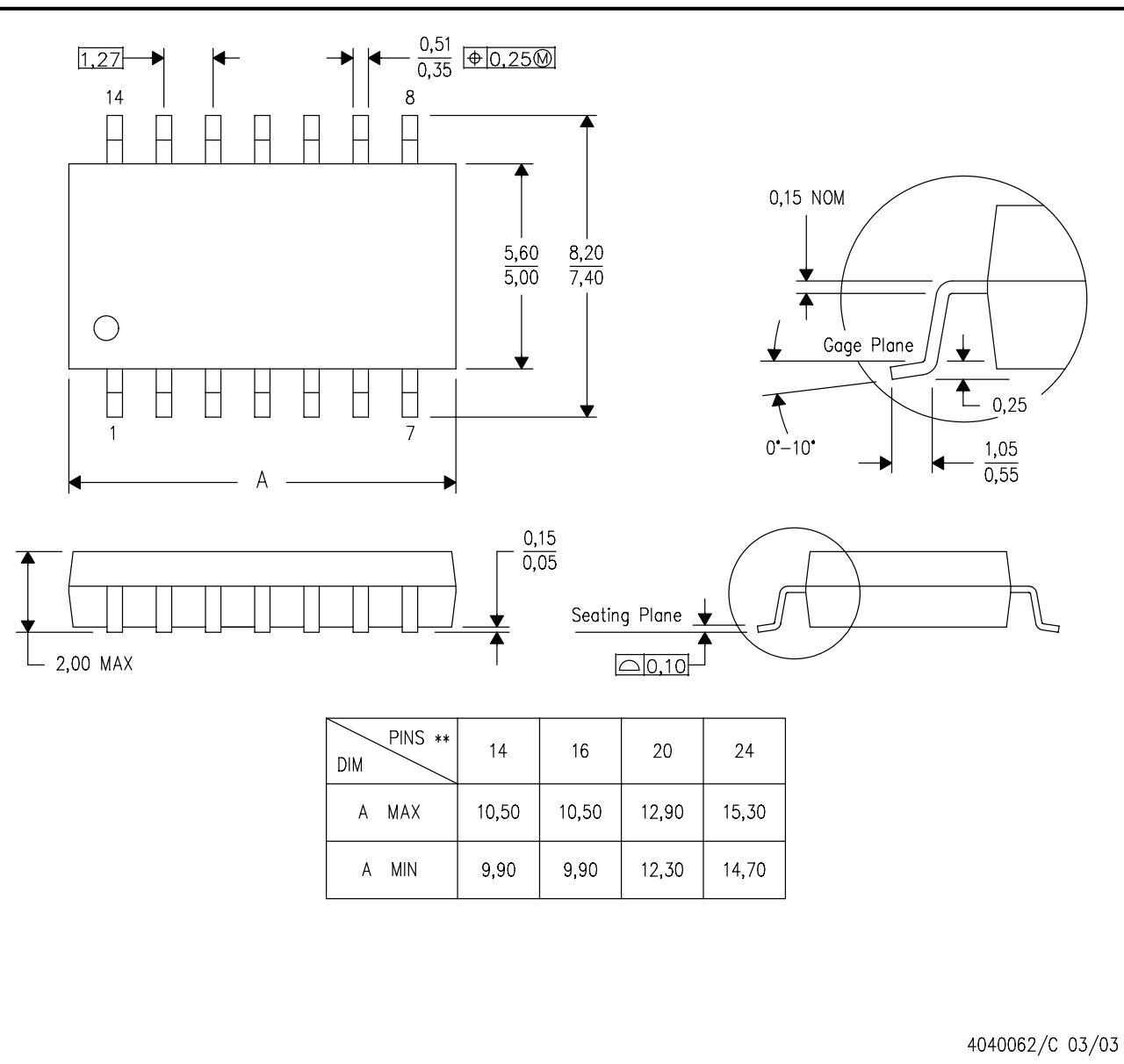
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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