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Datasheet of THS4001CD - IC OPAMP VFB 270MHZ 8SOIC

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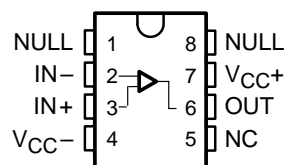
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**THS4001**  
**270-MHz HIGH-SPEED AMPLIFIER**

SLOS206A- DECEMBER 1997 - REVISED MARCH 1999

- **Very High Speed**
  - 270 MHz Bandwidth (Gain = 1, -3 dB)
  - 400 V/μsec Slew Rate
  - 40-ns Settling Time (0.1%)
- **High Output Drive, I<sub>O</sub> = 100 mA**
- **Excellent Video Performance**
  - 60 MHz Bandwidth (0.1 dB, G = 1)
  - 0.04% Differential Gain
  - 0.15° Differential Phase
- **Very Low Distortion**
  - THD = -72 dBc at f = 1 MHz
- **Wide Range of Power Supplies**  
V<sub>CC</sub> = ± 2.5 V to ± 15 V,  
I<sub>CC</sub> = 7.5 mA
- **Evaluation Module Available**

**D PACKAGE**  
**(TOP VIEW)**



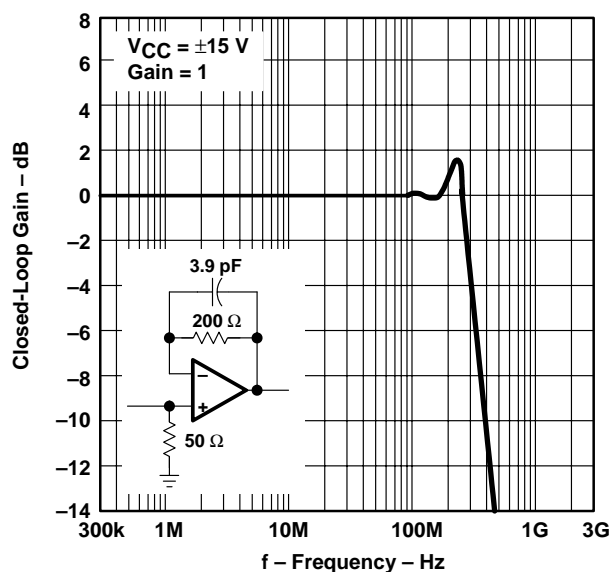
NC - No internal connection

**description**

The THS4001 is a very high-performance, voltage-feedback operational amplifier especially suited for a wide range of video applications. The device is specified to operate over a wide range of supply voltages from ± 15 V to ± 2.5 V. With a bandwidth of 270 MHz, a slew rate of over 400 V/μs, and settling times of less than 30 ns, the THS4001 offers the unique combination of high performance in an easy to use voltage feedback configuration over a wide range of power supply voltages.

The THS4001 is stable at all gains for both inverting and noninverting configurations. It has a high output drive capability of 100 mA and draws only 7.5 mA of quiescent current. Excellent professional video results can be obtained with the differential gain/phase performance of 0.04%/0.15° and 0.1 dB gain flatness to 60 MHz. For applications requiring low distortion, the THS4001 is ideally suited with total harmonic distortion of -72 dBc at f = 1 MHz.

**CLOSED-LOOP GAIN**  
**vs**  
**FREQUENCY**



**HIGH-SPEED AMPLIFIER FAMILY**

DEVICE	ARCH.		SUPPLY VOLTAGE			BW (MHz)	SR (V/μs)	THD f = 1 MHz (dB)	t <sub>s</sub> 0.1% (ns)	DIFF. GAIN	DIFF. PHASE	V <sub>n</sub> (nV/√Hz)
	VFB	CFB	5 V	±5 V	±15 V							
THS3001		•		•	•	420	6500	-96	40	0.01%	0.02°	1.6
THS4001	•		•	•	•	270	400	-72	40	0.04%	0.15°	12.5
THS4031/32	•			•	•	100	100	-72	60	0.02%	0.03°	1.6
THS4061/62	•			•	•	180	400	-72	40	0.02%	0.02°	14.5



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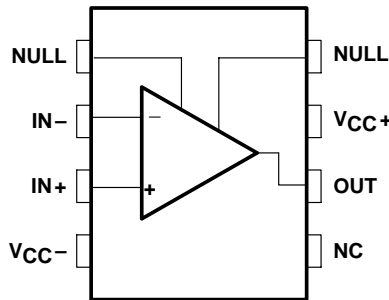
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**AVAILABLE OPTIONS**

T <sub>A</sub>	PACKAGED DEVICES	
	SMALL OUTLINE† (D)	EVALUATION MODULE
0°C to 70°C	THS4001CD	THS4001EVM
-40°C to 85°C	THS4001ID	—

† The D packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4001CDR).

**symbol**



**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage, V <sub>CC-</sub> to V <sub>CC+</sub>	33 V
Input voltage, V <sub>I</sub>	±V <sub>CC</sub>
Output current, I <sub>O</sub>	175 mA
Differential input voltage, V <sub>ID</sub>	±4 V
Continuous total power dissipation	See Dissipation Ratings Table
Operating free air temperature, T <sub>A</sub> : C suffix	0°C to 70 °C
I suffix	-40°C to 85 °C
Storage temperature, T <sub>stg</sub>	-65°C to 150 °C
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
D	740 mW	6 mW/°C	475 mW	385 mW



**CAUTION:** The THS4001 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality

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**recommended operating conditions**

		MIN	TYP	MAX	UNIT
Supply voltage, $V_{CC}$	Dual supply	$\pm 2.5$		$\pm 16$	V
	Single supply	5		32	
Quiescent current, $I_{CC}$	$\pm 15$ V		7.8	9.5	mA
	$\pm 5$ V, $\pm 2.5$ V		6.7	8	
Operating free-air temperature, $T_A$	C suffix	0		70	$^{\circ}$ C
	I suffix	-40		85	

**electrical characteristics,  $V_{CC} = \pm 15$  V,  $R_L = 150 \Omega$ ,  $T_A = 25^{\circ}$ C (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
Differential gain error	Gain = 2, $R_L = 150 \Omega$ , $f = 3.58$ MHz	$\pm 15$ V		0.04%		
		$\pm 5$ V		0.01%		
Differential phase error		$\pm 15$ V		0.15 $^{\circ}$		
		$\pm 5$ V		0.08 $^{\circ}$		
$V_{IO}$ Input offset voltage	$T_A = 25^{\circ}$ C	$\pm 15$ V,		2	8	mV
	$T_A = \text{full range}$	$\pm 5$ V			10	
$I_{IB}$ Input bias current	$T_A = 25^{\circ}$ C	$\pm 15$ V,		2.6	5	$\mu$ A
	$T_A = \text{full range}$	$\pm 5$ V			6	
$I_{OS}$ Input offset current	$T_A = 25^{\circ}$ C	$\pm 15$ V,		35	200	nA
	$T_A = \text{full range}$	$\pm 5$ V			500	
Open-loop gain	$V_O = \pm 10$ V, $R_L = 1$ k $\Omega$	$T_A = 25^{\circ}$ C	$\pm 15$ V	5	10	V/mV
		$T_A = \text{full range}$		3		
	$V_O = \pm 2.5$ V, $R_L = 500 \Omega$	$T_A = 25^{\circ}$ C	$\pm 5$ V	3	6	
		$T_A = \text{full range}$		2		
CMRR Common-mode rejection ratio	$V_{(CM)} = \pm 12$ V	$T_A = 25^{\circ}$ C	$\pm 15$ V	85	100	dB
		$T_A = \text{full range}$		75		
PSRR Power supply rejection ratio	$T_A = 25^{\circ}$ C	$\pm 15$ V,	75	85	dB	
	$T_A = \text{full range}$	$\pm 5$ V	70			
$V_{ICR}$ Common-mode input voltage range		$\pm 15$ V	13.5 to -13	14.8 to -14	V	
		$\pm 5$ V	3.6 to -2.7	4.4 to -3.6		
$V_O$ Output voltage swing	$R_L = 500 \Omega$	$\pm 15$ V	$\pm 13$	$\pm 13.5$	V	
		$\pm 5$ V	$\pm 3.3$	$\pm 3.8$		
		$\pm 2.5$ V	$\pm 0.8$	$\pm 1.3$		
$I_O$ Output current	Gain = 2, $R_L = 20 \Omega$	$\pm 15$ V	50	100	mA	
		$\pm 5$ V	50	100		
		$\pm 2.5$ V	50	100		
THD Total harmonic distortion	$V_I = 1$ V(pp), $f = 1$ MHz	$\pm 15$ V		-72	dBc	
$R_I$ Input resistance				10	M $\Omega$	
$C_I$ Input capacitance				1.5	pF	
$R_O$ Output resistance	Open loop			10	$\Omega$	

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operating characteristics,  $V_{CC} = \pm 15\text{ V}$ ,  $R_L = 150\ \Omega$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
Slew rate	Gain = -1	$\pm 15\text{ V}$		400		V/ $\mu\text{s}$
		$\pm 5\text{ V}$		400		
		$\pm 2.5\text{ V}$		350		
Settling time to 0.1%	10 V step (0 to 10 V), Gain = -1	$\pm 15\text{ V}$		40		ns
	-2.5 V to 2.5 V step, Gain = -1	$\pm 5\text{ V}$		30		
-3 dB Bandwidth	Gain = +1, $R_f = 150\ \Omega$	$\pm 15\text{ V}$		270		MHz
		$\pm 5\text{ V}$		220		
		$\pm 2.5\text{ V}$		180		
	Gain = -1, $R_f = 150\ \Omega$	$\pm 15\text{ V}$		80		MHz
		$\pm 5\text{ V}$		75		
		$\pm 2.5\text{ V}$		70		
Bandwidth for 0.1 dB flatness	Gain = +1	$\pm 15\text{ V}$		60		MHz
		$\pm 5\text{ V}$		50		
		$\pm 2.5\text{ V}$		40		
$V_n$	Equivalent input noise voltage	f = 10 kHz	$\pm 15\text{ V}$ , $\pm 5\text{ V}$	12.5		nV/ $\sqrt{\text{Hz}}$
$I_n$	Equivalent input noise current	f = 10 kHz	$\pm 15\text{ V}$ , $\pm 5\text{ V}$	1.5		pA/ $\sqrt{\text{Hz}}$

### TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE	
$I_{IB}$	Input bias current	vs Free-air temperature	1
$V_{IO}$	Input offset voltage	vs Free-air temperature	2
	Open-loop gain	vs Frequency	3
	Phase	vs Frequency	3
	Differential gain	vs DC voltage	4, 5
	Differential phase	vs DC voltage	4, 5
	Closed-loop gain	vs Frequency	6, 7
CMRR	Common-mode rejection ratio	vs Frequency	8
PSRR	Power-supply rejection ratio	vs Frequency	9
		vs Free-air temperature	10
$V_{O(PP)}$	Output voltage swing	vs Supply voltage	11
		vs Load resistance	12
	Bandwidth (-3 dB)	vs Feedback resistance	13, 14
$I_{CC}$	Supply current	vs Supply voltage	15
		vs Free-air temperature	16
$E_{NV}$	Noise spectral density	vs Frequency	17
THD	Total harmonic distortion	vs Frequency	18

**TYPICAL CHARACTERISTICS**

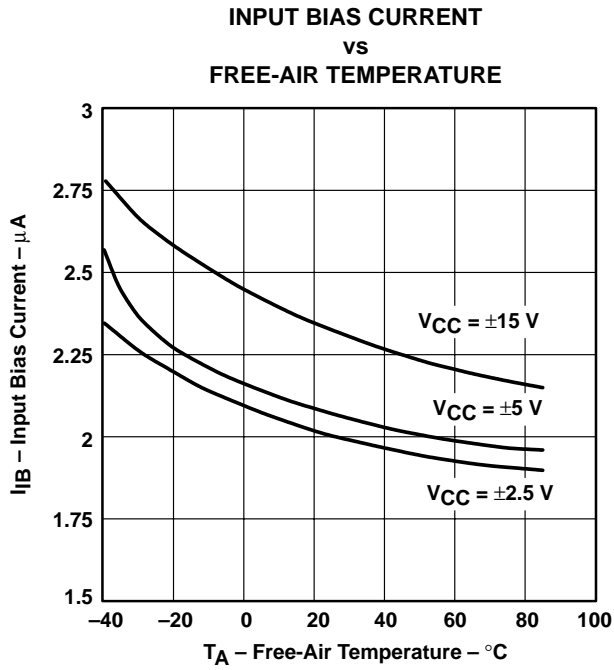


Figure 1

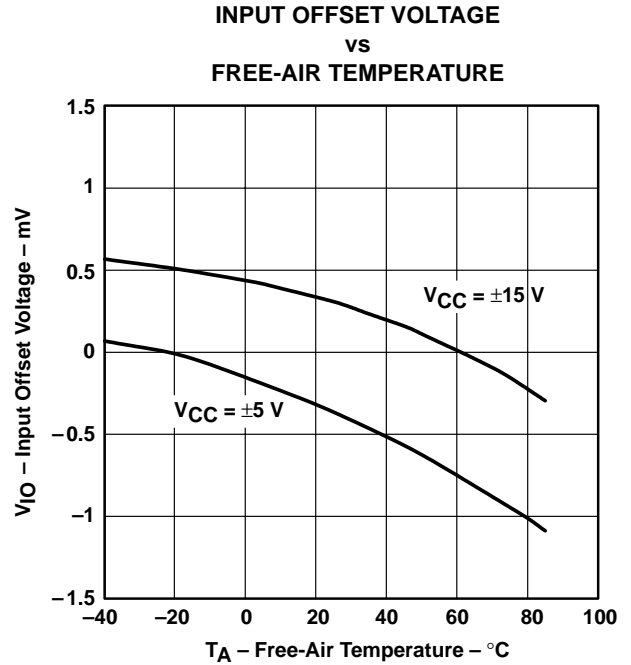


Figure 2

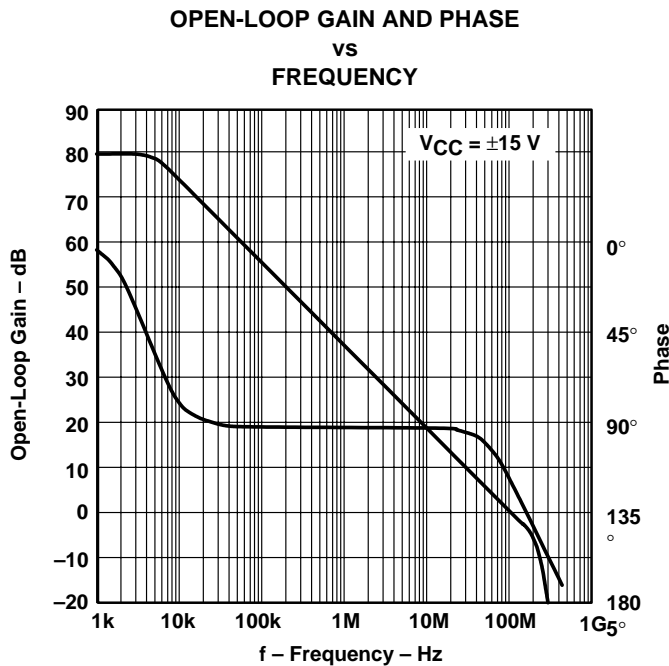


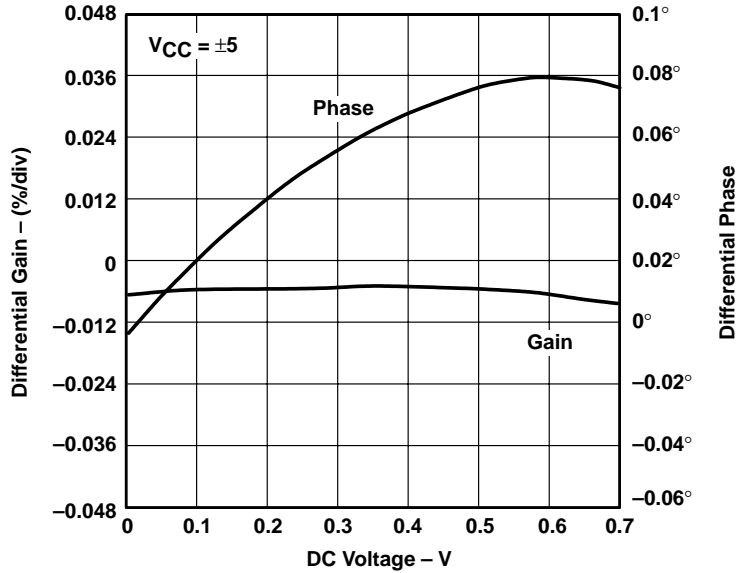
Figure 3

**THS4001**  
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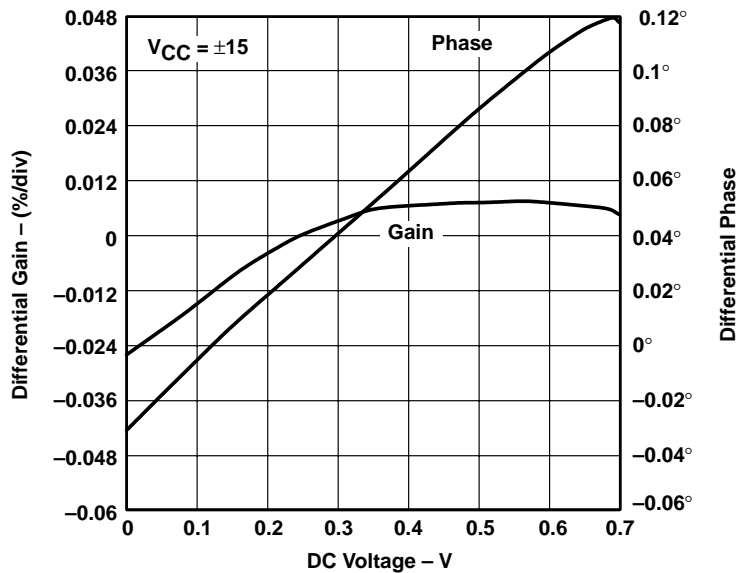
**TYPICAL CHARACTERISTICS**

**DIFFERENTIAL GAIN AND  
 DIFFERENTIAL PHASE  
 vs  
 DC VOLTAGE**



**Figure 4**

**DIFFERENTIAL GAIN AND  
 DIFFERENTIAL PHASE  
 vs  
 DC VOLTAGE**



**Figure 5**

**TYPICAL CHARACTERISTICS**

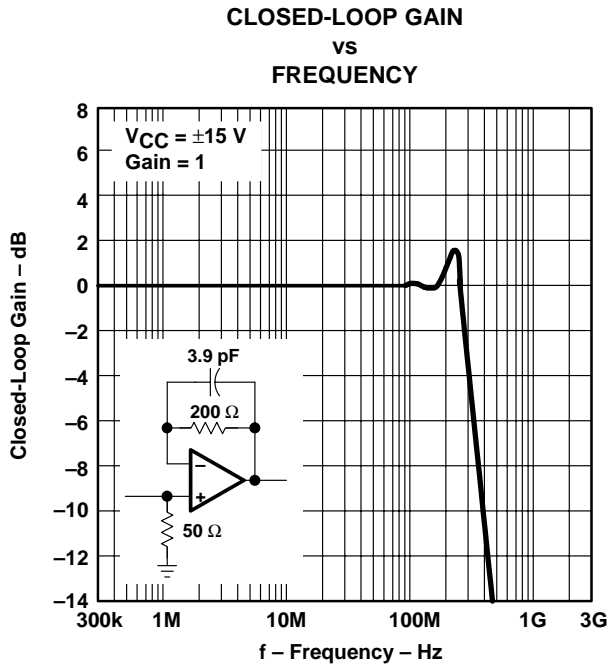


Figure 6

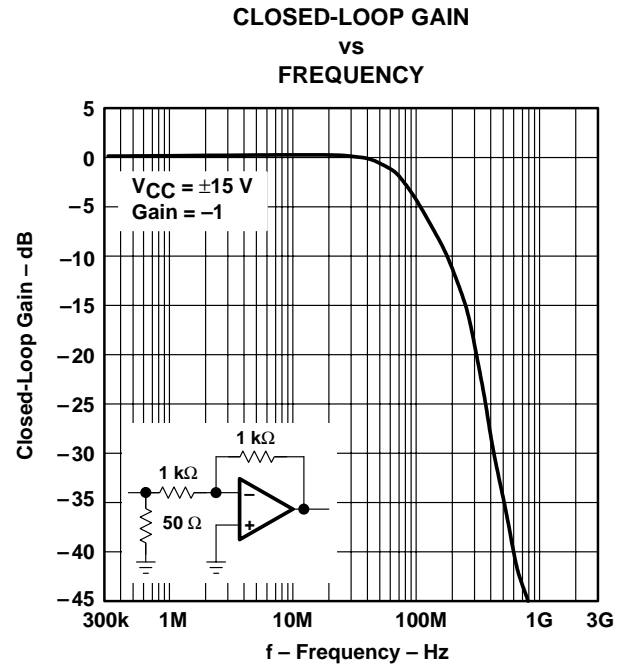


Figure 7

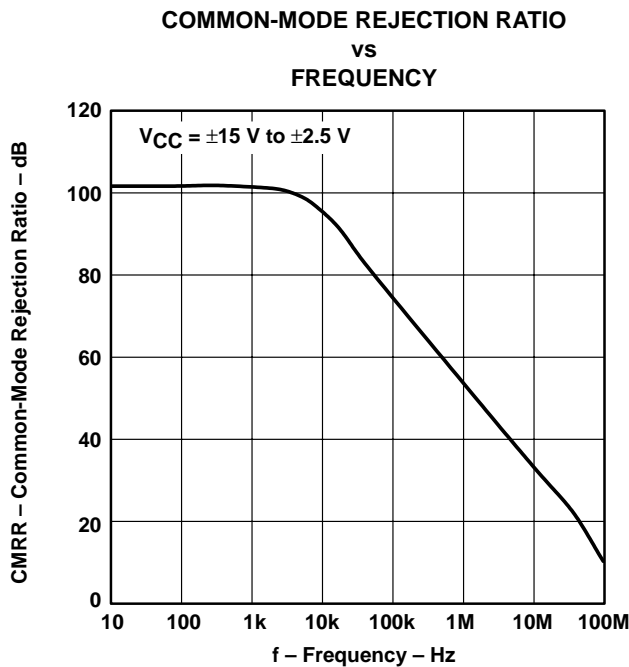


Figure 8

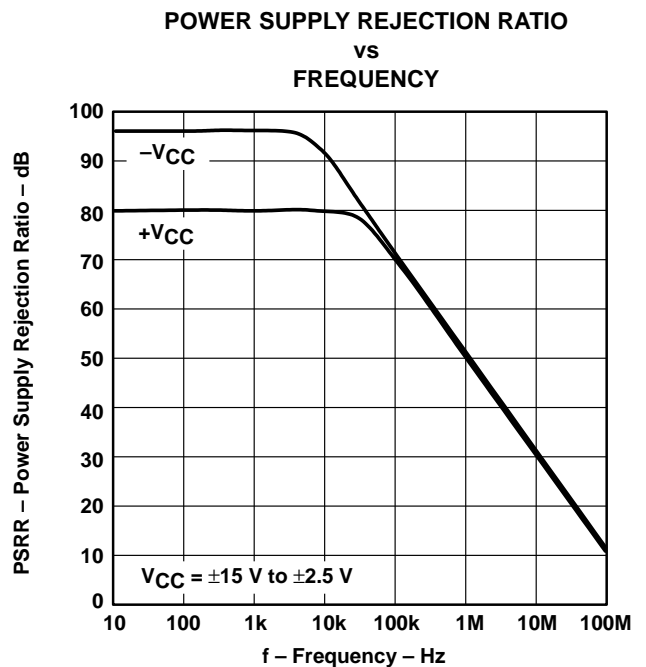


Figure 9

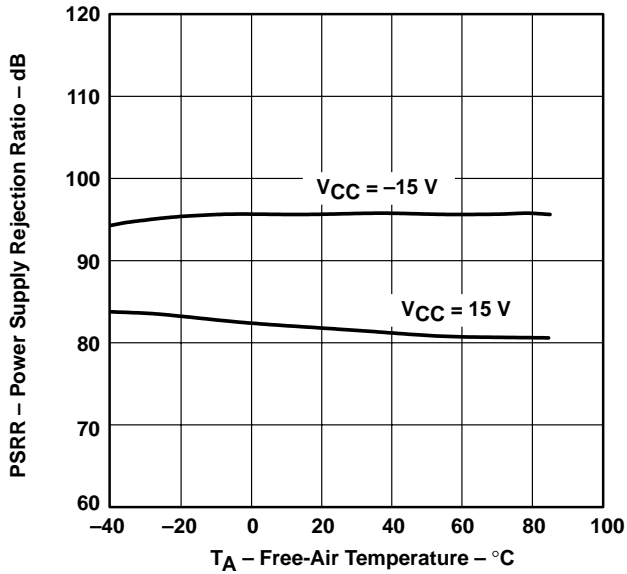


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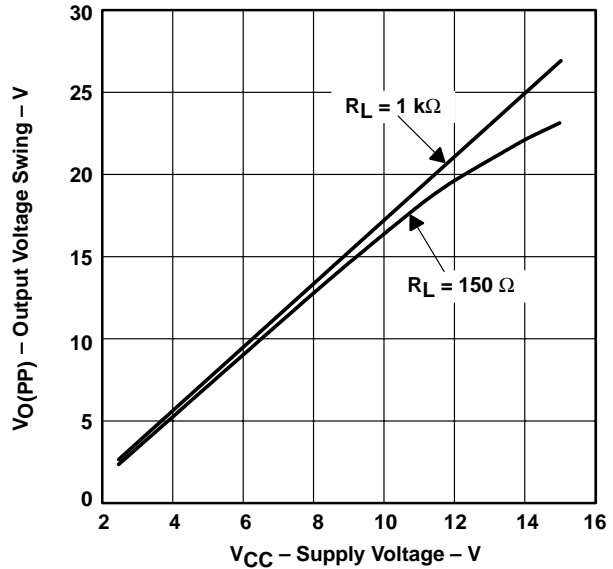
**TYPICAL CHARACTERISTICS**

**POWER SUPPLY REJECTION RATIO  
 VS  
 FREE-AIR TEMPERATURE**



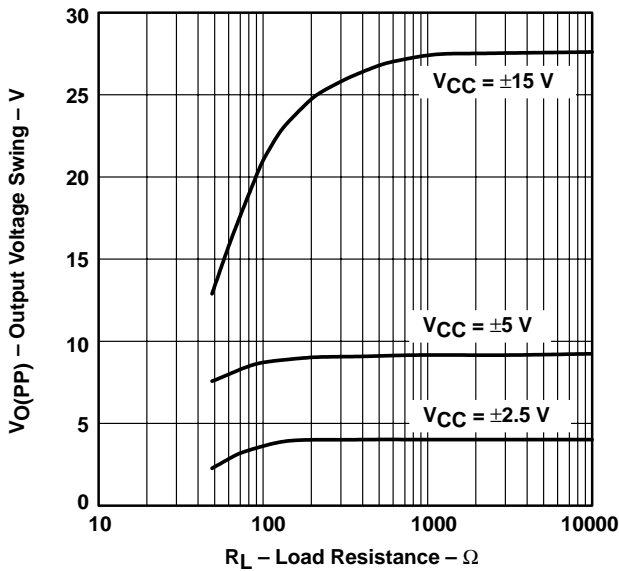
**Figure 10**

**OUTPUT VOLTAGE SWING  
 VS  
 SUPPLY VOLTAGE**



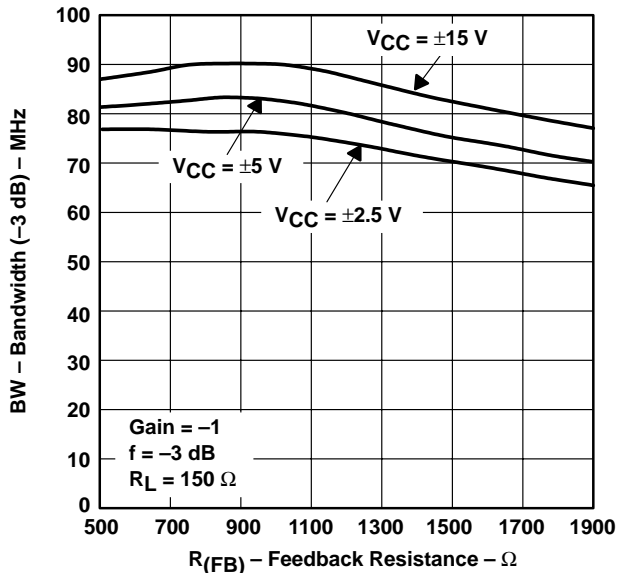
**Figure 11**

**OUTPUT VOLTAGE SWING  
 VS  
 LOAD RESISTANCE**



**Figure 12**

**BANDWIDTH (-3 dB)  
 VS  
 FEEDBACK RESISTANCE**



**Figure 13**

**TYPICAL CHARACTERISTICS**

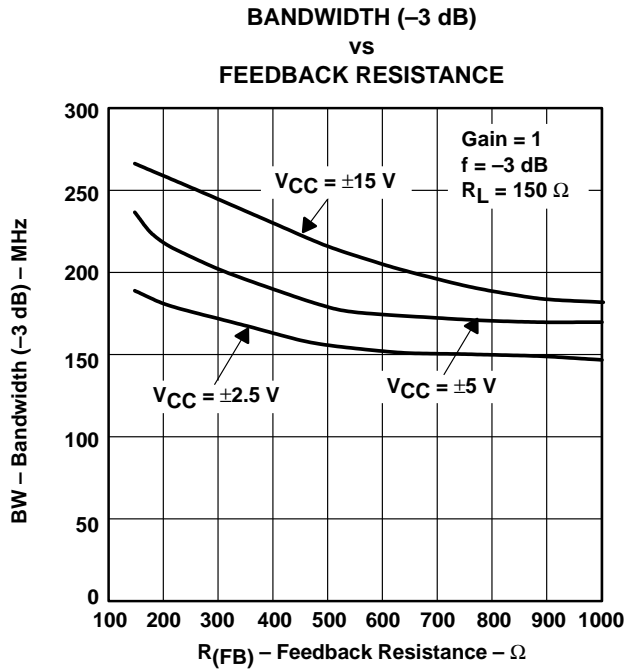


Figure 14

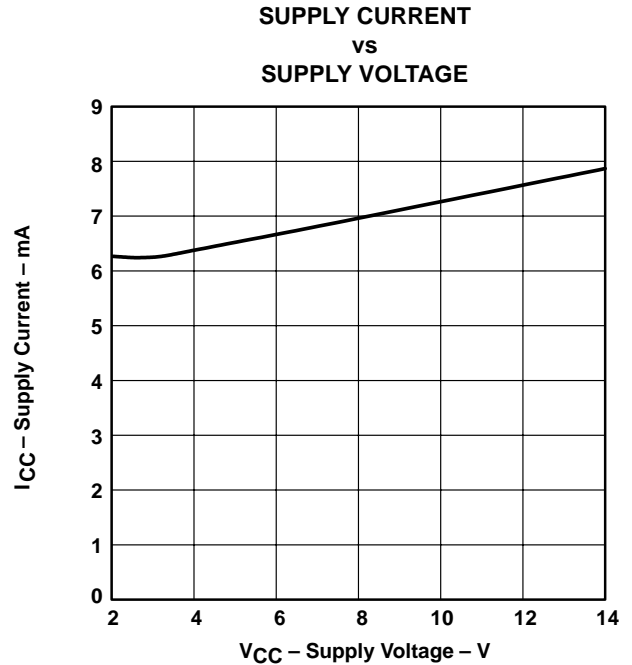


Figure 15

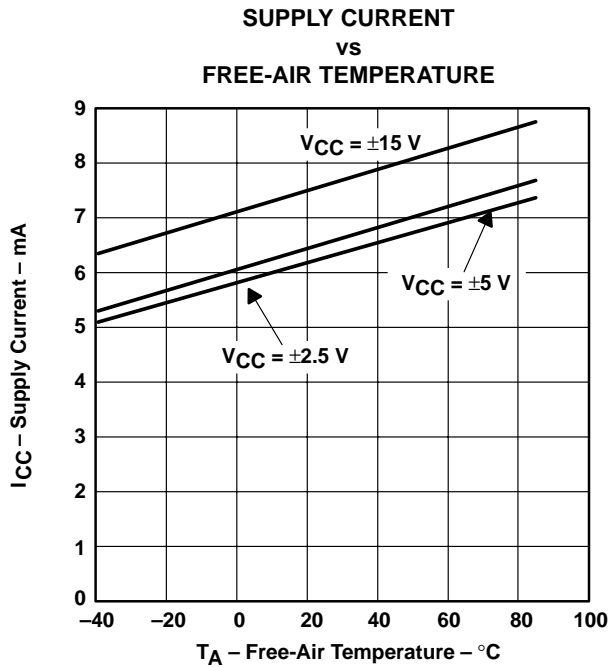


Figure 16

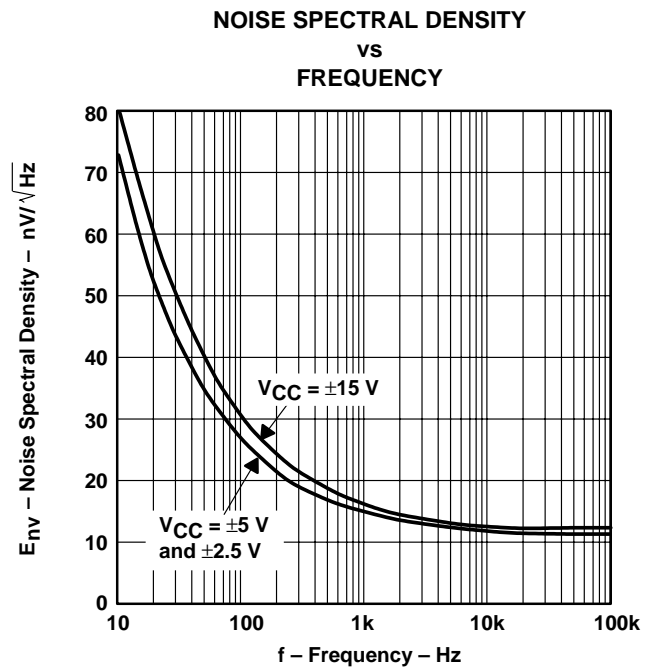


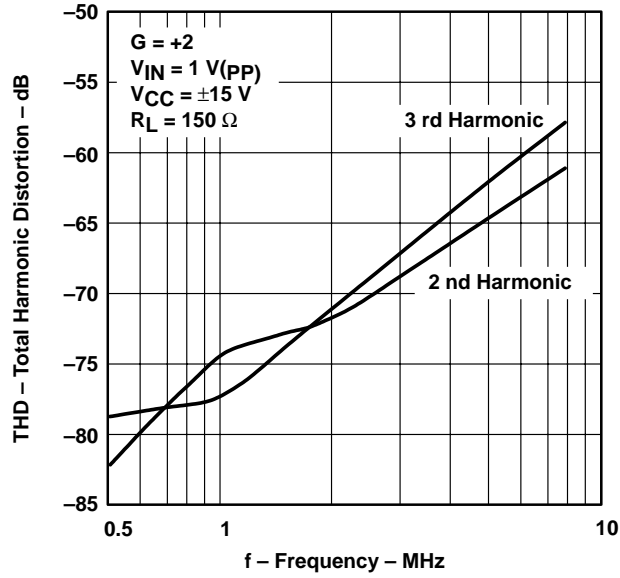
Figure 17

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**TYPICAL CHARACTERISTICS**

**TOTAL HARMONIC DISTORTION  
 vs  
 FREQUENCY**



**Figure 18**

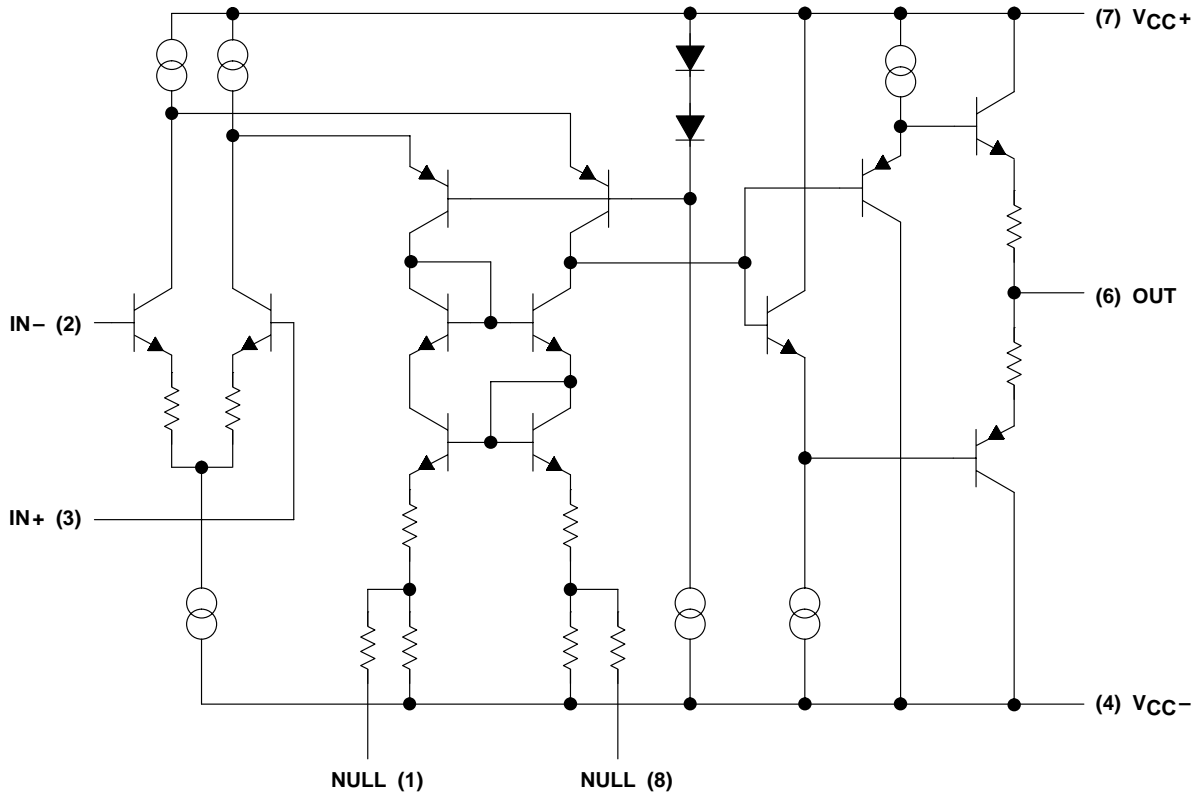
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**APPLICATION INFORMATION**

**theory of operation**

The THS4001 is a high speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing  $f_T$ s of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 19.



**Figure 19. THS4001 Simplified Schematic**

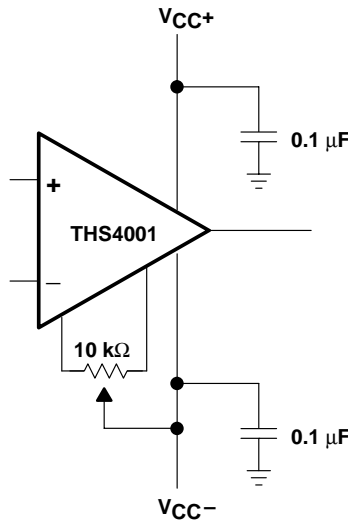
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**APPLICATION INFORMATION**

**offset nulling**

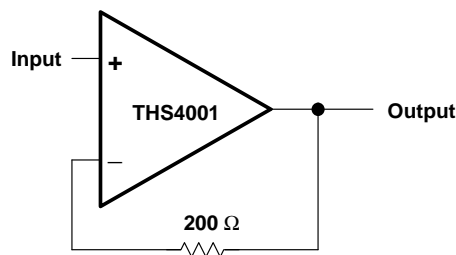
The THS4001 has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided. By placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply, the input offset can be adjusted. This is shown in Figure 20.



**Figure 20. Offset Nulling Schematic**

**optimizing unity gain response**

Internal frequency compensation of the THS4001 was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the  $G=+1$  configuration. For optimum settling time and minimum ringing, a feedback resistor of  $200\ \Omega$  should be used as shown in Figure 21. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.



**Figure 21. Noninverting, Unity Gain Schematic**

## APPLICATION INFORMATION

### driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS4001 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 22. A minimum value of 20  $\Omega$  should work well for most applications. For example, in 75- $\Omega$  transmission systems, setting the series resistor value to 75  $\Omega$  both isolates any capacitance loading and provides the proper line impedance matching at the source end.

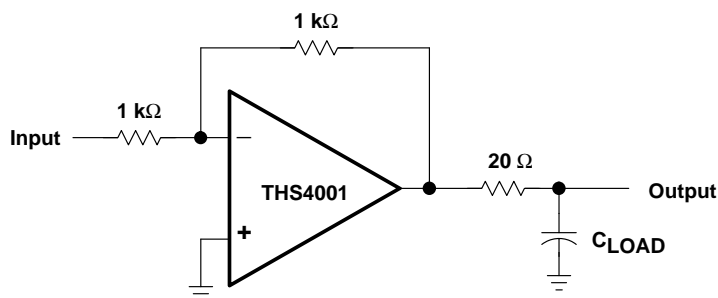


Figure 22. Driving a Capacitive Load

### circuit layout considerations

In order to achieve the levels of high frequency performance of the THS4001, it is essential that proper printed-circuit board high frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS4001 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8- $\mu$ F tantalum capacitor in parallel with a 0.1- $\mu$ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- $\mu$ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- $\mu$ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high speed op amps. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

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**APPLICATION INFORMATION**

**circuit layout considerations (continued)**

- Surface-mount passive components – Using surface mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

**evaluation board**

An evaluation board is available for the THS4001 (literature number SLOP119). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 23. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. To order the evaluation board contact your local TI sales office or distributor. For more detailed information, refer to the *THS4001 EVM User's Manual* (literature number SLOU017).

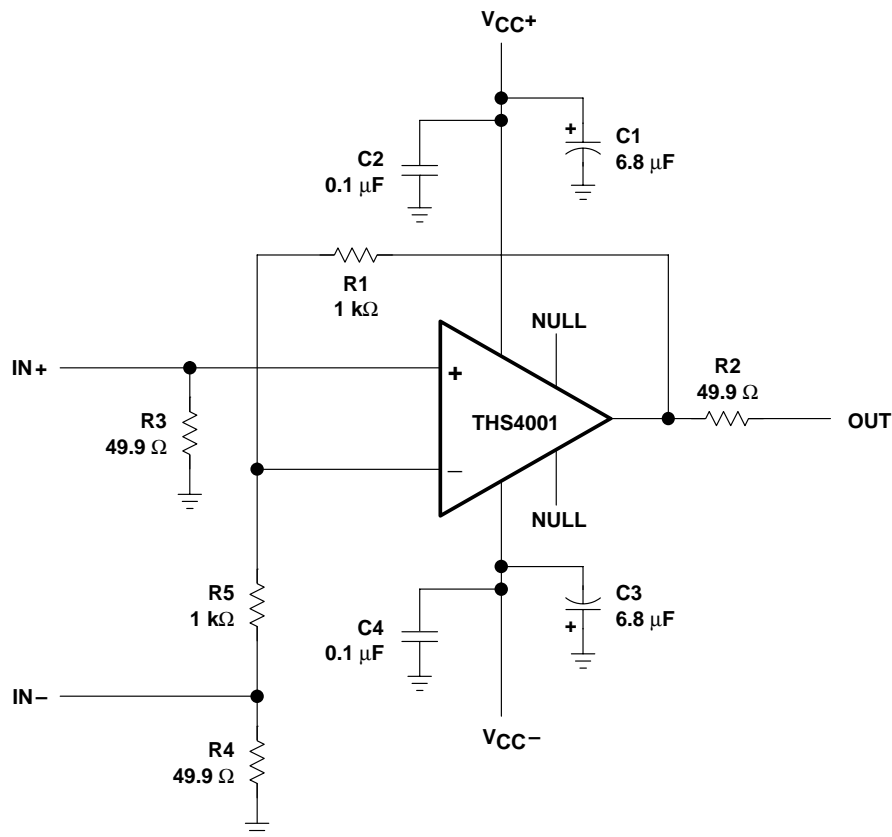


Figure 23.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4001CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4001C	<a href="#">Samples</a>
THS4001CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4001C	<a href="#">Samples</a>
THS4001CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4001C	<a href="#">Samples</a>
THS4001ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4001I	<a href="#">Samples</a>
THS4001IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4001I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.





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10-Jun-2014

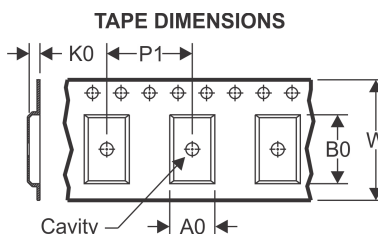
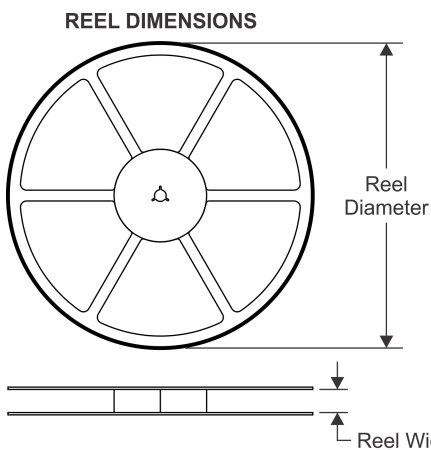
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<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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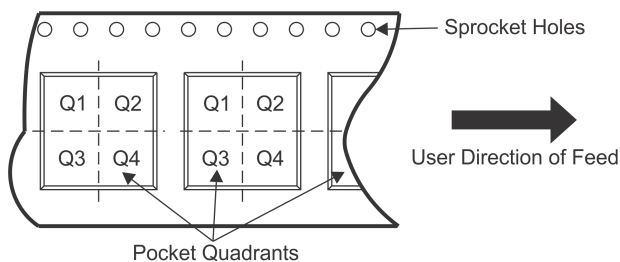
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**TAPE AND REEL INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

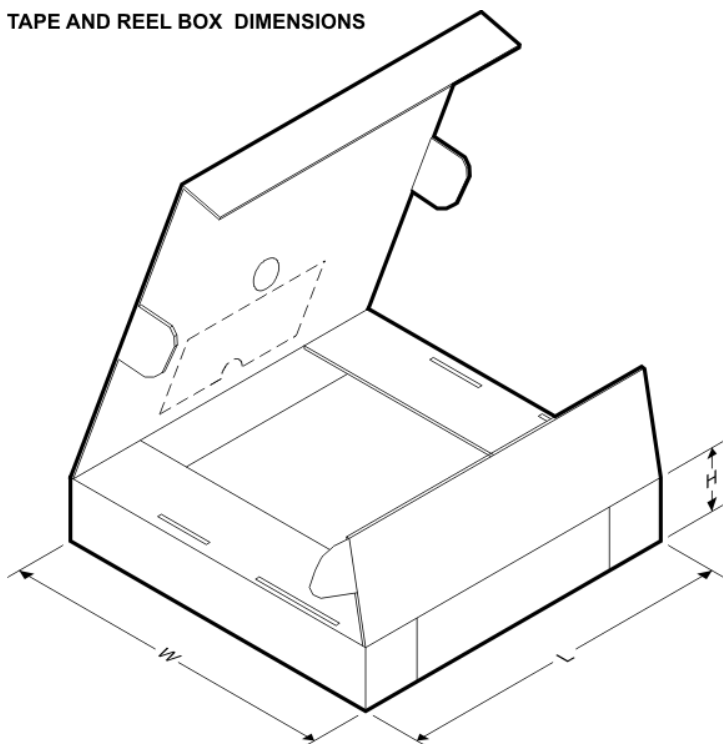
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4001CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



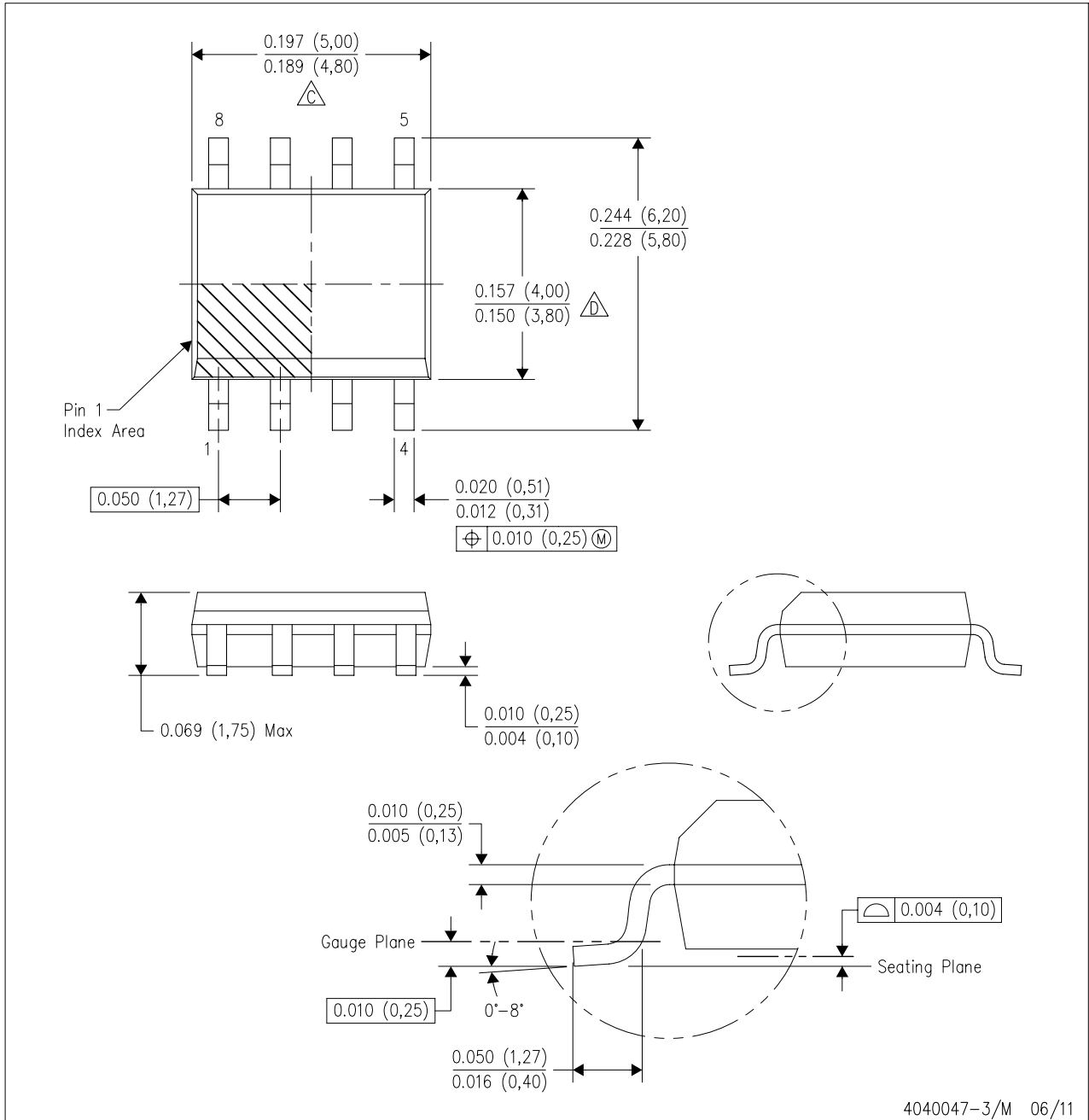
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4001CDR	SOIC	D	8	2500	367.0	367.0	38.0

**MECHANICAL DATA**

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



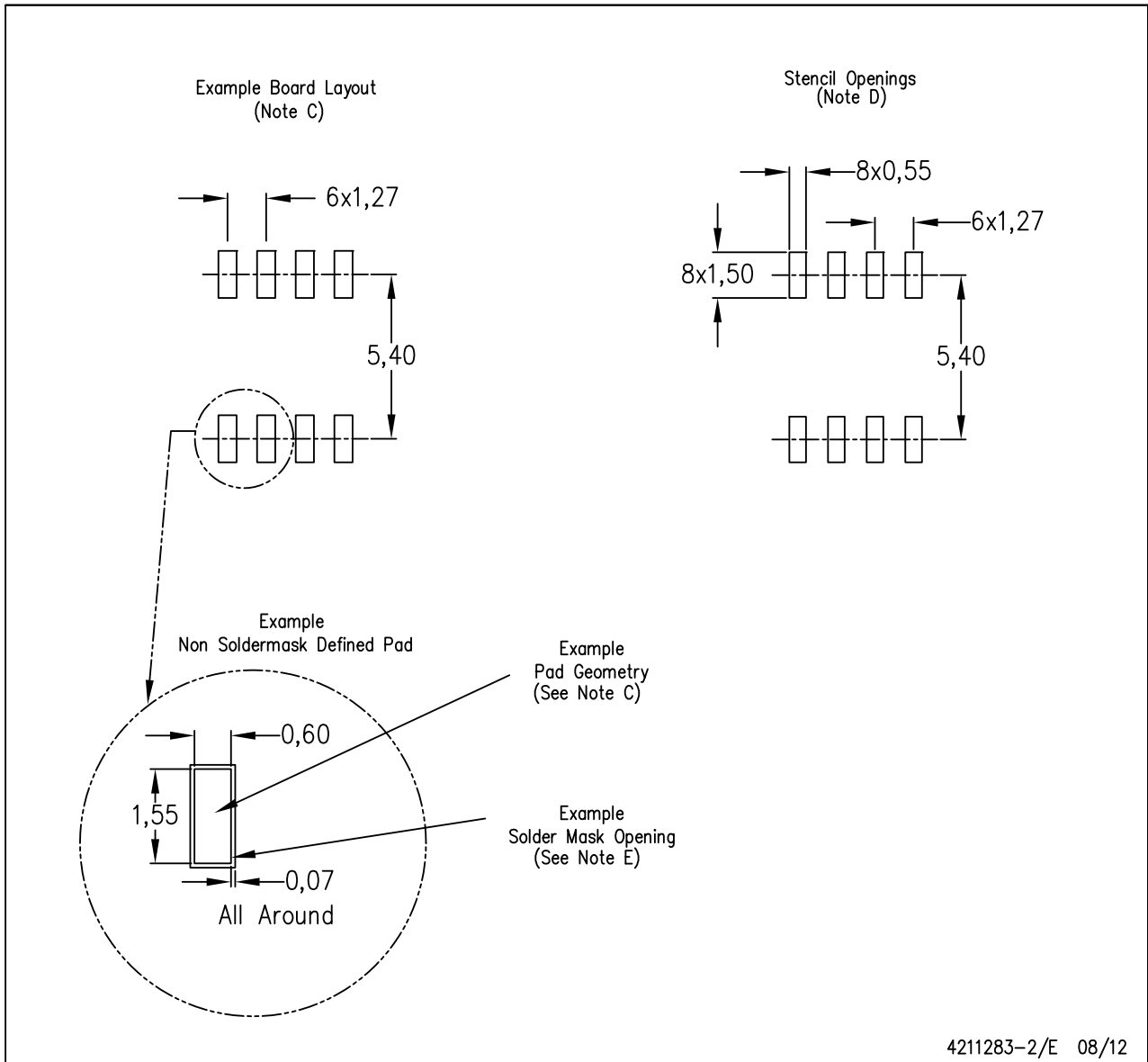
4040047-3/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

**LAND PATTERN DATA**

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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