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Infineon Technologies
BSZ018NE2LSI

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OptiMOS™ Power-MOSFET

Features

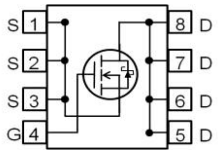
- Optimized for high performance Buck converter
- Monolithic integrated Schottky like diode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Pb-Free RoHS Halogen-Free

Product Summary

V_{DS}	25	V
$R_{DS(on),max}$	1.8	mΩ
I_D	40	A
Q_{OSS}	23	nC
Q_G(0V..10V)	36	nC

PG-TSDSON-8
(fused leads)



Type	Package	Marking
BSZ018NE2LSI	PG-TSDSON-8 (fused leads)	018NE2I

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	40	A
		V_{GS}=10 V, T_C=100 °C	40	
		V_{GS}=4.5 V, T_C=25 °C	40	
		V_{GS}=4.5 V, T_C=100 °C	40	
		V_{GS}=4.5 V, T_A=25 °C, R_{thJA}=60 K/W[2]	22	
Pulsed drain current[3]	$I_{D,pulse}$	T_C=25 °C	160	
Avalanche current, single pulse[4]	I_{AS}	T_C=25 °C	20	
Avalanche energy, single pulse	E_{AS}	I_D=20 A, R_{GS}=25 Ω	80	mJ
Gate source voltage	V_{GS}		±20	V

[1] J-STD20 and JESD22

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See figure 3 for more detailed information

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	69	W
		T_A=25 °C, R_{thJA}=60 K/W[2)]	2.1	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

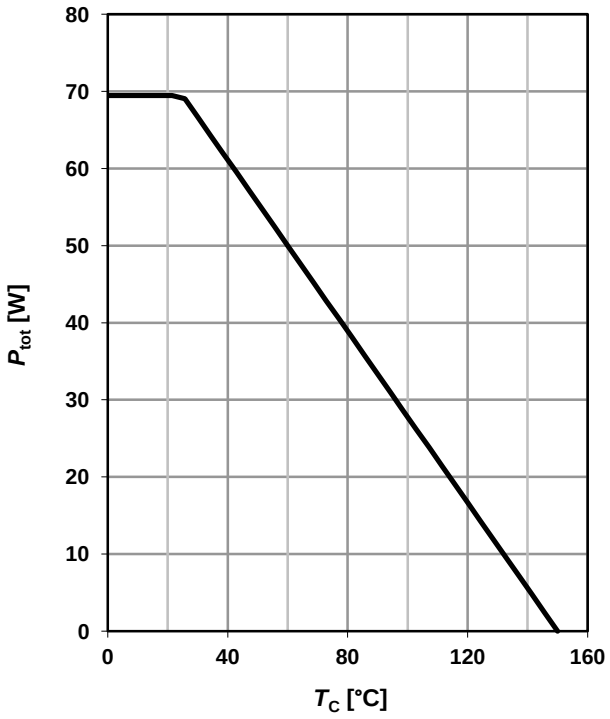
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.8	K/W
Device on PCB	R_{thJA}	6 cm^2 cooling area[2)]	-	-	60	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=10 mA	25	-	-	V
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	I_D=10 mA, referenced to 25 °C	-	15	-	mV/K
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1.2	-	2.0	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=20 V, V_{GS}=0 V, T_j=25 °C	-	-	0.5	mA
		V_{DS}=20 V, V_{GS}=0 V, T_j=125 °C	-	2	-	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=20 A	-	2.0	2.5	mΩ
		V_{GS}=10 V, I_D=20 A	-	1.5	1.8	
Gate resistance	R_G		0.4	0.8	1.6	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=20 A	50	100	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz	-	2500	3325	pF
Output capacitance	C_{oss}		-	1100	1463	
Reverse transfer capacitance	C_{rss}		-	110	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω	-	5.2	-	ns
Rise time	t_r		-	4.8	-	
Turn-off delay time	$t_{d(off)}$		-	25	-	
Fall time	t_f		-	3.6	-	
Gate Charge Characteristics[5]						
Gate to source charge	Q_{gs}	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	6.3	8.4	nC
Gate charge at threshold	$Q_{g(th)}$		-	4.1	-	
Gate to drain charge	Q_{gd}		-	4.3	6.5	
Switching charge	Q_{sw}		-	6.6	-	
Gate charge total	Q_g		-	17	23	
Gate plateau voltage	$V_{plateau}$			2.5		V
Gate charge total	Q_g	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 10 V	-	36	48	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	15	-	
Output charge	Q_{oss}	V_{DD}=12 V, V_{GS}=0 V	-	23	31	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	40	A
Diode pulse current	$I_{S,pulse}$		-	-	160	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=7 A, T_j=25 °C	-	0.55	0.7	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=7 A, di_F/dt=400 A/µs	-	5	-	nC

[4] See figure 13 for more detailed information
[5] See figure 16 for gate charge parameter definition

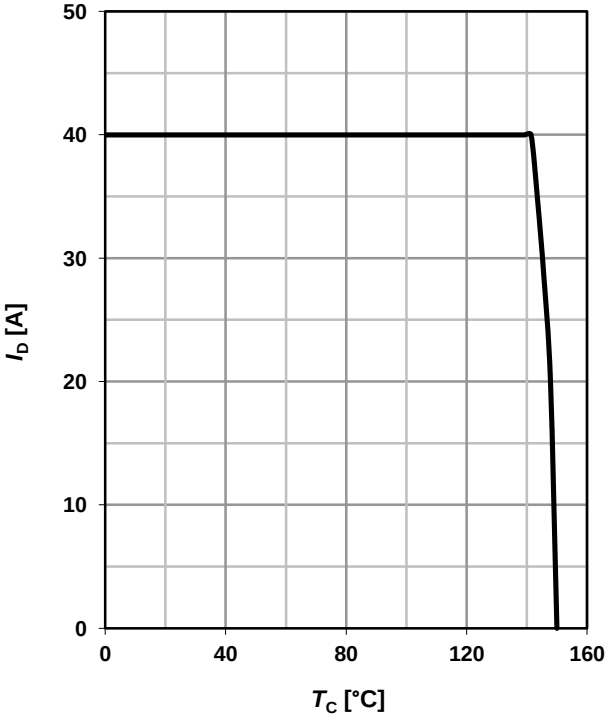
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

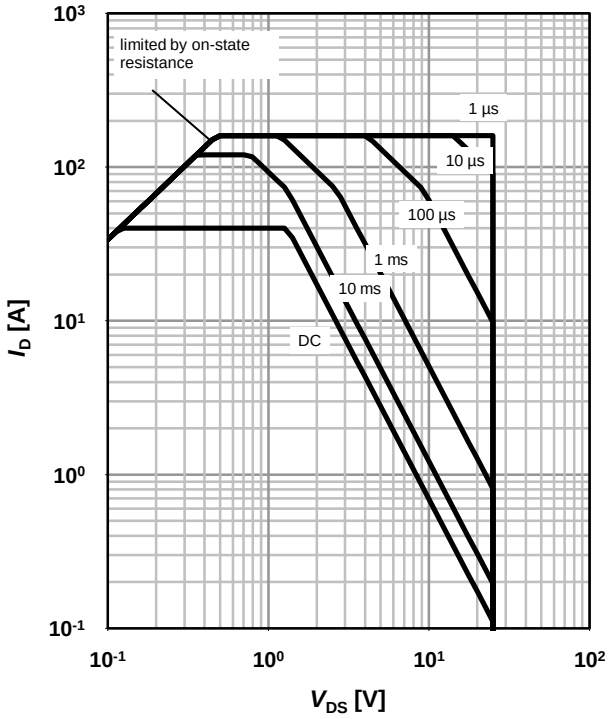
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

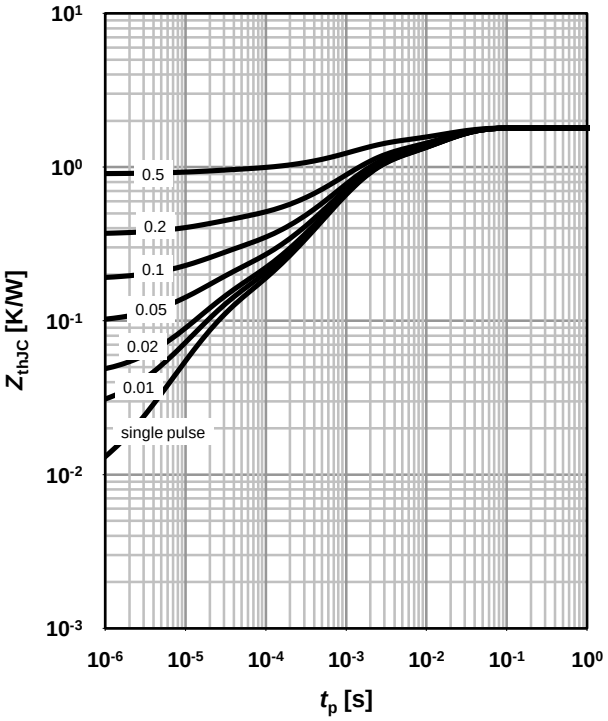
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

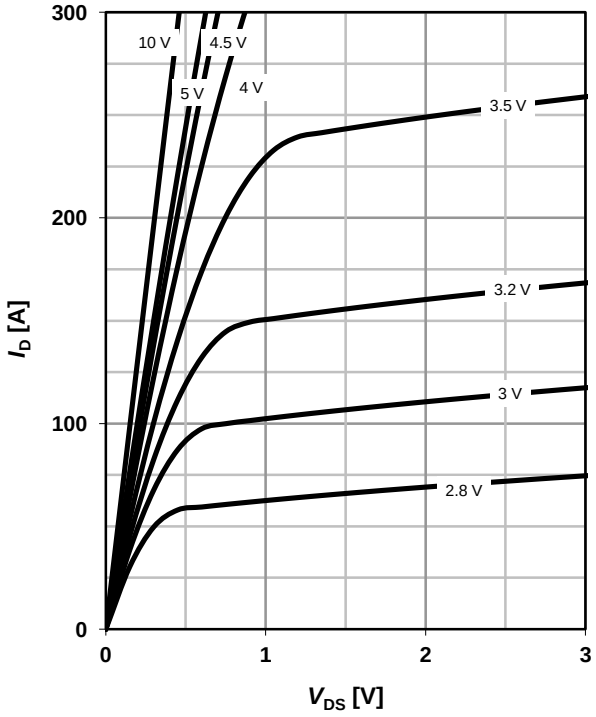
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

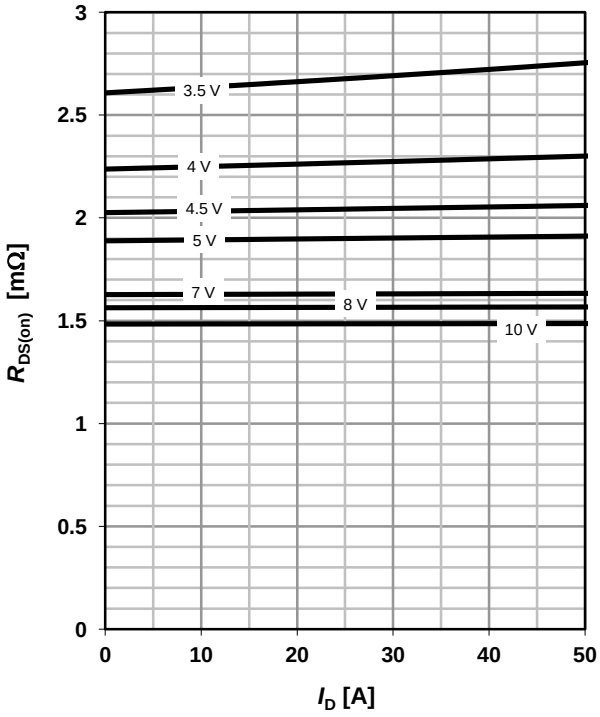
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

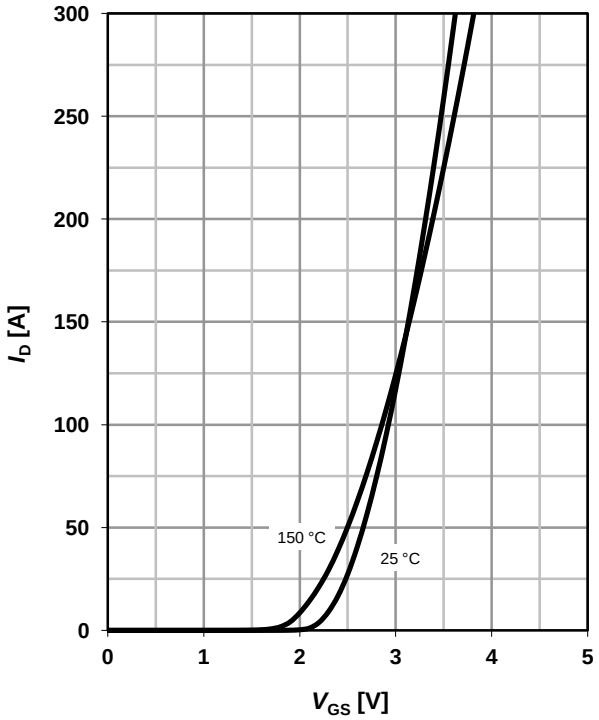
parameter: V_{GS}



7 Typ. transfer characteristics

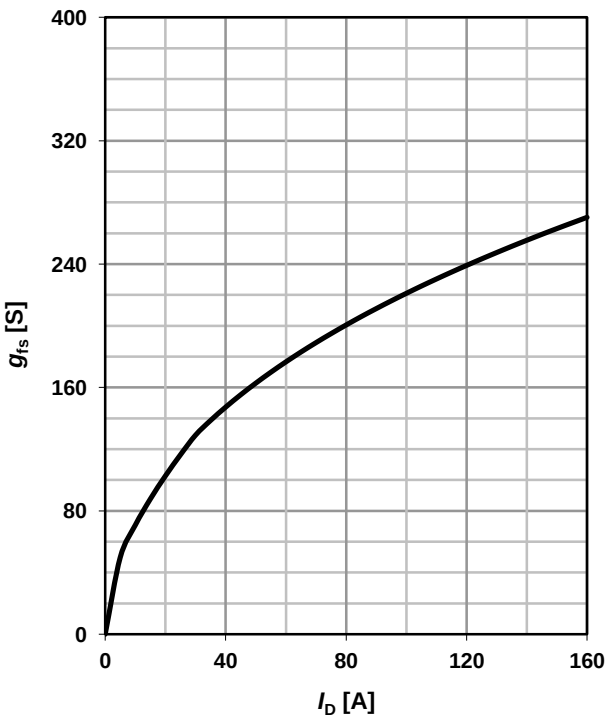
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



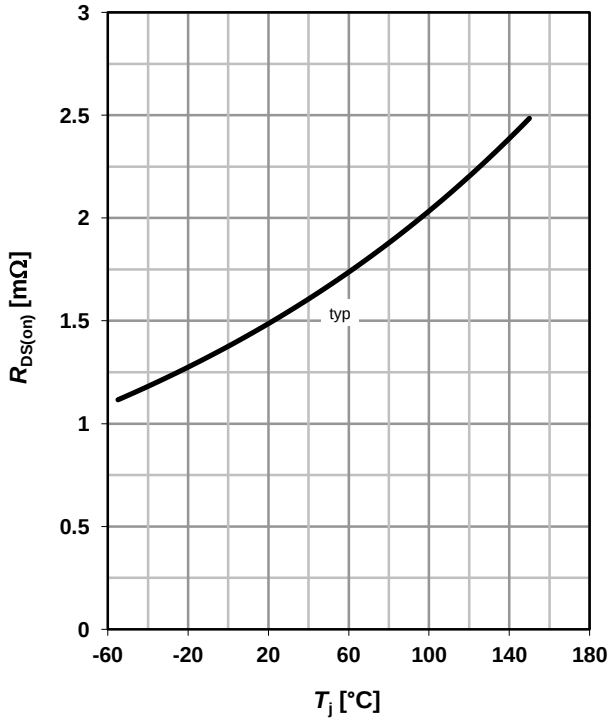
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



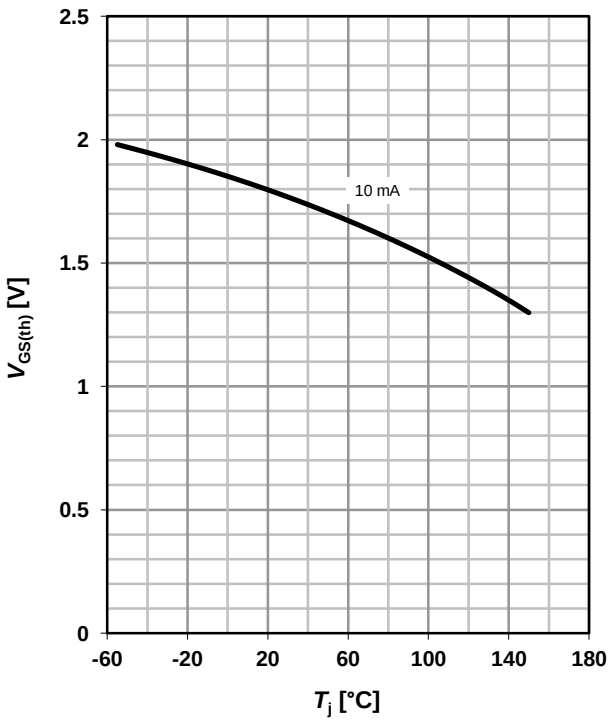
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V



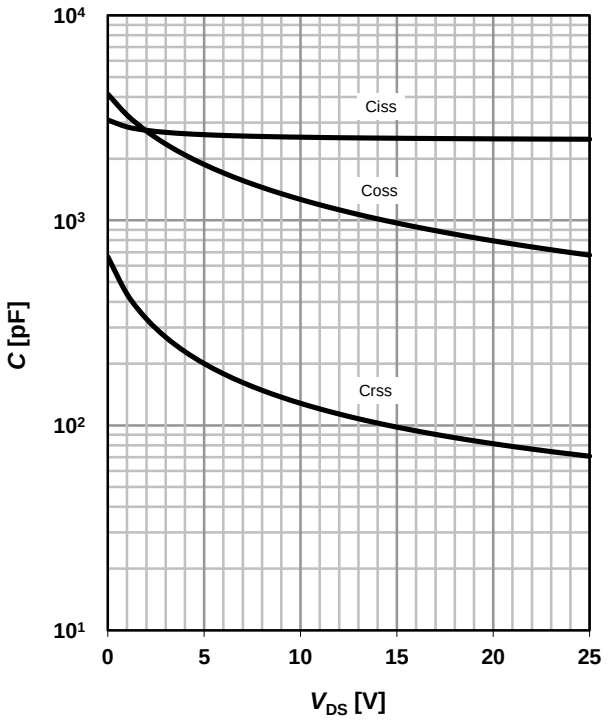
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=10 mA



11 Typ. capacitances

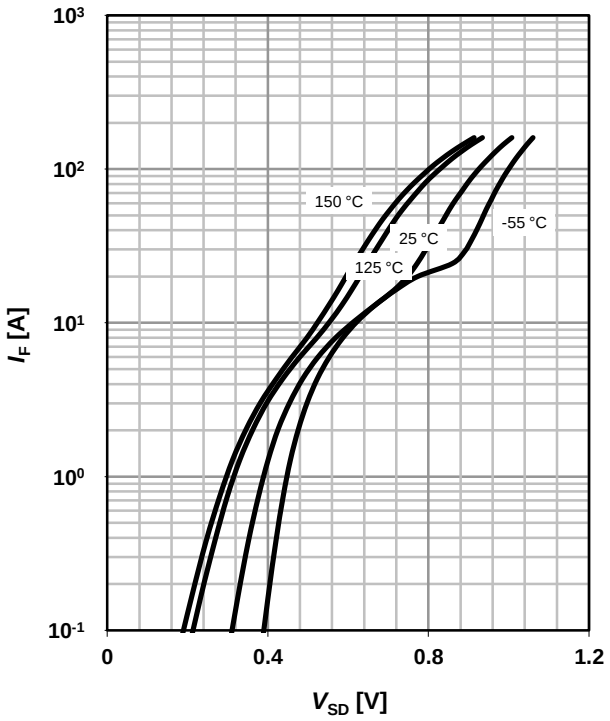
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

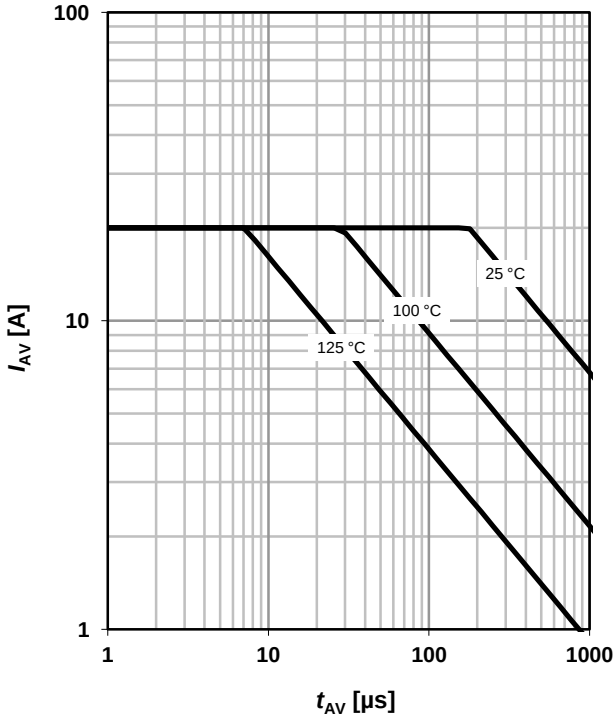
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

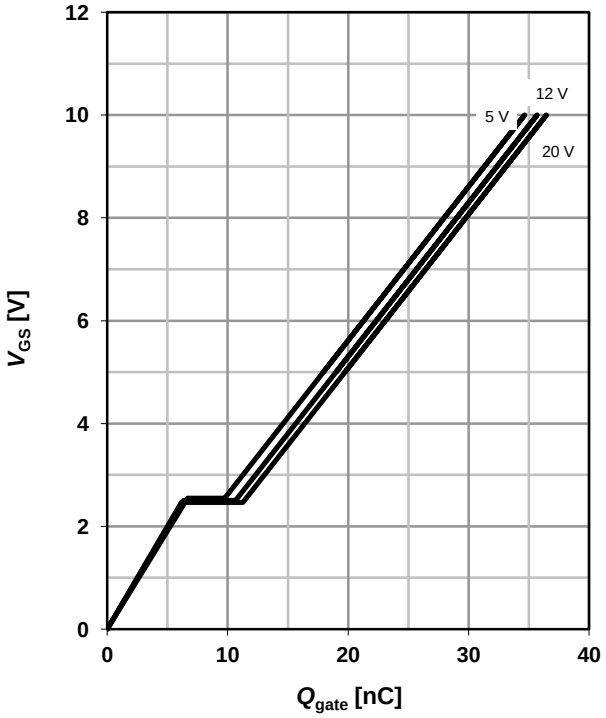
parameter: $T_{j(start)}$



14 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=30 A pulsed

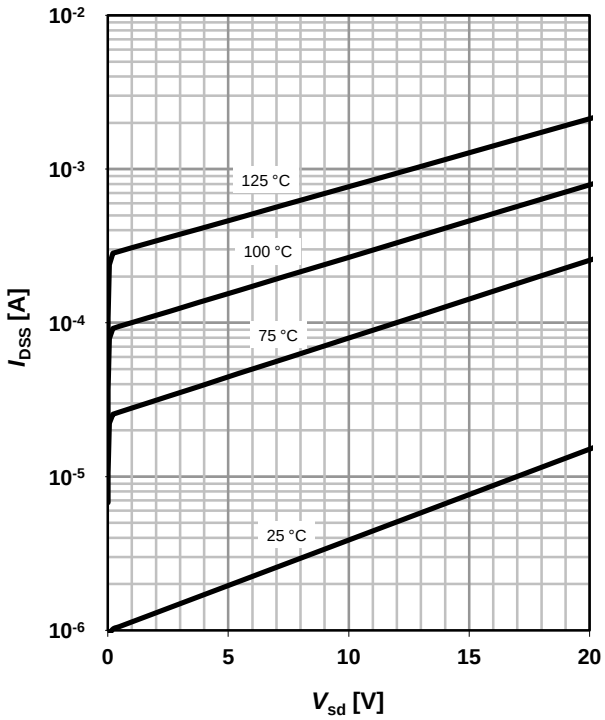
parameter: V_{DD}



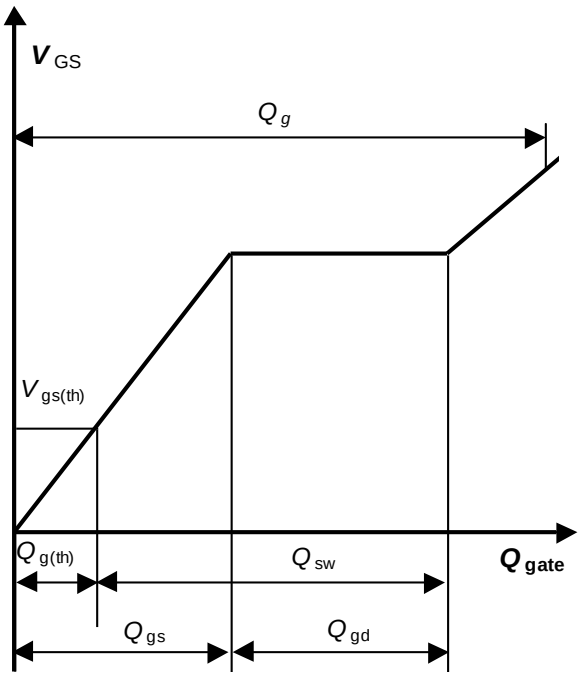
15 Typ. drain-source leakage current

I_{DSS}=f(V_{DS}); V_{GS}=0 V

parameter: T_j

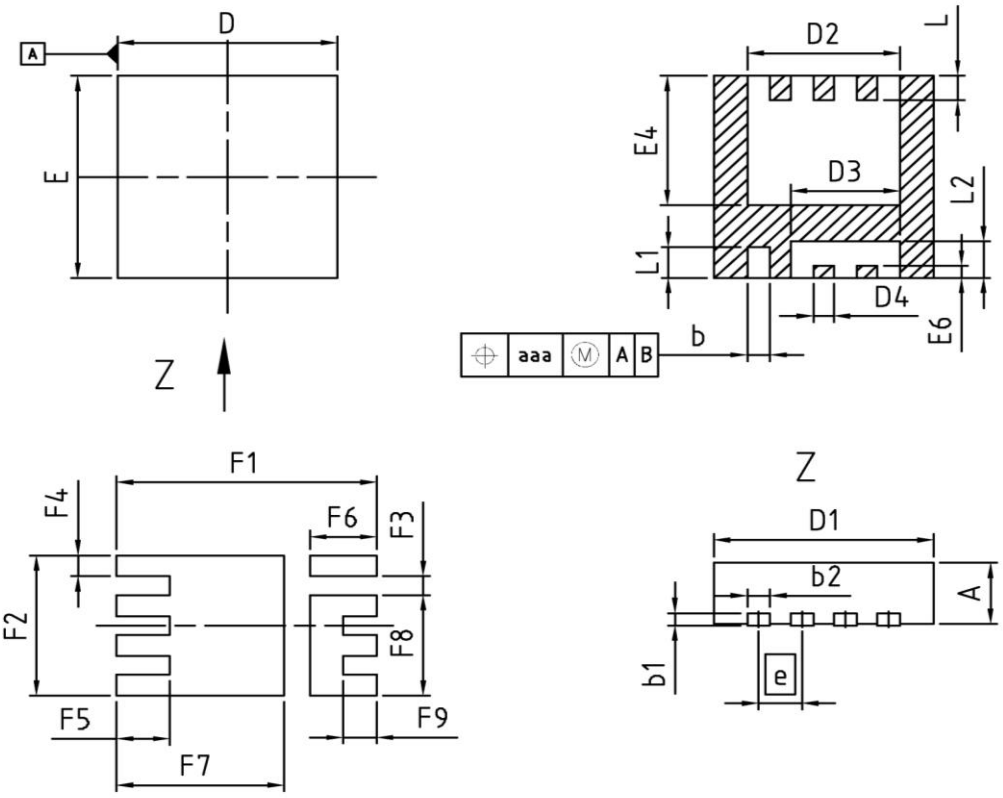


16 Gate charge waveforms



BSZ018NE2LSI

Package Outline **PG-TSDSON-8 (fused leads)**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.24	0.44	0.009	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.19	2.39	0.086	0.094
D3	1.54	1.74	0.061	0.069
D4	0.21	0.41	0.008	0.016
E	3.20	3.40	0.126	0.134
E4	2.01	2.21	0.079	0.087
E6	0.10	0.30	0.004	0.012
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.30	0.51	0.012	0.020
L1	0.40	0.70	0.016	0.028
L2	0.50	0.70	0.020	0.028
aaa	0.25		0.010	
F1	3.90		0.154	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.80		0.031	
F6	1.00		0.039	
F7	2.51		0.099	
F8	1.64		0.065	
F9	0.50		0.020	

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SCALE
0 2.5 5mm

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