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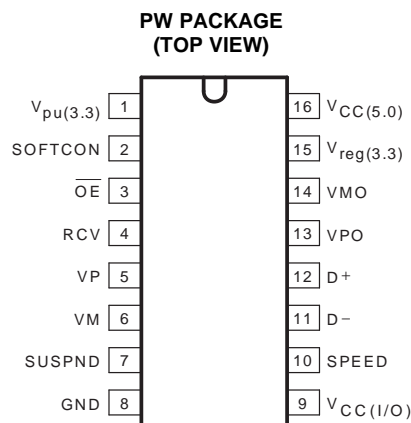
ADVANCED UNIVERSAL SERIAL BUS TRANSCEIVERS

Check for Samples: [TUSB1106-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Compatible With Universal Serial Bus Specification Rev. 2.0
- Transmit and Receive Serial Data at Both Full-Speed (12-Mbit/s) and Low-Speed (1.5-Mbit/s) Data Rates
- Integrated Bypassable 5-V to 3.3-V Voltage Regulator for Powering Via USB V_{BUS}
- V_{BUS} Disconnection Indication Through V_P and V_M
- Used as USB Device Transceiver or USB Host Transceiver
- Stable RCV Output During SE0 Condition
- Two Single-Ended Receivers With Hysteresis
- Low-Power Operation, Ideal for Portable Equipment
- Support I/O Voltage Range From 1.65 V to 3.6 V

- Available in a Thin Shrink Small-Outline Package [TSSOP (PW)]



DESCRIPTION

The TUSB1106-Q1 universal serial bus (USB) transceiver is compliant with the Universal Serial Bus Specification Rev. 2.0. This device can transmit and receive serial data at both full-speed (12-Mbit/s) and low-speed (1.5-Mbit/s) data rates. The TUSB1106-Q1 can be used as USB device transceiver or USB host transceiver.

The device allows USB application-specific ICs (ASICs) and programmable logic devices (PLDs), with power-supply voltages from 1.65 V to 3.6 V, to interface with the physical layer (PHY) of the universal serial bus. It has an integrated 5-V to 3.3-V voltage regulator for direct powering via the USB supply V_{BUS} .

The TUSB1106-Q1 allows only differential input mode and is available in a PW package.

The TUSB1106-Q1 is ideal for portable electronic devices such as mobile phones, personal digital assistants, information appliances, and digital still cameras.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ (2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|----------------------------|--------------|-----------------------|------------------|
| -40°C to 85°C | TSSOP – PW | Reel of 2000 | TUSB1106IPWRQ1 | TU1106I |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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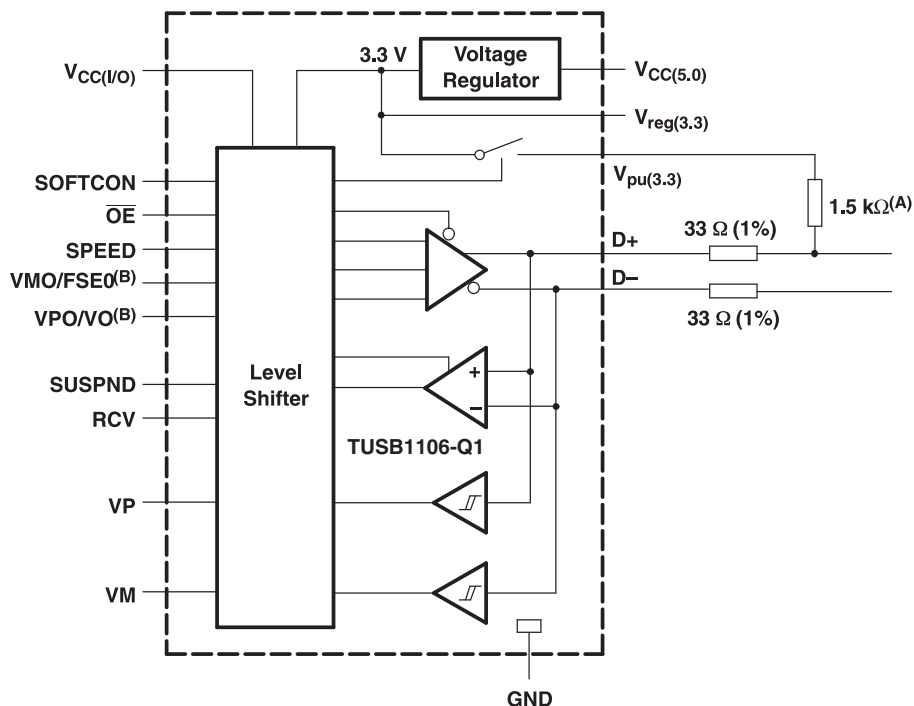
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FUNCTIONAL BLOCK DIAGRAM



- A. Connect to D– for low-speed operation and to D+ for high-speed operation.
- B. Pin function depends on device type.

TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|-----------------|-----|------|---|
| NAME | NO. | | |
| \overline{OE} | 3 | I | Output enable (CMOS level with respect to $V_{CC(I/O)}$, active LOW). Enables the transceiver to transmit data on the USB bus input pad. Push pull, CMOS. |
| RCV | 4 | O | Differential data receiver (CMOS level with respect to $V_{CC(I/O)}$). Driven LOW when input SUSPND is HIGH. The output state of RCV is preserved and stable during an SE0 condition output pad. Push pull, 4-mA output drive, CMOS. |
| VP | 5 | O | Single-ended D+ receiver (CMOS level with respect to V). For external detection of single-ended zero (SE0), error conditions, speed of connected device. Driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$ output pad. Push pull, 4-mA output drive, CMOS. |
| VM | 6 | O | Single-ended D– receiver (CMOS level with respect to $V_{CC(I/O)}$). For external detection of single-ended zero (SE0), error conditions, speed of connected device. Driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$ output pad. Push pull, 4-mA output drive, CMOS. |
| SUSPND | 7 | I | Suspend (CMOS level with respect to $V_{CC(I/O)}$). A HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW-level input pad. Push pull, CMOS. |
| MODE | | I | Mode (CMOS level with respect to $V_{CC(I/O)}$). A HIGH level enables the differential input mode (VPO, VMO), whereas a LOW level enables a single-ended input mode (VO, FSE0). See Table 5 and Table 6 input pad. Push pull, CMOS. |
| GND | 8 | | Ground supply |
| $V_{CC(I/O)}$ | 9 | | Supply voltage for digital I/O pins (1.65 to 3.6 V). When $V_{CC(I/O)}$ is not connected, the D+ and D– pins are in 3-state. This supply pin is independent of $V_{CC(5.0)}$ and $V_{reg(3.3)}$ and must never exceed the $V_{reg(3.3)}$ voltage. |
| SPEED | 10 | I | Speed selection (CMOS level with respect to $V_{CC(I/O)}$). Adjusts the slew rate of differential data outputs D+ and D– according to the transmission speed. Input pad, push pull, CMOS. LOW – low speed (1.5 Mbit/s) HIGH – full speed (12 Mbit/s) |
| D– | 11 | AI/O | Negative USB data bus connection (analog, differential). For low-speed mode, connect to pin $V_{pu(3.3)}$ via a 1.5-k Ω resistor. |
| D+ | 12 | AI/O | Positive USB data bus connection (analog, differential). For full-speed mode, connect to pin $V_{pu(3.3)}$ via a 1.5-k Ω resistor. |
| VPO/VO | | I | Driver data (CMOS level with respect to $V_{CC(I/O)}$, Schmitt trigger). See Driving Function table . Push pull, CMOS. |
| VPO | 13 | | |
| VMO/FSE0 | | I | Driver data (CMOS level with respect to $V_{CC(I/O)}$, Schmitt trigger). See Driving Function table . Push pull, CMOS. |
| VMO | 14 | | |
| $V_{reg(3.3)}$ | 15 | | Internal regulator option. Regulated supply-voltage output (3 V to 3.6 V) during 5-V operation. A decoupling capacitor of at least 0.1 mF is required for the regulator bypass option. Used as a supply-voltage input for 3.3 V \pm 10% operation. |
| $V_{CC(5.0)}$ | 16 | | Internal regulator option. Supply-voltage input (4 V to 5.5 V). Can be connected directly to USB supply VBUS regulator bypass option. Connect to $V_{reg(3.3)}$. |
| $V_{pu(3.3)}$ | 1 | | Pullup supply voltage (3.3 V \pm 10%). Connect an external 1.5-k Ω resistor on D+ (full speed) or D– (low speed). Pin function is controlled by input SOFTCON. SOFTCON = LOW – $V_{pu(3.3)}$ floating (high impedance), ensures zero pullup current SOFTCON = HIGH – $V_{pu(3.3)}$ = 3.3 V, internally connected to $V_{reg(3.3)}$ |
| SOFTCON | 2 | I | Software-controlled USB connection. A HIGH level applies 3.3 V to pin $V_{pu(3.3)}$, which is connected to an external 1.5-k Ω pullup resistor. This allows USB connect/disconnect signaling to be controlled by software input pad. Push pull, CMOS. |

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FUNCTIONAL DESCRIPTION

Function Selection

FUNCTION TABLE

| SUSPND | \overline{OE} | D+, D– | RCV | VP, VM | FUNCTION |
|--------|-----------------|--------------------------|-------------------------|--------|--|
| L | L | Driving and receiving | Active | Active | Normal driving (differential receiver active) |
| L | H | Receiving ⁽¹⁾ | Active | Active | Receiving |
| H | L | Driving | Inactive ⁽²⁾ | Active | Driving during suspend ⁽³⁾ (differential receiver inactive) |
| H | H | High-Z ⁽¹⁾ | Inactive ⁽²⁾ | Active | Low-power state |

- (1) Signal levels on D+ and D– are determined by other USB devices and external pullup/pulldown resistors.
 (2) In suspend mode (SUSPND = HIGH) the differential receiver is inactive and output RCV is always LOW. Out of suspend (K), signaling is detected via the single-ended receivers VP and VM.
 (3) During suspend, the slew-rate control circuit of low-speed operation is disabled. The D+ and D– lines are still driven to their intended states, without slew-rate control. This is permitted because driving during suspend is used to signal remote wakeup by driving a K signal (one transition from idle to K state) for a period of 1 ms to 15 ms.

Operating Functions

**Driving Function (Pin \overline{OE} = L)
Using Differential Input Data Interface**

| VMO | VPO | DATA | DATA STATE | |
|-----|-----|----------------------|------------|------------|
| | | | LOW SPEED | FULL SPEED |
| L | L | SE0 | X | X |
| H | L | Differential logic 0 | J | K |
| L | H | Differential logic 1 | K | J |
| H | H | Illegal state | X | X |

Table 1. Receiving Function (Pin \overline{OE} = H)

| D+, D– | RCV | VP ⁽¹⁾ | VM ⁽¹⁾ | DATA STATE | |
|----------------------|---------------------|-------------------|-------------------|------------|------------|
| | | | | LOW SPEED | FULL SPEED |
| Differential logic 0 | L | L | H | J | K |
| Differential logic 1 | H | H | L | K | J |
| SE0 | RCV* ⁽²⁾ | L | L | X | X |

- (1) VP = VM = H indicates the sharing mode ($V_{CC(5.0)}$ and $V_{reg(3.3)}$ are disconnected).
 (2) RCV* denotes the signal level on output RCV just before SE0 state occurs. This level is stable during the SE0 period.

Power-Supply Configurations

The TUSB1106-Q1 can be used with different power-supply configurations, which can be dynamically changed. An overview is given in [Table 3](#).

- Normal mode – Both $V_{CC(I/O)}$ and $V_{CC(5.0)}$ or ($V_{CC(5.0)}$ and $V_{reg(3.3)}$) are connected. For 5-V operation, $V_{CC(5.0)}$ is connected to a 5-V source (4 V to 5.5 V). The internal voltage regulator then produces 3.3 V for the USB connections. For 3.3-V operation, both $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are connected to a 3.3-V source (3 V to 3.6 V). $V_{CC(I/O)}$ is independently connected to a voltage source (1.65 V to 3.6 V), depending on the supply voltage of the external circuit.
- Disable mode – $V_{CC(I/O)}$ is not connected, $V_{CC(5.0)}$ or ($V_{CC(5.0)}$ and $V_{reg(3.3)}$) are connected. In this mode, the internal circuits of the TUSB1106-Q1 ensure that the D+ and D– pins are in 3-state and the power consumption drops to the low-power (suspended) state level. Some hysteresis is built into the detection of $V_{CC(I/O)}$ lost.
- Sharing mode – $V_{CC(I/O)}$ is connected, ($V_{CC(5.0)}$ and $V_{reg(3.3)}$) are not connected. In this mode, the D+ and D– pins are made 3-state and the TUSB1106-Q1 allows external signals of up to 3.6 V to share the D+ and D–

lines. The internal circuits of the TUSB1106-Q1 ensure that virtually no current (maximum 10 μ A) is drawn via the D+ and D– lines. The power consumption through $V_{CC(I/O)}$ drops to the low-power (suspended) state level. Both the VP and VM pins are driven HIGH to indicate this mode. Pin RCV is made LOW. Some hysteresis is built into the detection of $V_{reg(3.3)}$ lost.

Table 2. Pin States in Disable or Sharing Mode

| PINS | DISABLE-MODE STATE | SHARING-MODE STATE |
|---|---|-----------------------|
| $V_{CC(5.0)}/V_{reg(3.3)}$ | 5-V input/3.3-V output, 3.3-V input/3.3-V input | Not present |
| $V_{CC(I/O)}$ | Not present | 1.65-V to 3.6-V input |
| $V_{pu(3.3)}$ | High impedance (off) | High impedance (off) |
| D+, D– | High impedance | High impedance |
| VP, VM | Invalid ⁽¹⁾ | H |
| RCV | Invalid ⁽²⁾ | L |
| Inputs (VO/VPO, FSE0/VMO, SPEED, SUSPND, OE, SOFTCON) | High impedance | High impedance |

(1) High impedance or driven LOW

(2) High impedance or driven LOW

Table 3. Power-Supply Configuration Overview

| $V_{CC(5.0)}$ or $V_{reg(3.3)}$ | $V_{CC(I/O)}$ | CONFIGURATION | SPECIAL CHARACTERISTICS |
|---------------------------------|---------------|---------------|--|
| Connected | Connected | Normal mode | |
| Connected | Not connected | Disable mode | D+, D–, and $V_{pu(3.3)}$ are in high impedance. VP, VM, and RCV are invalid. ⁽¹⁾ |
| Not connected | Connected | Sharing mode | D+, D–, and $V_{pu(3.3)}$ are in high impedance. VP and VM are driven HIGH. RCV is driven LOW. |

(1) High impedance or driven LOW

Power-Supply Input Options

The TUSB1106-Q1 has two power-supply input options.

- Internal regulator – $V_{CC(5.0)}$ is connected to 4 V to 5.5 V. The internal regulator is used to supply the internal circuitry with 3.3 V (nominal). $V_{reg(3.3)}$ becomes a 3.3-V output reference.
- Regulator bypass – $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are connected to the same supply. The internal regulator is bypassed and the internal circuitry is supplied directly from the $V_{reg(3.3)}$ power supply. The voltage range is 3 V to 3.6 V to comply with the USB specification.

The supply-voltage range for each input option is specified in [Table 4](#).

Table 4. Power-Supply Input Options

| INPUT OPTION | $V_{CC(5.0)}$ | $V_{REG(3.3)}$ | $V_{CC(I/O)}$ |
|--------------------|---|---|---|
| Internal regulator | Supply input for internal regulator (4 V to 5.5 V) | Voltage-reference output (3.3 V, 300 μ A) | Supply input for digital I/O pins (1.65 V to 3.6 V) |
| Regulator bypass | Connected to $V_{reg(3.3)}$ with maximum voltage drop of 0.3 V (2.7 V to 3.6 V) | Supply input (3 V to 3.6 V) | Supply input for digital I/O pins (1.65 V to 3.6 V) |

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---------------------------|--|---------------------|--------|
| $V_{CC(5.0)}$ | Supply voltage range | –0.5 | 6 | V |
| $V_{I(I/O)}$ | Supply voltage range | –0.5 | 4.6 | V |
| $V_{CCreg(3.3)}$ | Regulated voltage range | –0.5 | 4.6 | V |
| V_I | DC input voltage | –0.5 | $V_{CC(I/O)} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I = -1.8 \text{ V to } 5.4 \text{ V}$ | | 100 mA |
| T_{stg} | Storage temperature range | –40 | 125 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | | MIN | NOM | MAX | UNIT |
|------------------|---|-----------------|------|-----|---------------|------|
| $V_{CC(5.0)}$ | Supply voltage, internal regulator option | 5-V operation | 4 | 5 | 5.5 | V |
| $V_{CCreg(3.3)}$ | Supply voltage, regulator bypass option | 3.3-V operation | 3 | 3.3 | 3.6 | V |
| $V_{CC(I/O)}$ | I/O supply voltage | | 1.65 | | 3.6 | V |
| V_I | I/O supply voltage | | 0 | | $V_{CC(I/O)}$ | V |
| $V_{I/O}$ | Input voltage on analog I/O pins (D+, D–) | | 0 | | 3.6 | V |
| T_c | Junction temperature | | –40 | | 85 | °C |

STATIC ELECTRICAL CHARACTERISTICS – SUPPLY PINS

over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|--|-----|------|-----|---------|
| $V_{reg(3.3)}$ | Regulated supply-voltage output | Internal regulator option, $I_{load} \leq 300 \mu A^{(1)(2)}$ | 3 | 3.3 | 3.6 | V |
| I_{CC} | Operating supply current | Full-speed transmitting and receiving at 12 Mbit/s, $C_L = 50 \text{ pF}$ on D+ and D- ⁽³⁾ | | 6 | 8 | mA |
| $I_{CC(I/O)}$ | Operating I/O supply current | Full-speed transmitting and receiving at 12 Mbit/s ⁽³⁾ | | 2.3 | 2.5 | mA |
| $I_{CC(idle)}$ | Supply current during full-speed idle and SE0 | Full-speed idle: $V_{D+} > 2.7 \text{ V}$, $V_{D-} < 0.3 \text{ V}$ SE0: $V_{D+} < 0.3 \text{ V}$, $V_{D-} < 0.3 \text{ V}^{(4)}$ | | | 500 | μA |
| $I_{CC(I/O)(static)}$ | Static I/O supply current | Full-speed idle, SE0 or suspend | | 10 | 22 | μA |
| $I_{CC(susp)}$ | Suspend supply current | SUSPND = HIGH ⁽⁴⁾ | | 10 | 22 | μA |
| $I_{CC(dis)}$ | Disable-mode supply current | $V_{CC(I/O)}$ not connected ⁽⁴⁾ | | 10 | 22 | μA |
| $I_{CC(I/O)(sharing)}$ | Sharing-mode I/O supply current | $V_{CC(5.0)}$ or $V_{reg(3.3)}$ not connected | | 10 | 22 | μA |
| $I_{Dx(sharing)}$ | Sharing-mode load current on D+ and D- | $V_{CC(5.0)}$ or $V_{reg(3.3)}$ not connected, SOFTCON = LOW, $V_{Dx} = 3.6 \text{ V}$ | | | 10 | μA |
| $V_{reg(3.3)th}$ | Regulated supply-voltage detection threshold | $1.65 \text{ V} \leq V_{CC(I/O)} \leq V_{reg(3.3)}$, $2.7 \text{ V} \leq V_{reg(3.3)} \leq 3.6 \text{ V}$ | | | 0.8 | V |
| | | Supply lost during power down Supply detect during power up ⁽⁵⁾ | | 2.4 | | |
| $V_{reg(3.3)hys}$ | Regulated supply-voltage detection hysteresis | $V_{CC(I/O)} = 1.8 \text{ V}$ | | 0.45 | | V |
| $V_{CC(I/O)th}$ | I/O supply-voltage detection threshold | $V_{reg(3.3)} = 2.7 \text{ V}$ to 3.6 V | | | 0.5 | V |
| | | Supply lost during power down Supply detect during power up | | 1.4 | | |
| $V_{CC(I/O)hys}$ | I/O supply-voltage detection hysteresis | $V_{reg(3.3)} = 3.3 \text{ V}$ | | 0.45 | | V |

(1) I_{load} includes the pullup resistor current via $V_{pu(3.3)}$.

(2) In suspend mode, the typical voltage is 2.8 V.

(3) Maximum value is characterized only, not tested in production.

(4) Excluding any load current and $V_{pu(3.3)}/V_{sw}$ source current to the 1.5-k Ω and 15-k Ω pullup and pulldown resistors (200 μA typ)

(5) When $V_{CC(I/O)} < 2.7 \text{ V}$, the minimum value for $V_{reg(3.3)th}$ (present) is 2 V.

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STATIC ELECTRICAL CHARACTERISTICS – DIGITAL PINS

over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC(I/O)}$ | MIN | MAX | UNIT |
|------------------------------------|-------------------------|--------------------|----------------------|-------------------|---------|
| V_{IL} LOW-level input voltage | | 1.65 V to 3.6 V | | $0.3 V_{CC(I/O)}$ | V |
| V_{IH} HIGH-level input voltage | | 1.65 V to 3.6 V | $0.6 V_{CC(I/O)}$ | | V |
| V_{OL} LOW-level output voltage | $I_{OL} = 100 \mu A$ | 1.65 V to 3.6 V | | 0.15 | V |
| | $I_{OL} = 2 \text{ mA}$ | | | 0.4 | |
| | $I_{OL} = 100 \mu A$ | 1.8 V \pm 0.15 V | | 0.15 | |
| | $I_{OL} = 2 \text{ mA}$ | | | 0.4 | |
| | $I_{OL} = 100 \mu A$ | 2.5 V \pm 0.2 V | | 0.15 | |
| | $I_{OL} = 2 \text{ mA}$ | | | 0.4 | |
| | $I_{OL} = 100 \mu A$ | 3.3 V \pm 0.3 V | | 0.15 | |
| | $I_{OL} = 2 \text{ mA}$ | | | 0.4 | |
| V_{OH} HIGH-level output voltage | $I_{OH} = 100 \mu A$ | 1.65 V to 3.6 V | $V_{CC(I/O)} - 0.15$ | | V |
| | $I_{OH} = 2 \text{ mA}$ | | $V_{CC(I/O)} - 0.4$ | | |
| | $I_{OH} = 100 \mu A$ | 1.8 V \pm 0.15 V | 1.5 | | |
| | $I_{OH} = 2 \text{ mA}$ | | 1.25 | | |
| | $I_{OH} = 100 \mu A$ | 2.5 V \pm 0.2 V | 2.15 | | |
| | $I_{OH} = 2 \text{ mA}$ | | 1.9 | | |
| | $I_{OH} = 100 \mu A$ | 3.3 V \pm 0.3 V | 2.85 | | |
| | $I_{OH} = 2 \text{ mA}$ | | 2.6 | | |
| I_{LI} Input leakage current | | | -1 | 1 | μA |
| C_{IN} Input capacitance | Pin to GND | | | 3.5 | pF |

STATIC ELECTRICAL CHARACTERISTICS – ANALOG I/O PINS

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4\text{ V to }5.5\text{ V}$ or $V_{reg(3.3)} = 3\text{ V to }3.6\text{ V}$, $V_{GND} = 0\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|----------------------|-----|-----|---------------|
| V_{DI} Differential input sensitivity | $ V_{I(D+)} - V_{I(D-)} $ | 0.2 | | | V |
| V_{CM} Differential common-mode voltage | Includes V_{DI} range | 0.8 | | 2.5 | V |
| V_{IL} LOW-level input voltage, single-ended receiver | | 2 | | 0.8 | V |
| V_{IH} HIGH-level input voltage, single-ended receiver | | 0.4 | | | V |
| V_{hys} Hysteresis voltage, single-ended receiver | | | | 0.7 | V |
| V_{OL} LOW-level output voltage | $R_L = 1.5\text{ k}\Omega$ to 3.6 V | | | 0.3 | V |
| V_{OH} HIGH-level output voltage | $R_L = 1.5\text{ k}\Omega$ to GND | 2.8 ⁽¹⁾ | | 3.6 | V |
| I_{LZ} OFF-state leakage current | | | | 1 | μA |
| C_{IN} Transceiver capacitance | Pin to GND | | | 25 | pF |
| Z_{DRV} Driver output impedance | Steady-state drive | 34 ⁽²⁾ | 39 | 44 | Ω |
| Z_{INP} Input impedance | | 10 | | | M Ω |
| R_{SW} Internal switch resistance at $V_{pu(3.3)}$ | | | | 13 | Ω |
| V_{TERM} Termination voltage for upstream port pullup (RPU) | | 3 ⁽³⁾ (4) | | 3.6 | V |

(1) $V_{OH(min)} = V_{reg(3.3)} - 0.2\text{ V}$

(2) Includes external resistors of $33\text{ }\Omega \pm 1\%$ on both D+ and D–

(3) This voltage is available at $V_{reg(3.3)}$ and $V_{pu(3.3)}$.

(4) In suspend mode, the minimum voltage is 2.7 V .

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DYNAMIC ELECTRICAL CHARACTERISTICS – ANALOG I/O PINS (D+, D–)^{(1) (2)} Driver Characteristics, Full-Speed Mode

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4\text{ V to }5.5\text{ V}$ or $V_{reg(3.3)} = 3\text{ V to }3.6\text{ V}$, $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$, $V_{GND} = 0\text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------|---|---|-----|-------|------|
| t_{FR} | Rise time | $C_L = 50\text{ pF to }125\text{ pF}$, 10% to 90% of $ V_{OH} - V_{OL} $ (see Figure 1) | 4 | 20 | ns |
| t_{FF} | Fall time | $C_L = 50\text{ pF to }125\text{ pF}$, 90% to 10% of $ V_{OH} - V_{OL} $ (see Figure 1) | 4 | 20 | ns |
| FRFM | Differential rise/fall time matching (t_{FR}/t_{FF}) | Excluding the first transition from idle state | 90 | 111.1 | % |
| V_{CRS} | Output signal crossover voltage | Excluding the first transition from idle state (see Figure 10) | 1.3 | 2 | V |

(1) Test circuit, see Figure 13

(2) Driver timing in low-speed mode is not specified. Low-speed delay timings are dominated by the slow rise/fall times t_{LR} and t_{LF} .

DYNAMIC ELECTRICAL CHARACTERISTICS – ANALOG I/O PINS (D+, D–)^{(1) (2)} Driver Characteristics, Low-Speed Mode

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4\text{ V to }5.5\text{ V}$ or $V_{reg(3.3)} = 3\text{ V to }3.6\text{ V}$, $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$, $V_{GND} = 0\text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------|---|--|-----|-----|------|
| t_{LR} | Rise time | $C_L = 200\text{ pF to }600\text{ pF}$, 10% to 90% of $ V_{OH} - V_{OL} $ (see Figure 1) | 75 | 300 | ns |
| t_{LF} | Fall time | $C_L = 200\text{ pF to }600\text{ pF}$, 90% to 10% of $ V_{OH} - V_{OL} $ (see Figure 1) | 75 | 300 | ns |
| LRFM | Differential rise/fall time matching (t_{LR}/t_{LF}) | Excluding the first transition from idle state | 80 | 125 | % |
| V_{CRS} | Output signal crossover voltage | Excluding the first transition from idle state (see Figure 10) | 1.3 | 2 | V |

(1) Test circuit, see Figure 13

(2) Driver timing in low-speed mode is not specified. Low-speed delay timings are dominated by the slow rise/fall times t_{LR} and t_{LF} .

DYNAMIC ELECTRICAL CHARACTERISTICS – ANALOG I/O PINS (D+, D–)^{(1) (2)} Driver Timing, Full-Speed Mode

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4\text{ V to }5.5\text{ V}$ or $V_{reg(3.3)} = 3\text{ V to }3.6\text{ V}$, $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$, $V_{GND} = 0\text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------|--|----------------------------|-----|-----|------|
| $t_{PLH(drv)}$ | Driver propagation delay (VO/VPO, FSE0/VMO to D+, D–) | LOW to HIGH (see Figure 4) | | 18 | ns |
| $t_{PHL(drv)}$ | | HIGH to LOW (see Figure 4) | | 18 | |
| t_{PHZ} | Driver disable delay (\overline{OE} to D+, D–) | HIGH to OFF (see Figure 2) | | 15 | ns |
| t_{PLZ} | | LOW to OFF (see Figure 2) | | 15 | |
| t_{PZH} | Driver enable delay (\overline{OE} to D+, D–) | OFF to HIGH (see Figure 2) | | 15 | ns |
| t_{PZL} | | OFF to LOW (see Figure 2) | | 15 | |

(1) Test circuit, see Figure ?

(2) Driver timing in low-speed mode is not specified. Low-speed delay timings are dominated by the slow rise/fall times t_{LR} and t_{LF} .

DYNAMIC ELECTRICAL CHARACTERISTICS FOR ANALOG I/O PINS (D+, D–)⁽¹⁾ Receiver Timing, Full-Speed and Low-Speed Mode, Differential Receiver

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4\text{ V to }5.5\text{ V}$ or $V_{reg(3.3)} = 3\text{ V to }3.6\text{ V}$, $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$, $V_{GND} = 0\text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------|----------------------------|-----|-----|------|
| $t_{PLH(rcv)}$ | LOW to HIGH (see Figure 3) | | 15 | ns |
| $t_{PHL(rcv)}$ | HIGH to LOW (see Figure 3) | | 15 | |

(1) Test circuit, see Figure ?

DYNAMIC ELECTRICAL CHARACTERISTICS FOR ANALOG I/O PINS (D+, D–)⁽¹⁾ Receiver Timing, Full-Speed and Low-Speed Mode, Single-Ended Receiver

over recommended ranges of operating free-air temperature and supply voltage, $V_{CC} = 4\text{ V to }5.5\text{ V}$ or $V_{reg(3.3)} = 3\text{ V to }3.6\text{ V}$, $V_{CC(I/O)} = 1.65\text{ V to }3.6\text{ V}$, $V_{GND} = 0\text{ V}$, see Table 10 for valid voltage level combinations, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------|----------------------------|-----|-----|------|
| $t_{PLH(se)}$ | LOW to HIGH (see Figure 3) | | 18 | ns |
| $t_{PHL(se)}$ | HIGH to LOW (see Figure 3) | | 18 | |

(1) Test circuit, see Figure 13

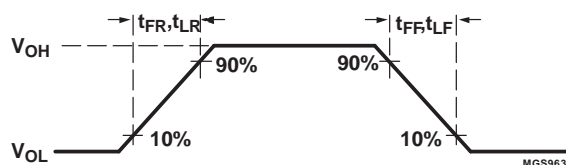


Figure 1. Rise and Fall Times

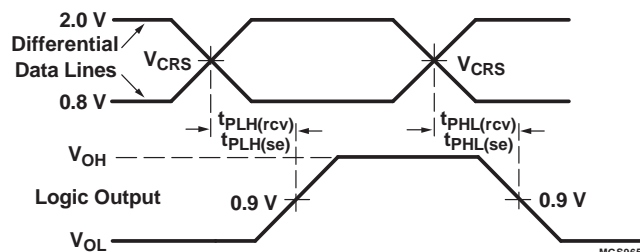


Figure 3. D+, D– to RCV, VP, VM

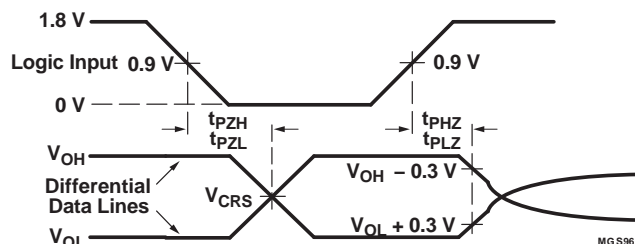


Figure 2. \overline{OE} to D+, D–

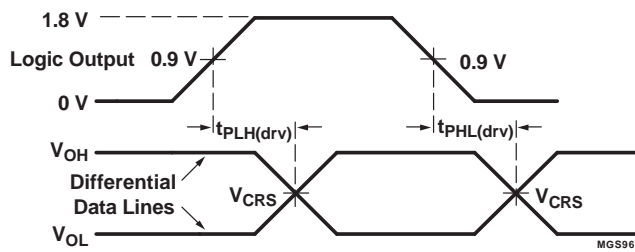


Figure 4. VO/VPO, FSE0/VMO to D+, D–

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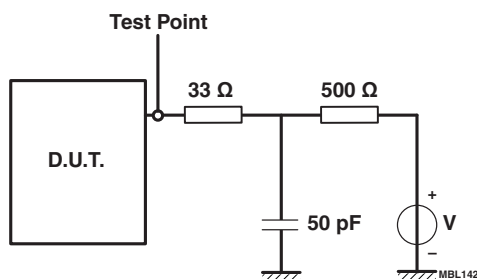


Figure 5. Load for Enable and Disable Times

- A. $V = 0\text{ V}$ for t_{PZH} , t_{PHZ}
- B. $V = V_{\text{reg}(3.3)}$ for t_{PZL} , t_{PLZ}

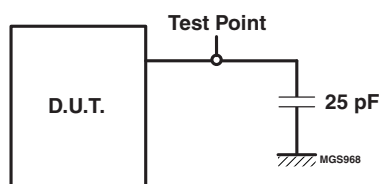


Figure 6. Load for VM, VP, and RCV

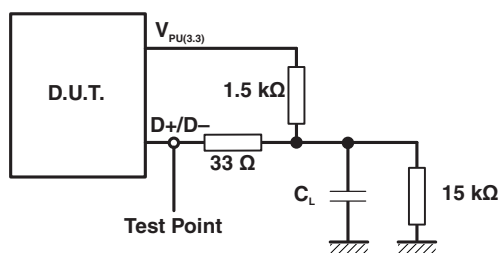


Figure 7. Load for D+, D-

- A. Full-speed mode: connected to D+
- B. Low-speed mode: Connected to D-
- C. Load capacitance:
 - $C_L = 50\text{ pF}$ or 125 pF (full-speed mode, minimum or maximum timing)
 - $C_L = 200\text{ pF}$ or 600 pF (low-speed mode, minimum or maximum timing)

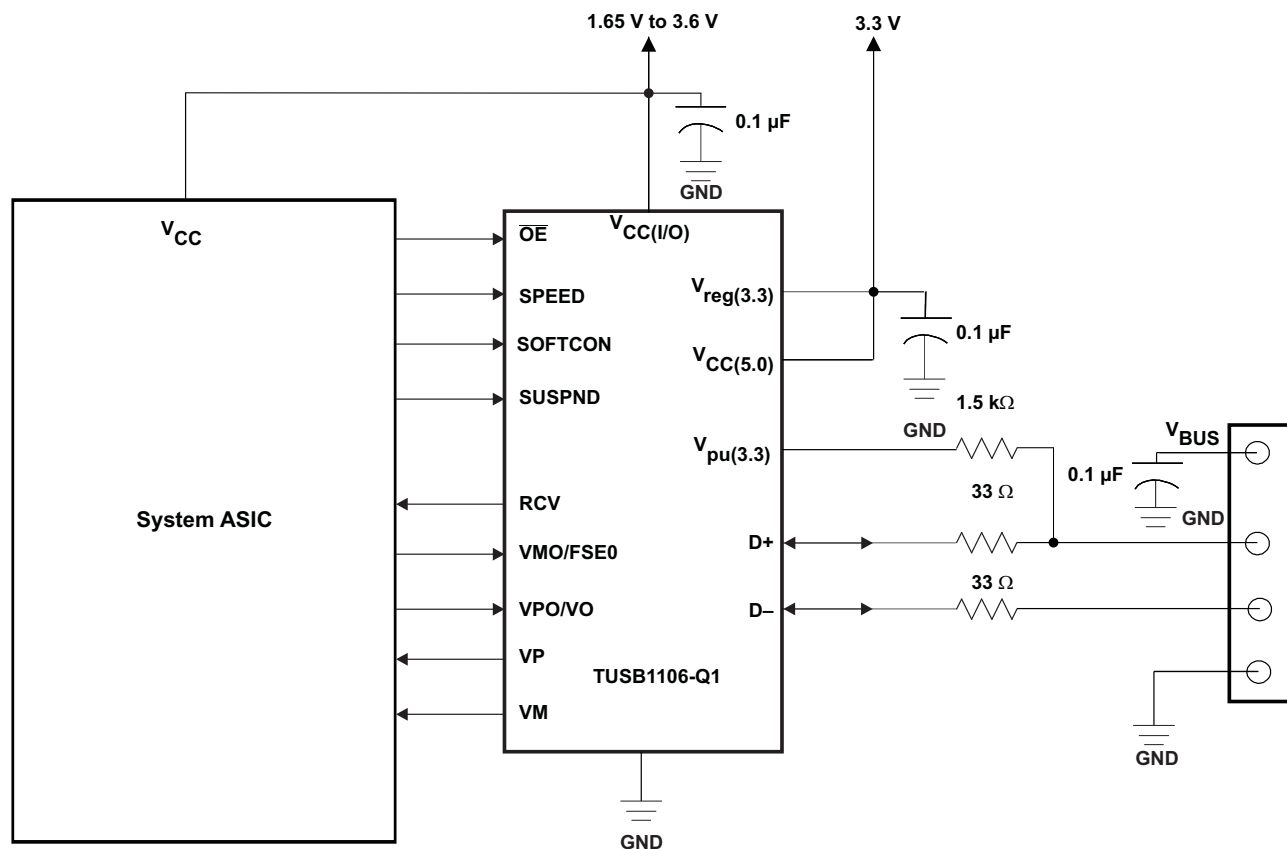


Figure 8. Peripheral-Side (Full-Speed) Regulator Bypass Mode

Peripheral-Side (Full-Speed) Regulator Bypass Mode

This mode is applicable when there is a 3.3-V supply already available on the board. The V_{BUS} pin of the USB connector, if left unused at the peripheral side, should be terminated with a 0.1- μ F capacitor. While operating at full speed, the 1.5-k Ω resistor must be connected between the D+ line and $V_{PU(3.3)}$ or an external 3.3-V supply. When the $V_{CC(5.0)}$ and the $V_{reg(3.3)}$ are connected together, the device operates at regulator bypass mode. This enables power savings since the regulator is turned off.

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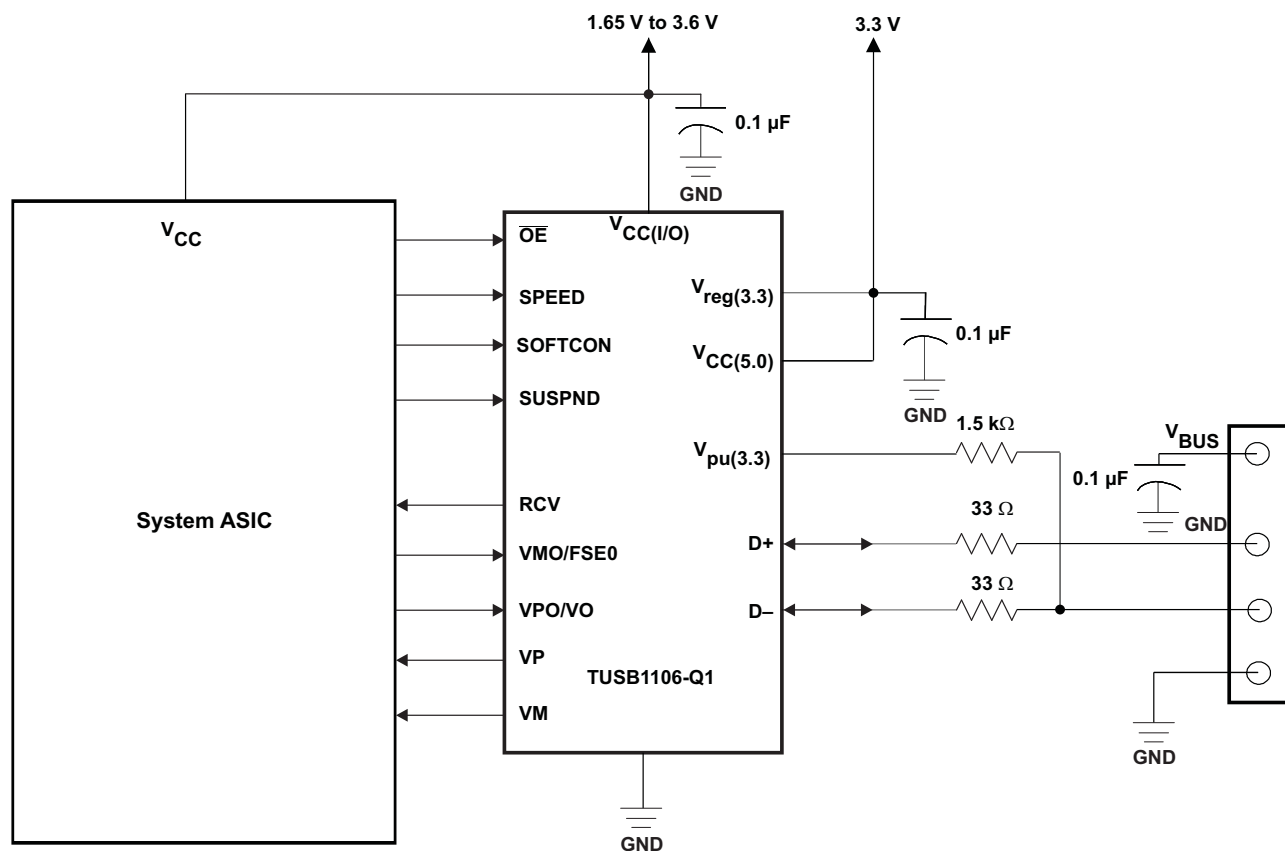


Figure 9. Peripheral-Side (Low-Speed) Regulator Bypass Mode

Peripheral-Side (Low-Speed) Regulator Bypass Mode

This mode is applicable when there is a 3.3-V supply already available on the board. The V_{BUS} pin of the USB connector, if left unused at the peripheral side, should be terminated with a 0.1- μ F capacitor. While operating at low speed, the 1.5-k Ω resistor must to be connected between the D- line and $V_{PU(3.3)}$ or an external 3.3-V supply. When the $V_{CC(5.0)}$ and the $V_{reg(3.3)}$ are connected together, the device operates at regulator bypass mode. This enables power savings since the regulator is turned off.

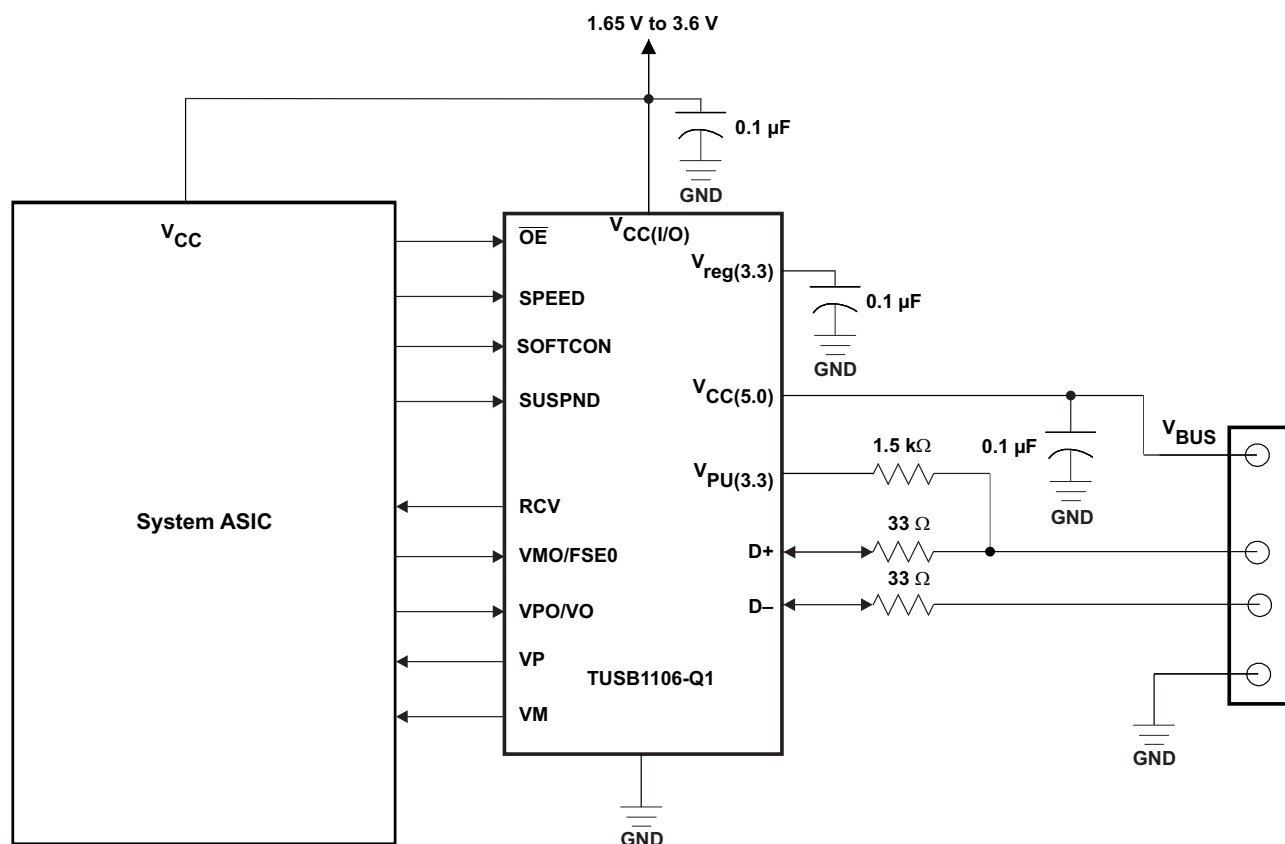


Figure 10. Peripheral-Side (Full-Speed) Internal Regulator Mode

Peripheral-Side (Full-Speed) Internal Regulator Mode

The USB side of the TUSB1106-Q1 can be powered from the V_{BUS} line directly if a 3.3-V supply is not present on board. In this case, the internal regulator can be used to provide the 3.3-V supply for USB signaling. The $V_{CC(5.0)}$ is connected to the V_{BUS} , which receives 5-V supply from the host, and generates the 3.3-V output at the $V_{reg(3.3)}$ pin. In this mode, it is important that both $V_{CC(5.0)}$ and $V_{reg(3.3)}$ pins have individual bypass capacitors in the range of 0.1 μ F. Powering $V_{CC(5.0)}$ through the V_{BUS} port of the USB connector realizes significant power saving for portable applications, such as cell phones, PDAs, etc. In this operating mode, the $I_{CC(5.0)}$ current is fed from the host. The USB-side power consumption, $I_{CC(5.0)}$ is 4 mA (with the regulator active), as opposed to logic-side $I_{CC(I/O)}$ of 1 mA under full-speed operation. While operating at full speed, the 1.5-k Ω resistor must be connected between the D+ line and the $V_{PU(3.3)}$ or an external 3.3-V supply.

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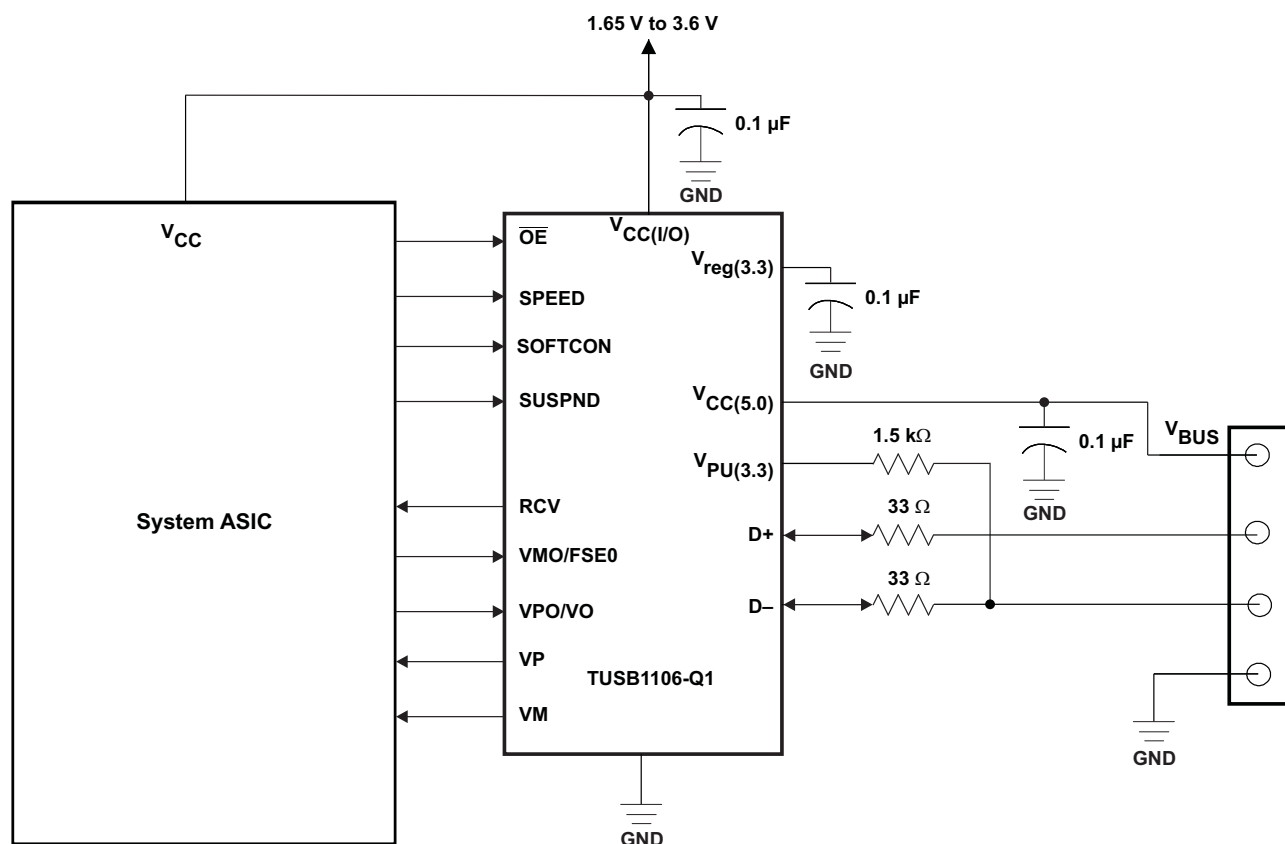


Figure 11. Peripheral-Side (Low-Speed) Internal Regulator Mode

Peripheral-Side (Low-Speed) Internal Regulator Mode

The USB side of the TUSB1106-Q1 can be powered from the V_{BUS} line directly if a 3.3-V supply is not present on board. In this case, the internal regulator can be used to provide the 3.3-V supply for the USB signaling. The $V_{CC(5.0)}$ is connected to the V_{BUS} , which receives 5-V supply from the host, and generates the 3.3-V output at the $V_{reg(3.3)}$ pin. In this mode, it is important that both $V_{CC(5.0)}$ and $V_{reg(3.3)}$ pins have individual bypass capacitors in the range of 0.1 μ F. Powering $V_{CC(5.0)}$ through the V_{BUS} port of the USB connector realizes significant power saving for portable applications, such as cell phones, PDAs, etc. In this operating mode, the $I_{CC(5.0)}$ current is fed from the host side. The USB-side power consumption, $I_{CC(5.0)}$ is 4 mA (with the regulator active), as opposed to logic-side $I_{CC(I/O)}$ of 1 mA under full-speed operation. While operating at low speed, the 1.5-k Ω resistor must be connected between the D- line and the $V_{PU(3.3)}$ or an external 3.3-V supply.

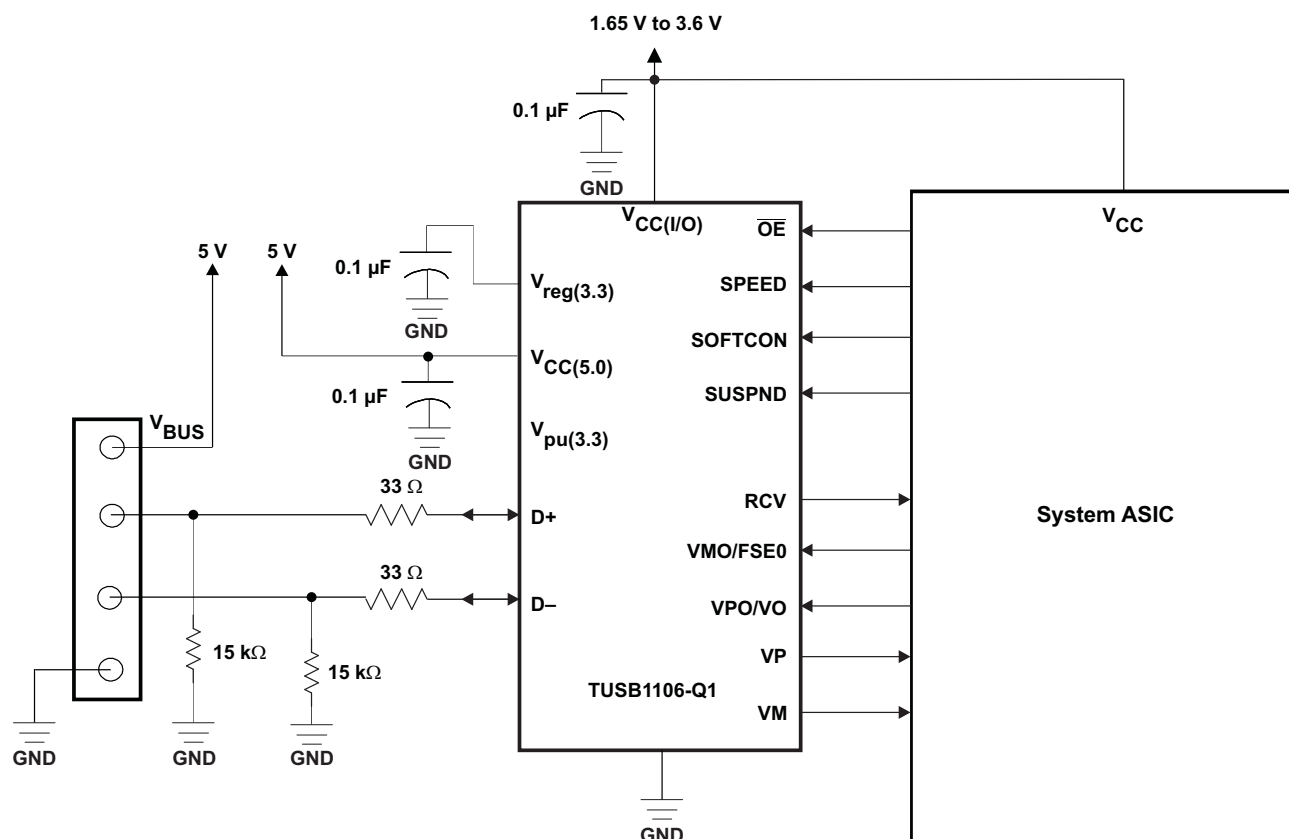


Figure 12. Host Side ($V_{CC(5.0)}$ Supplied From V_{BUS} Pin)

Host Side ($V_{CC(5.0)}$ Supplied From V_{BUS} Pin)

If there is no 3.3-V supply on board, an external 5-V supply can support the USB-side power needs. When the $V_{CC(5.0)}$ is connected to an external 5-V supply, the on-chip regulator generates the 3.3-V internal supply rail, which is used to drive the USB signaling levels at the USB side of the TUSB1106-Q1. The logic-side I/Os can operate at any voltage range from 1.65 V to 3.6 V.

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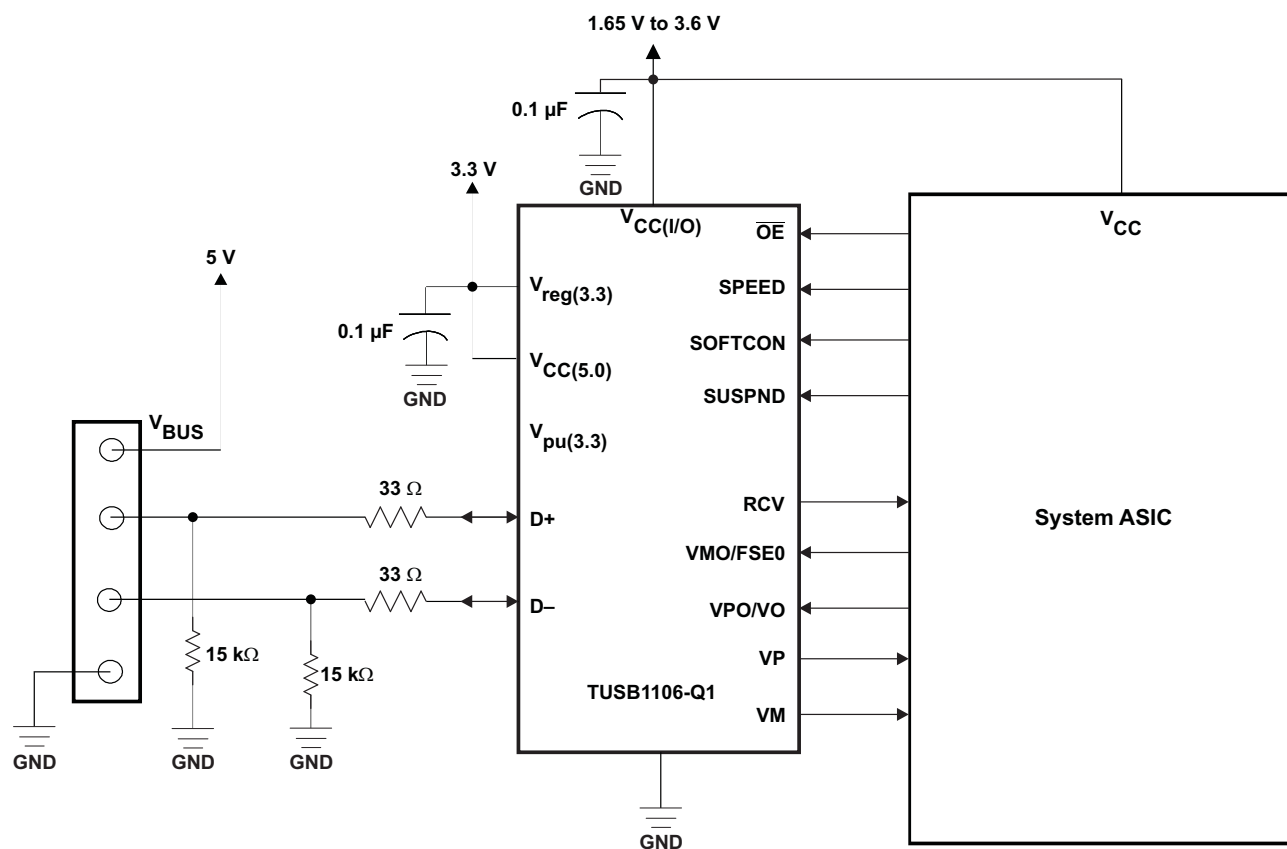


Figure 13. Host-Side (3.3-V Supply Present) Internal Regulator Bypass Mode

Host-Side (3.3-V Supply Present) Internal Regulator Bypass Mode

If a 3.3-V supply supports the USB-side power, $V_{CC(5.0)}$ and $V_{reg(3.3)}$ must be tied together and connected to a 3.3-V supply. It also makes the regulator inactive.



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Datasheet of TUSB1106IPWRQ1 - IC SRL BUS TXRX UNVRSL 16TSSOP

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PACKAGE OPTION ADDENDUM

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11-Apr-2013

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TUSB1106IPWRQ1 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TU1106I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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Datasheet of TUSB1106IPWRQ1 - IC SRL BUS TXRX UNVRSL 16TSSOP

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PACKAGE OPTION ADDENDUM

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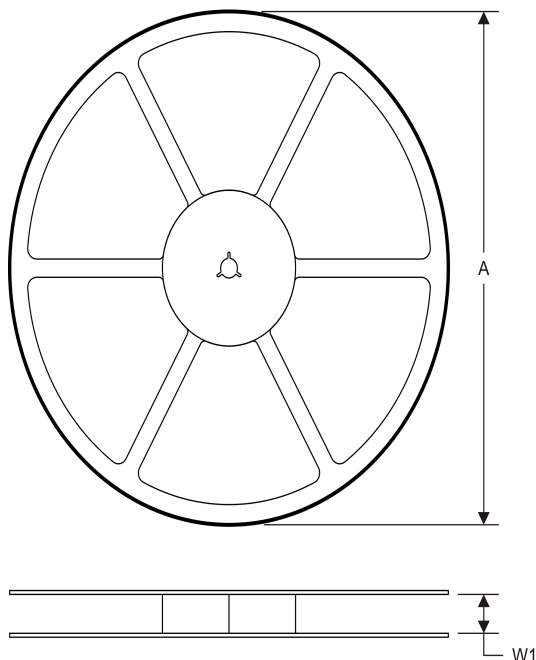
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

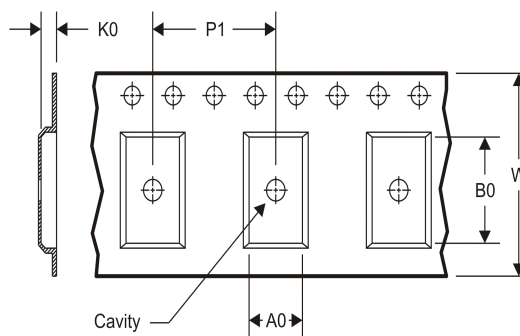
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



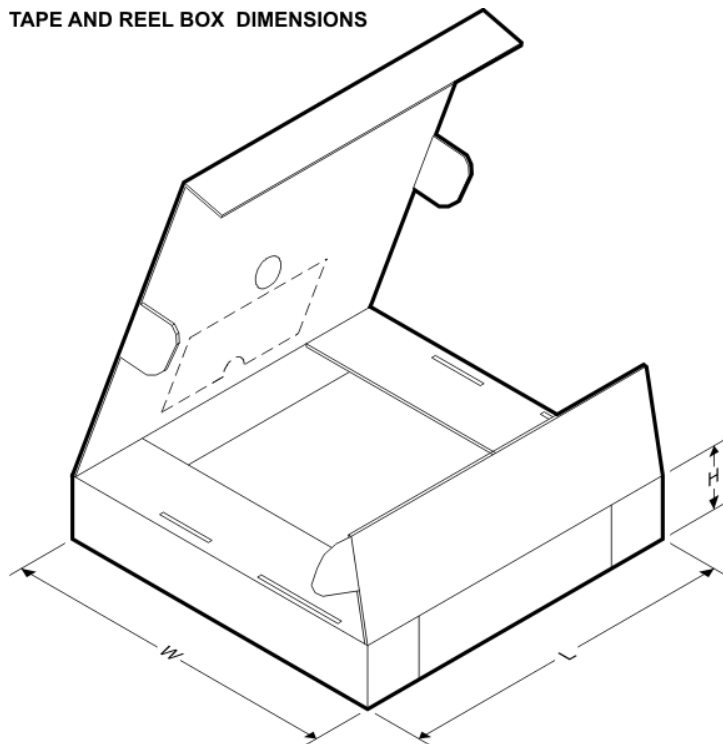
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TUSB1106IPWRQ1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



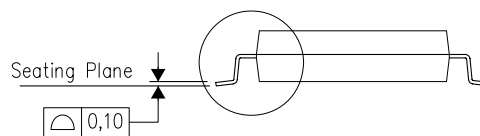
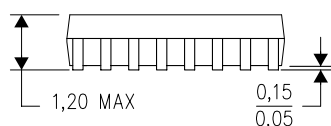
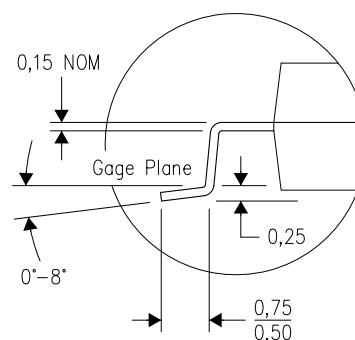
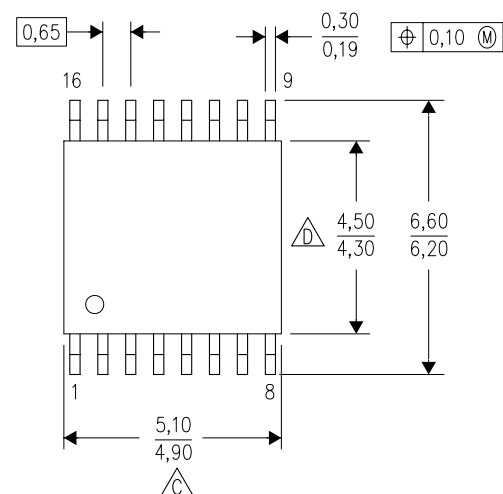
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TUSB1106IPWRQ1 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |



MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



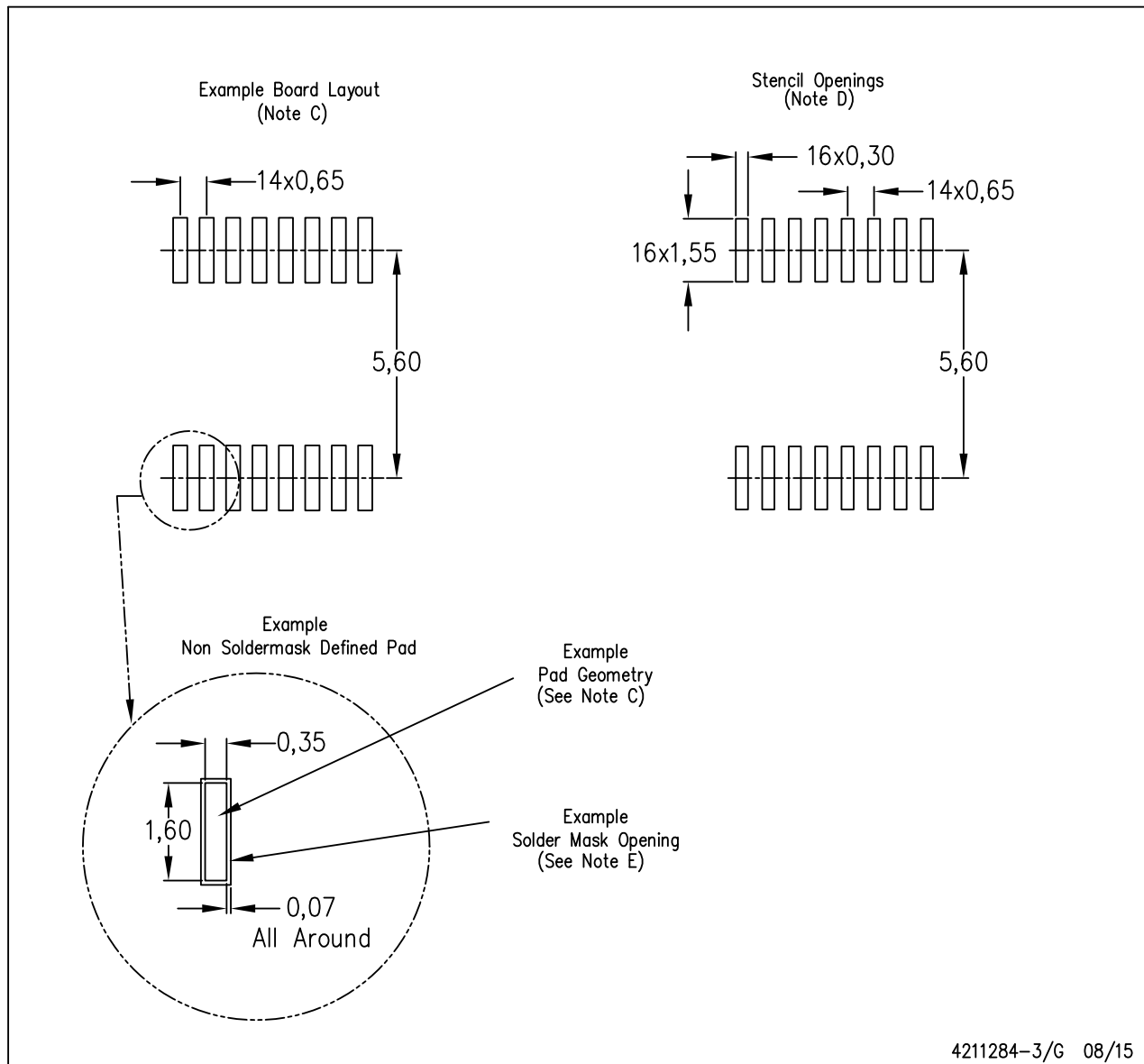
4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

LAND PATTERN DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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