

## Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Texas Instruments](#)  
[SN74SSQEC32882ZALR](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

## 28-Bit to 56-Bit Registered Buffer With Address Parity Test One Pair to Four Pair Differential Clock PLL Driver

Check for Samples: [SN74SSQEC32882](#)

### FEATURES

- JEDEC SSTE32882
- 1-to-2 Register Outputs and 1-to-4 Clock Pair Outputs Support Stacked DDR3 RDIMMs
- CKE Powerdown Mode for Optimized System Power Consumption
- 1.5V/1.35V/1.25V Phase Lock Loop Clock Driver for Buffering One Differential Clock Pair (CK and  $\overline{\text{CK}}$ ) and Distributing to Four Differential Outputs
- 1.5V/1.35V/1.25V CMOS Inputs
- Checks Parity on Command and Address

### (CS-Gated) Data Inputs

- Configurable Driver Strength
- Uses Internal Feedback Loop
- Optimized Power Consumption

### APPLICATIONS

- DDR3 Registered DIMMs up to DDR3-1866
- DDR3L Registered DIMMs up to DDR3L-1600
- DDR3U Registered DIMMs up to DDR3U-1333
- Single-, Dual- and Quad-Rank RDIMM

### DESCRIPTION

This 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for operation on DDR3 registered DIMMs with  $V_{DD}$  of 1.5 V, on DDR3L registered DIMMs with  $V_{DD}$  of 1.35 V and on DDR3U registered DIMMs with  $V_{DD}$  of 1.25 V.

All inputs are 1.5 V, 1.35V and 1.25 V CMOS compatible. All outputs are CMOS drivers optimized to drive DRAM signals on terminated traces in DDR3 RDIMM applications. The clock outputs  $Y_n$  and  $\overline{Y}_n$  and control net outputs  $DxCKEn$ ,  $DxCSn$  and  $DxODTn$  can be driven with a different strength and skew to optimize signal integrity, compensate for different loading and equalize signal travel speed.

The SN74SSQEC32882 has two basic modes of operation associated with the Quad Chip Select Enable ( $\overline{\text{QCSSEN}}$ ) input. When the  $\overline{\text{QCSSEN}}$  input pin is open (or pulled high), the component has two chip select inputs,  $\overline{\text{DCS0}}$  and  $\overline{\text{DCS1}}$ , and two copies of each chip select output,  $\overline{\text{QACS0}}$ ,  $\overline{\text{QACS1}}$ ,  $\overline{\text{QBCS0}}$  and  $\overline{\text{QBCS1}}$ . This is the "QuadCS disabled" mode. When the  $\overline{\text{QCSSEN}}$  input pin is pulled low, the component has four chip select inputs  $\overline{\text{DCS}}[3:0]$ , and four chip select outputs,  $\overline{\text{QCS}}[3:0]$ . This is the "QuadCS enabled" mode. Through the remainder of this specification,  $\overline{\text{DCS}}[n:0]$  will indicate all of the chip select inputs, where  $n=1$  for QuadCS disabled, and  $n=3$  for QuadCS enabled.  $\overline{\text{QxCS}}[n:0]$  will indicate all of the chip select outputs.

The device also supports a mode where a single device can be mounted on the back side of a DIMM. If MIRROR=HIGH, Input Bus Termination (IBT) has to stay enabled for all input signals in this case.

The SN74SSQEC32882 operates from a differential clock (CK and  $\overline{\text{CK}}$ ). Data are registered at the crossing of CK going HIGH, and  $\overline{\text{CK}}$  going LOW. This data could be either re-driven to the outputs or it could be used to access device internal control registers.

The input bus data integrity is protected by a parity function. All address and command input signals are added up and the last bit of the sum is compared to the parity signal delivered by the system at the input PAR\_IN one clock cycle later. If they do not match the device pulls the open drain output  $\overline{\text{ERROUT}}$  LOW. The control signals ( $\overline{\text{DCKE0}}$ ,  $\overline{\text{DCKE1}}$ ,  $\overline{\text{DODT0}}$ ,  $\overline{\text{DODT1}}$ ,  $\overline{\text{DCS}}[n:0]$ ) are not part of this computation.

The SN74SSQEC32882 implements different power saving mechanisms to reduce thermal power dissipation and to support system power down states. By disabling unused outputs the power consumption is further reduced.

The package is optimized to support high density DIMMs. By aligning input and output positions towards DIMM finger signal ordering and SDRAM ballout the device de-scrambles the DIMM traces allowing low cross talk design with low interconnect latency.

Edge controlled outputs reduce ringing and improve signal eye opening at the SDRAM inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## SN74SSQEC32882



SCAS920-PUB – NOVEMBER 2011

[www.ti.com](http://www.ti.com)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Table 1. ORDERING INFORMATION**

T <sub>CASE(max)</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE <sup>(2)</sup> PART NUMBER	TOP-SIDE MARKING
See <a href="#">Table 4</a>	176ZAL	Tape and Reel	SN74SSQEC32882ZALR	EC32882S

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).  
 (2) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## APPLICATION INFORMATION

### Vendor Specific SPD Content

SPD EEPROM on DDR3 RDIMMs has 3 vendor specific bytes for vendor and revision ID. This information can be sued by the system BIOS. The following table shows the correct values for SN74SSQEC32882.

**Table 2. Vendor specific SPD content for SN74SSQEC32882**

Byte	Value	Description
65	0x80	Vendor ID, part 1
66	0x97	Vendor ID, part 2
67	0x3D	Revision ID

### Application Reports

For additional Information on SN74SSQEC32882 DDR3 Register please review the following application reports:

- [DDR3 Register CMR programming](#)
- [DDR3 RDIMM SPD settings](#)
- [Yn phase shift on SN74SSQEA32882](#)
- [DDR3 Register IBT Measurement](#)

## ABSOLUTE MAXIMUM RATINGS

**Table 3. Absolute Maximum Ratings Over Operating Free-Air Temperature Range<sup>(1)</sup>**

PARAMETER		VALUE	UNIT
V <sub>DD</sub>	Supply voltage	–0.4 to +1.975	V
V <sub>I</sub>	Receiver input voltage	See <sup>(2)</sup> and <sup>(3)</sup>	–0.4 to V <sub>DD</sub> + 0.5
V <sub>REF</sub>	Reference voltage		–0.4 to V <sub>DD</sub> + 0.5
V <sub>O</sub>	Driver output voltage	See <sup>(2)</sup> and <sup>(3)</sup>	–0.4 to V <sub>DD</sub> + 0.5
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub>	–50
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub>	±50
I <sub>O</sub>	Continuous output current	0 < V <sub>O</sub> < V <sub>DD</sub>	±50
I <sub>CCC</sub>	Continuous current through each V <sub>DD</sub> or GND pin		±100
T <sub>stg</sub>	Storage temperature		–65 to +150

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 1.975 V maximum.

**Table 4. Case Temperature vs Speed Node**

PARAMETER		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	UNIT
T <sub>case(max)</sub>	Maximum case temperature <sup>(1)</sup>	+109	+108	+106	+103	+101	°C

- (1) The temperature values fit to JEDEC RAW cards A, B, and C. The user must keep T<sub>case</sub> below the specified values in order to keep the junction temperature below +125°C. Other combinations of features and termination resistors can require lower case temperature and extra cooling. These combinations depend on the specific application.

## SN74SSQEC32882

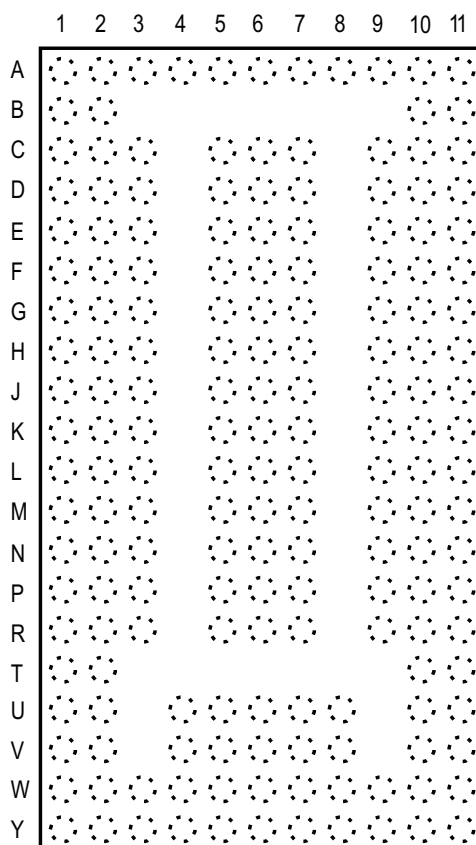
SCAS920-PUB –NOVEMBER 2011

[www.ti.com](http://www.ti.com)

### PACKAGE INFORMATION

#### Pinout Configuration

The package is a 8mm × 13.5mm 176-pin BGA with 0.65mm ball pitch in a 11 × 20 grid. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.



**Figure 1. Pinout Configuration**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74SSQEC32882ZALR	ACTIVE	NFBGA	ZAL	176	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-250C-168 HR	0 to 85	EC32882S	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

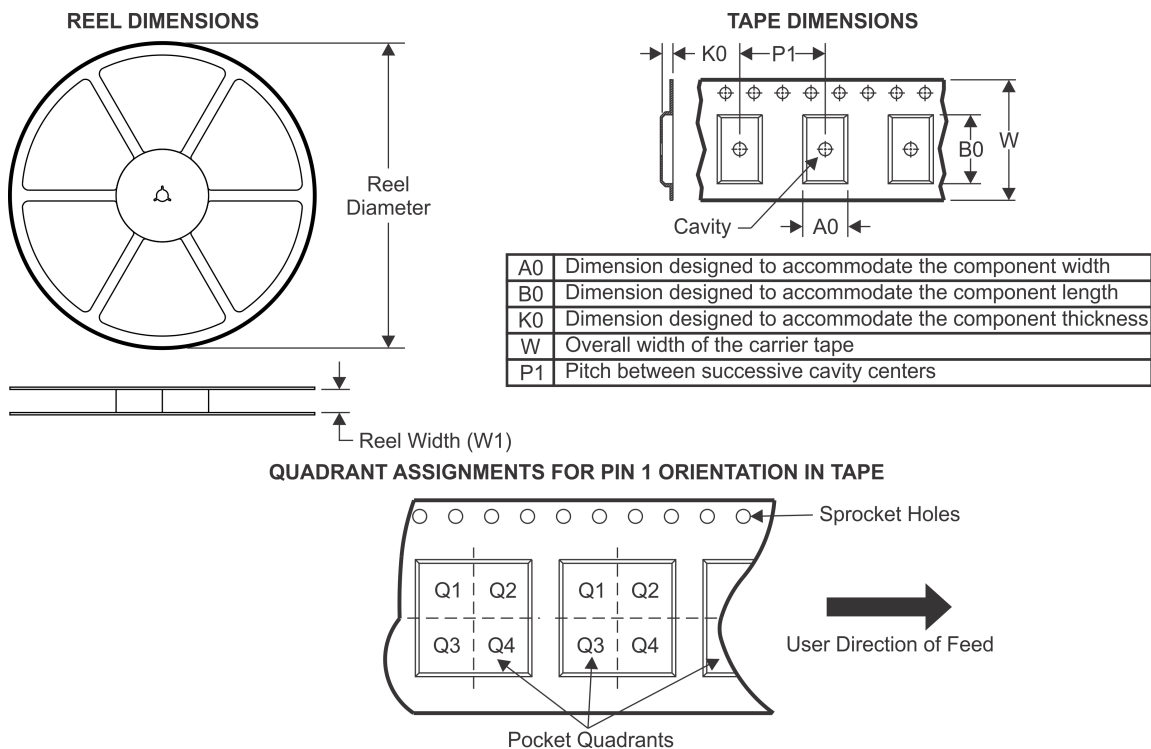
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

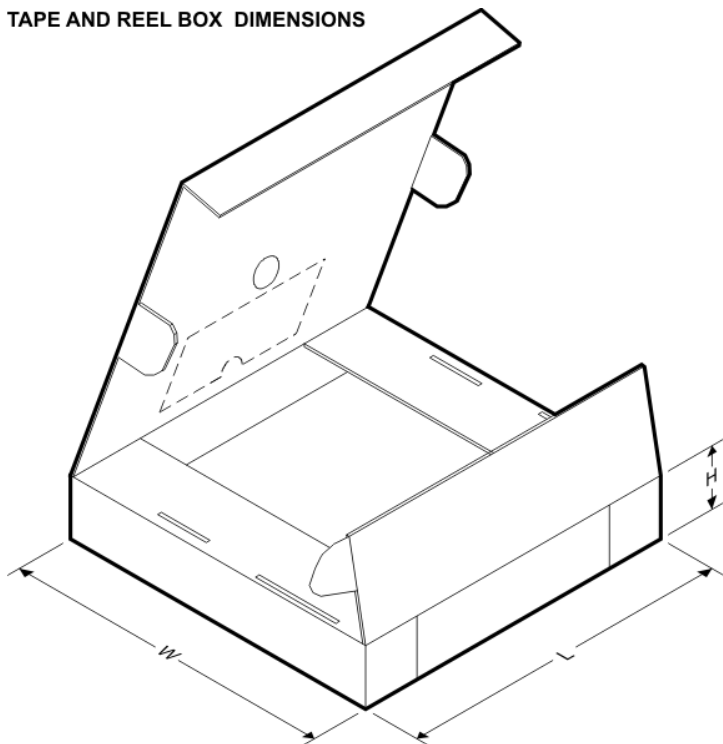
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSQEC32882ZALR	NFBGA	ZAL	176	2000	330.0	24.4	8.3	13.8	1.8	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



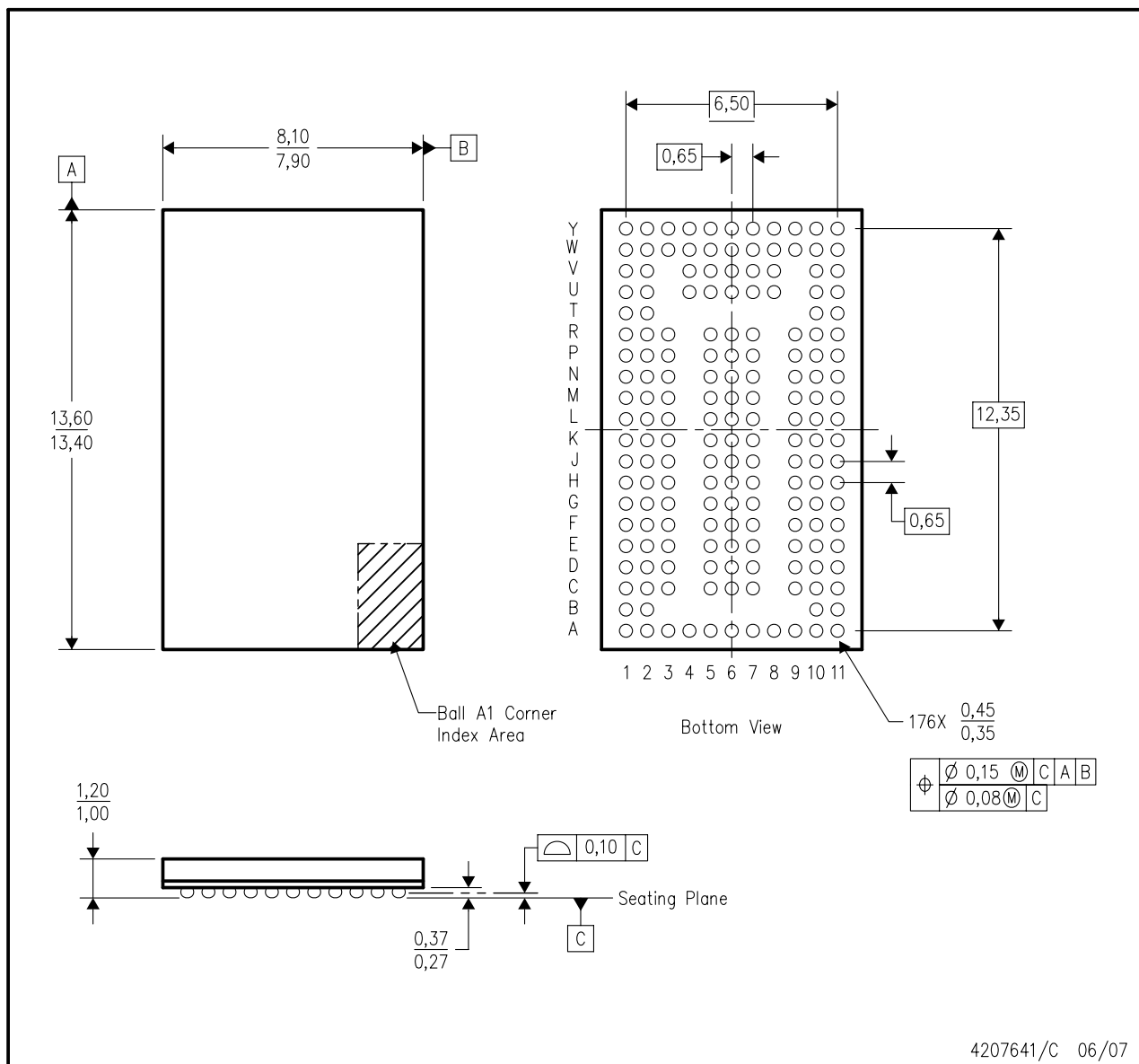
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSQEC32882ZALR	NFBGA	ZAL	176	2000	336.6	336.6	31.8

## MECHANICAL DATA

ZAL (R-PBGA-N176)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. This package is lead-free.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)