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STD8NM50N, STP8NM50N, STU8NM50N

N-channel 500 V, 0.73 Ω typ., 5 A MDmesh™II Power MOSFET in DPAK, TO-220 and IPAK packages

Datasheet — production data

Features

Order codes	$V_{DSS}@T_{JMAX}$	$R_{DS(on)max.}$	I_D
STD8NM50N STP8NM50N STU8NM50N	550 V	< 0.79 Ω	5 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

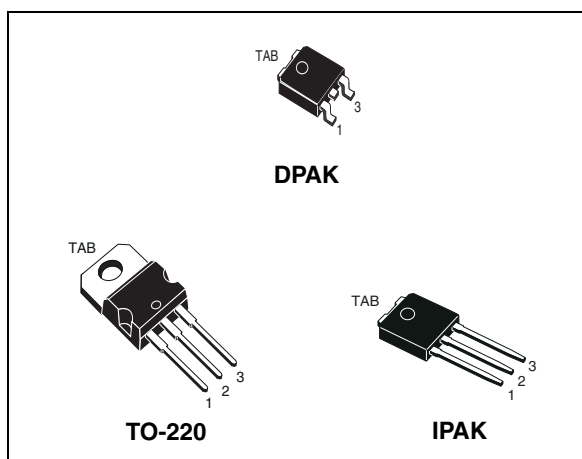


Figure 1. Internal schematic diagram

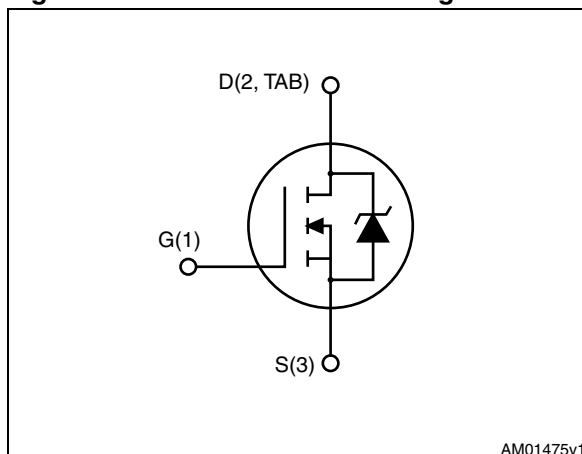


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STD8NM50N	8NM50N	DPAK	Tape and reel
STP8NM50N		TO-220	Tube
STU8NM50N		IPAK	

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Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	45	W
$dv/dt^{(1)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. $I_{SD} \leq 7\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$, $V_{DS} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	IPAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case max	2.78			$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max		100	62.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50			$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose		300		$^\circ\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	140	mJ

Electrical characteristics

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2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 500\text{ V}$ $V_{DS} = 500\text{ V}, T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		0.73	0.79	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	364 33 1.2	-	pF pF pF
$C_{oss(eq)}^{(1)}$	Equivalent output capacitance time related	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0$	-	147.5	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	5.4	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400\text{ V}, I_D = 5\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 16)	-	14 3 7	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

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Electrical characteristics

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15)		7		ns	
t_r	Rise time			4.4		ns	
$t_{d(off)}$	Turn-off-delay time				25		ns
t_f	Fall time				8.8		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 20)		187		ns
Q_{rr}	Reverse recovery charge			1.3		μC
I_{RRM}	Reverse recovery current			14		A
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 20)		224		ns
Q_{rr}	Reverse recovery charge			1.5		μC
I_{RRM}	Reverse recovery current			13		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Electrical characteristics

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAK

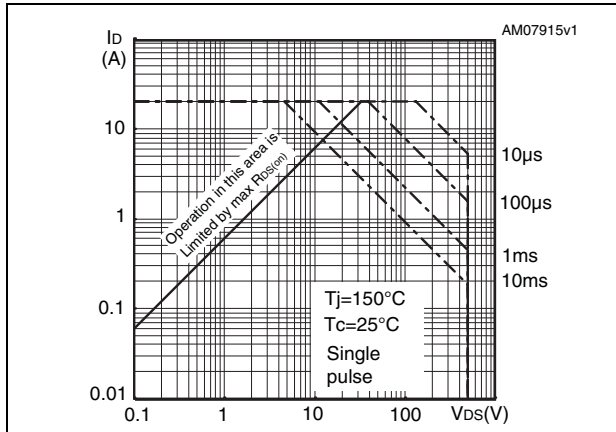


Figure 3. Thermal impedance for DPAK and IPAK

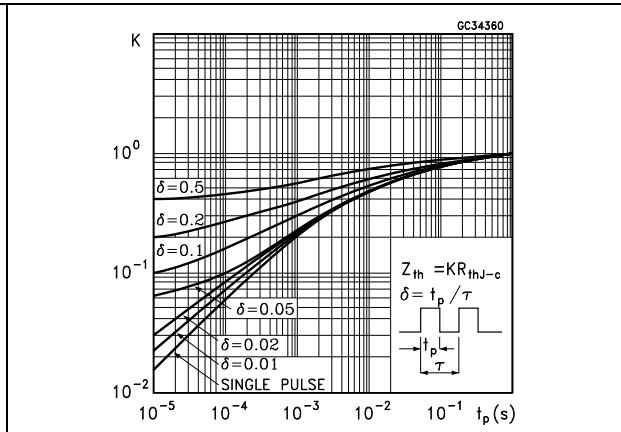


Figure 4. Safe operating area for TO-220

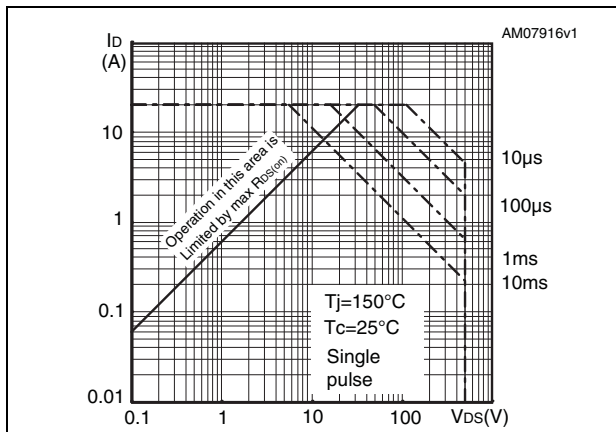


Figure 5. Thermal impedance for TO-220

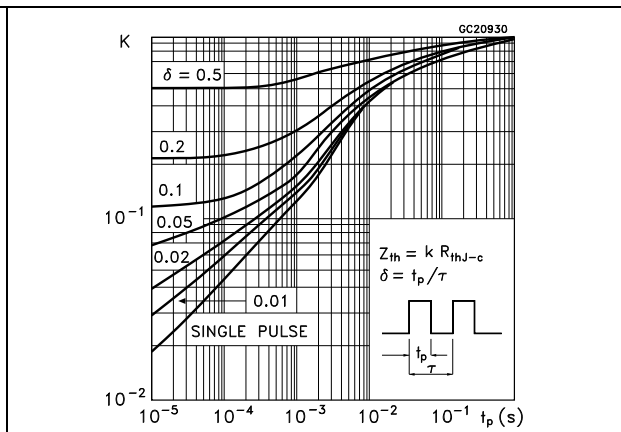


Figure 6. Output characteristics

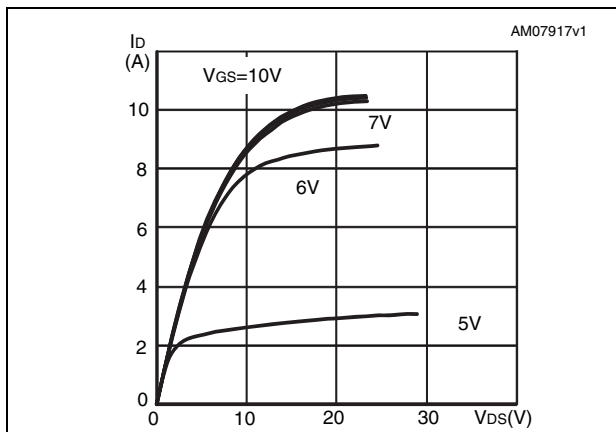
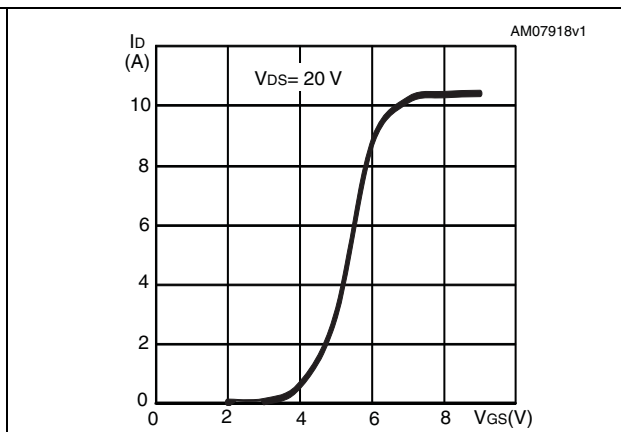


Figure 7. Transfer characteristics



STD8NM50N, STP8NM50N, STU8NM50N

Electrical characteristics

Figure 8. Static drain-source on resistance

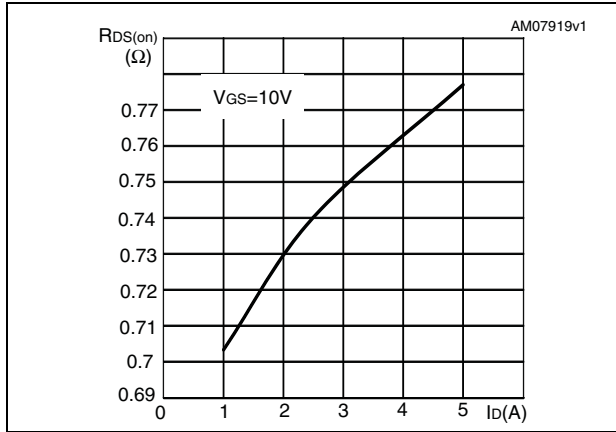


Figure 9. Gate charge vs gate-source voltage

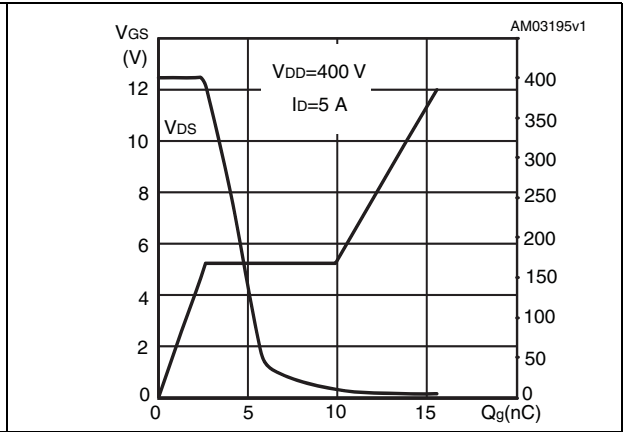


Figure 10. Capacitance variations

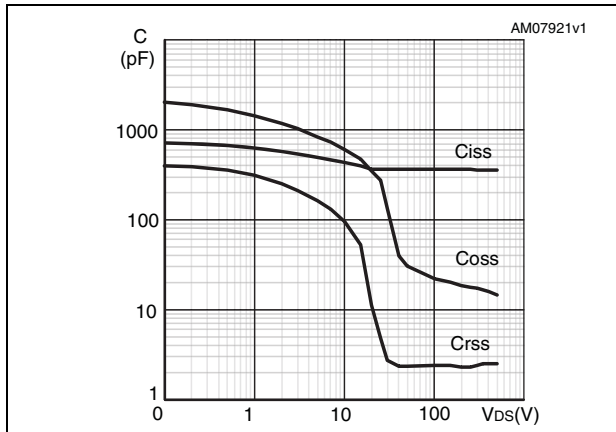


Figure 11. Output capacitance stored energy

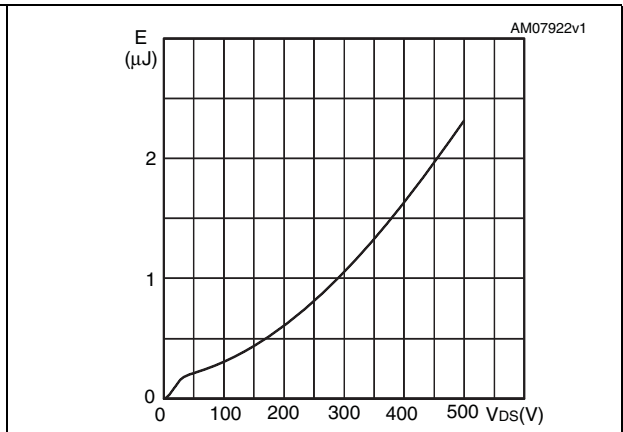


Figure 12. Normalized gate threshold voltage vs temperature

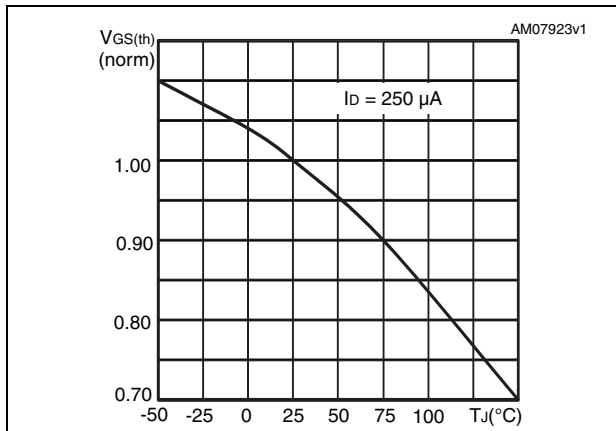
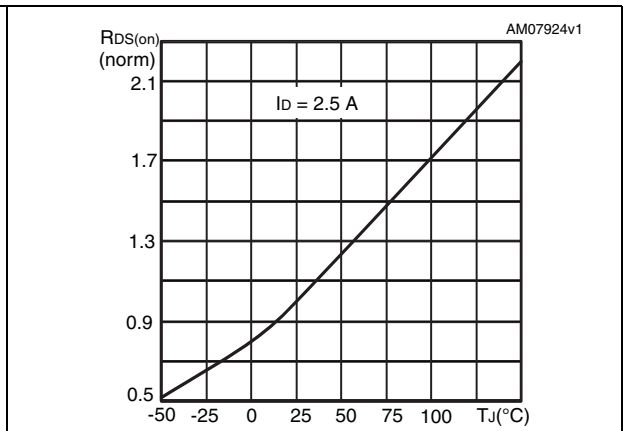


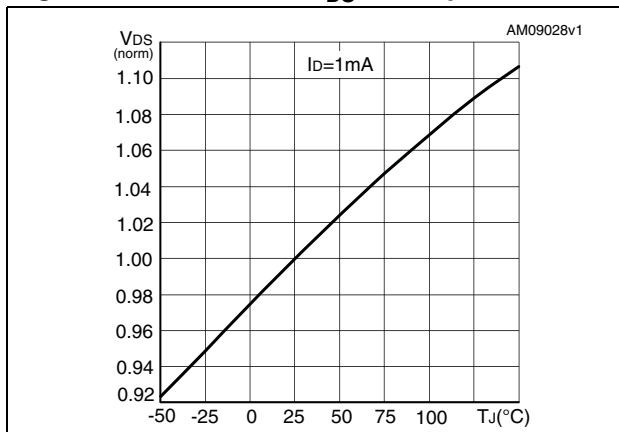
Figure 13. Normalized on resistance vs temperature



Electrical characteristics

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Figure 14. Normalized V_{DS} vs temperature



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Test circuits

3 Test circuits

Figure 15. Switching times test circuit for resistive load

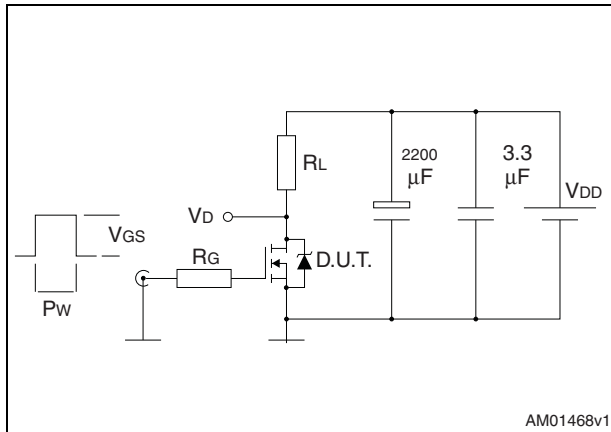


Figure 16. Gate charge test circuit

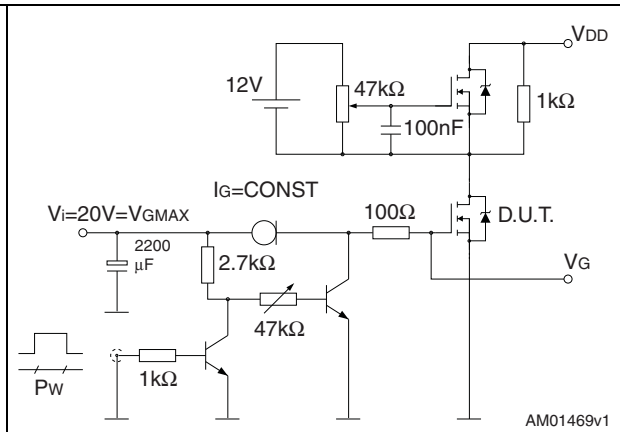


Figure 17. Test circuit for inductive load switching and diode recovery times

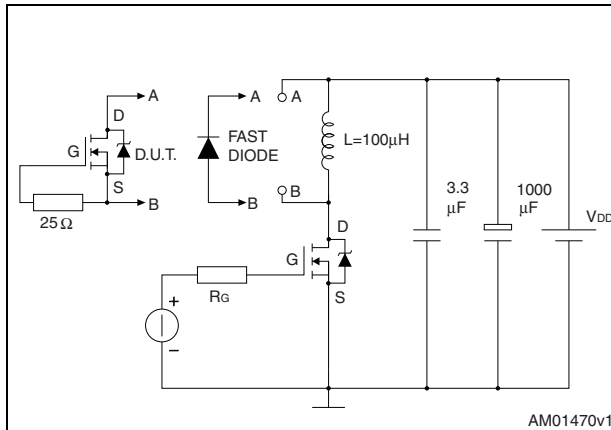


Figure 18. Unclamped inductive load test circuit

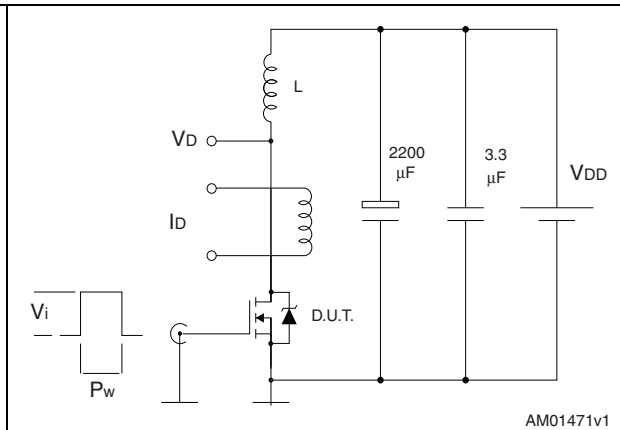


Figure 19. Unclamped inductive waveform

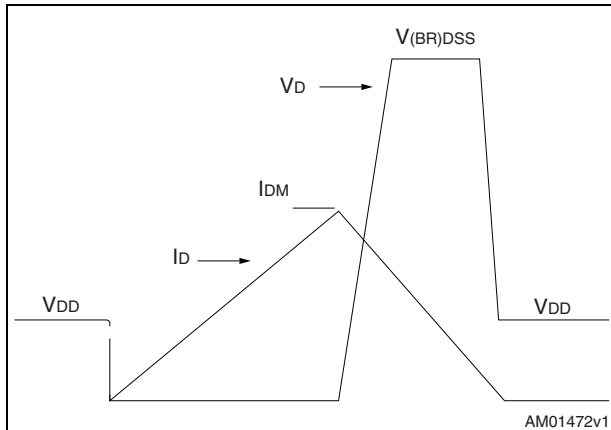
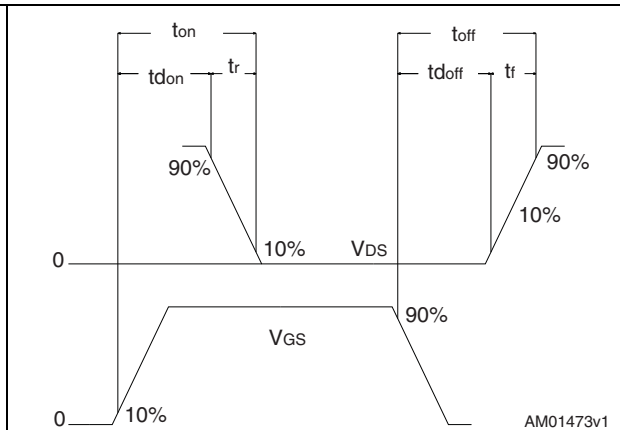


Figure 20. Switching time waveform



Package mechanical data
STD8NM50N, STP8NM50N, STU8NM50N

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

STD8NM50N, STP8NM50N, STU8NM50N

Package mechanical data

Figure 21. DPAK (TO-252) drawing

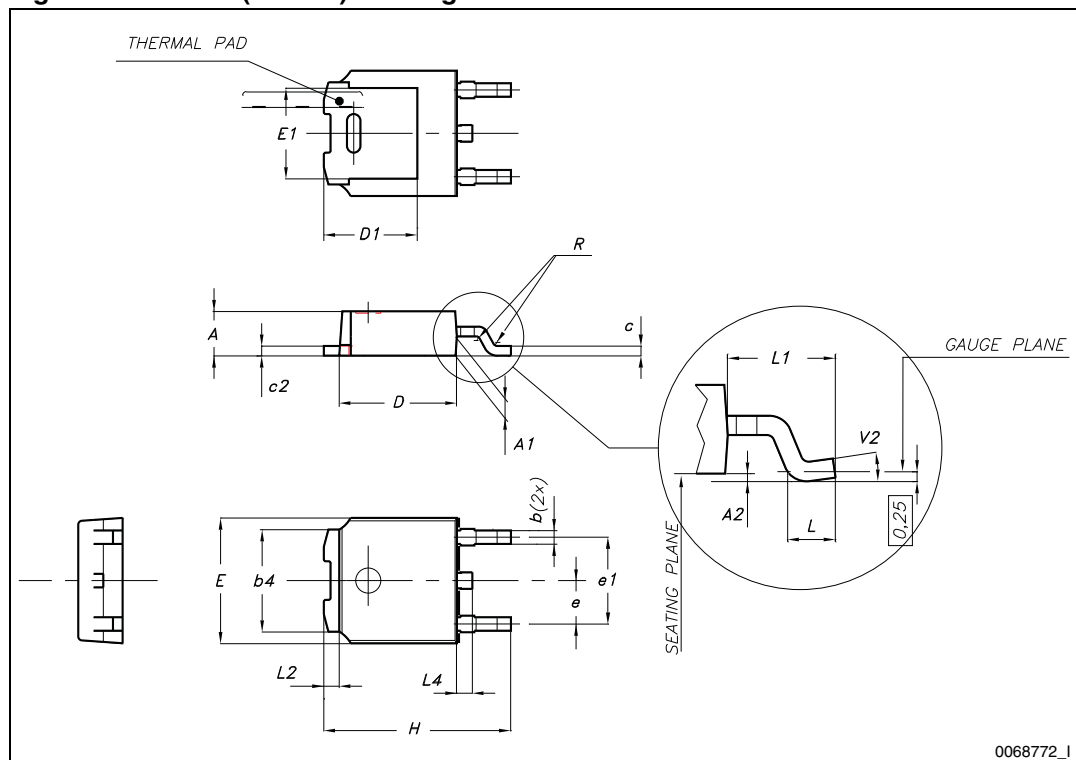
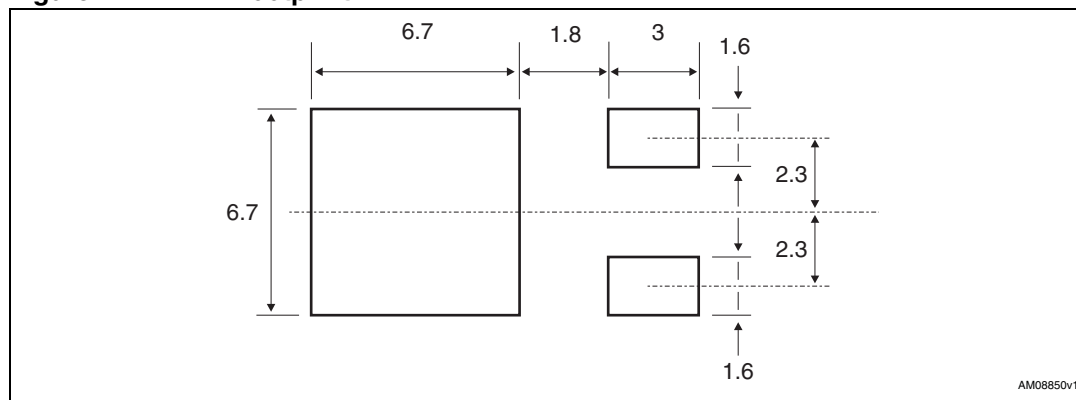


Figure 22. DPAK footprint^(a)



a. All dimension are in millimeters

Package mechanical data

STD8NM50N, STP8NM50N, STU8NM50N

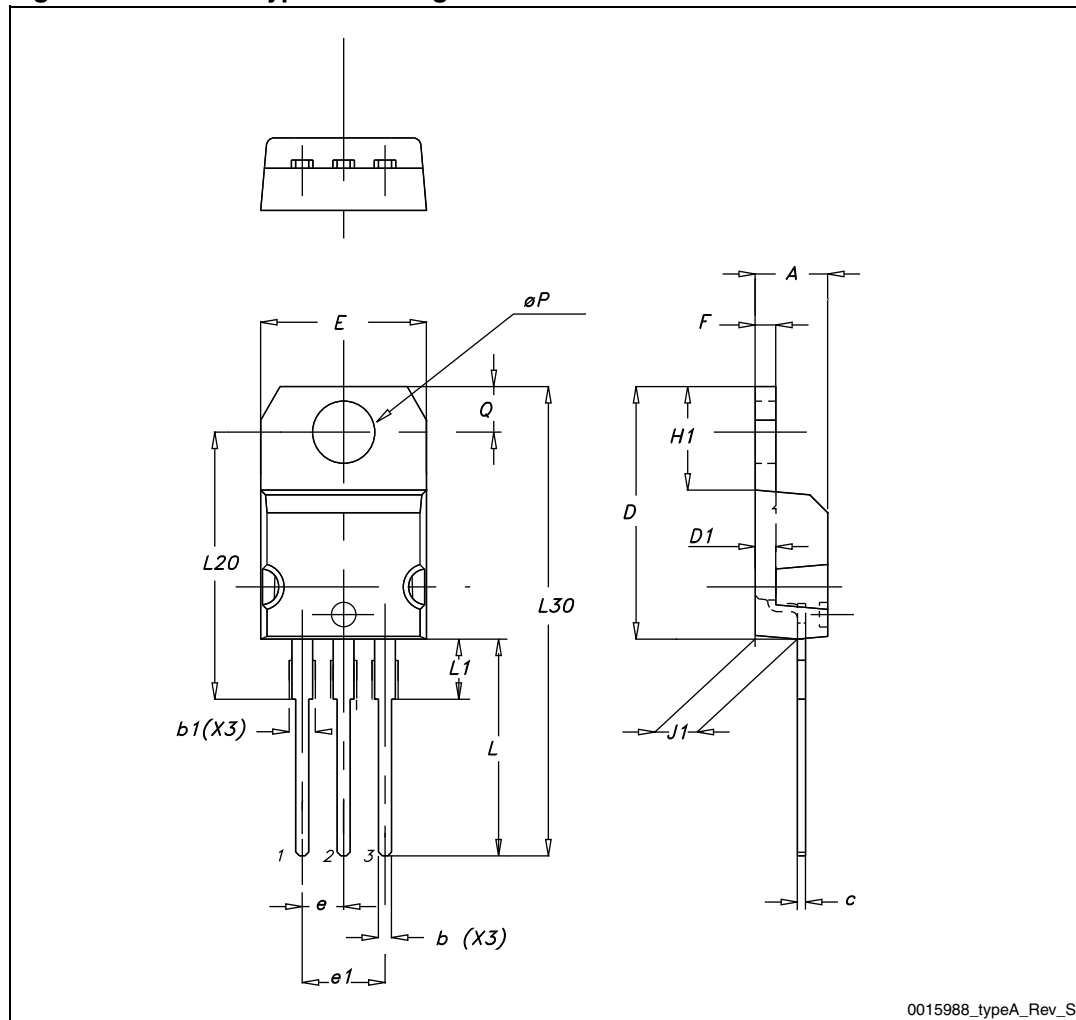
Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

STD8NM50N, STP8NM50N, STU8NM50N

Package mechanical data

Figure 23. TO-220 type A drawing



Package mechanical data

STD8NM50N, STP8NM50N, STU8NM50N

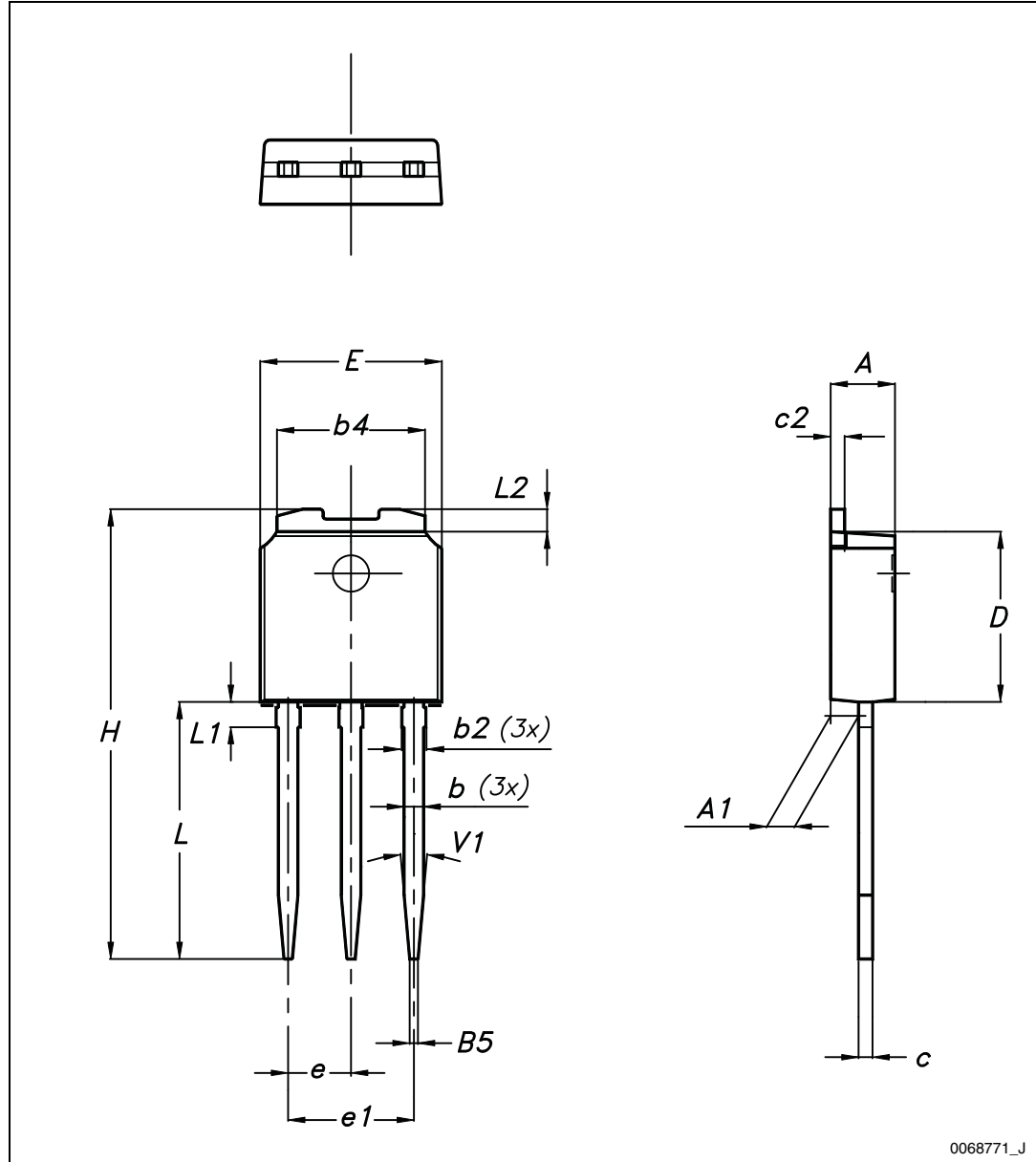
Table 11. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

STD8NM50N, STP8NM50N, STU8NM50N

Package mechanical data

Figure 24. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

STD8NM50N, STP8NM50N, STU8NM50N

Packaging mechanical data

Figure 25. Tape for DPAK (TO-252)

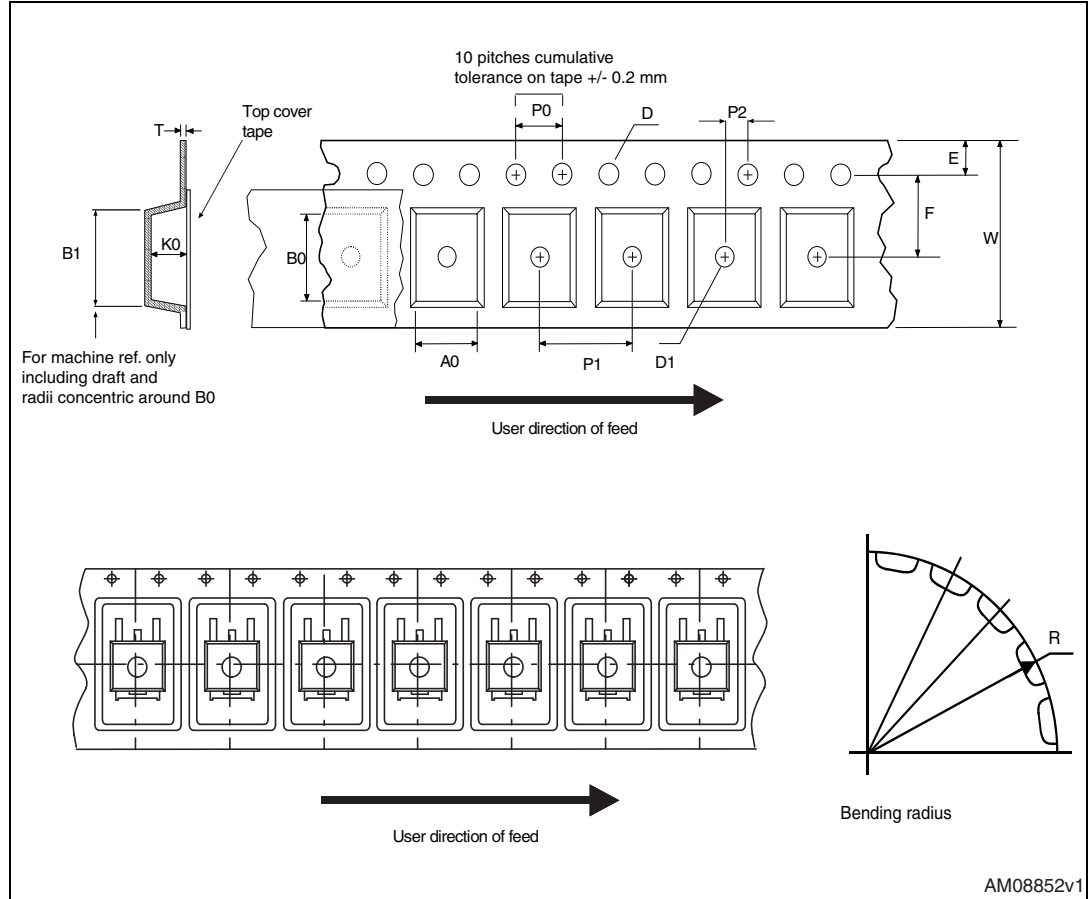
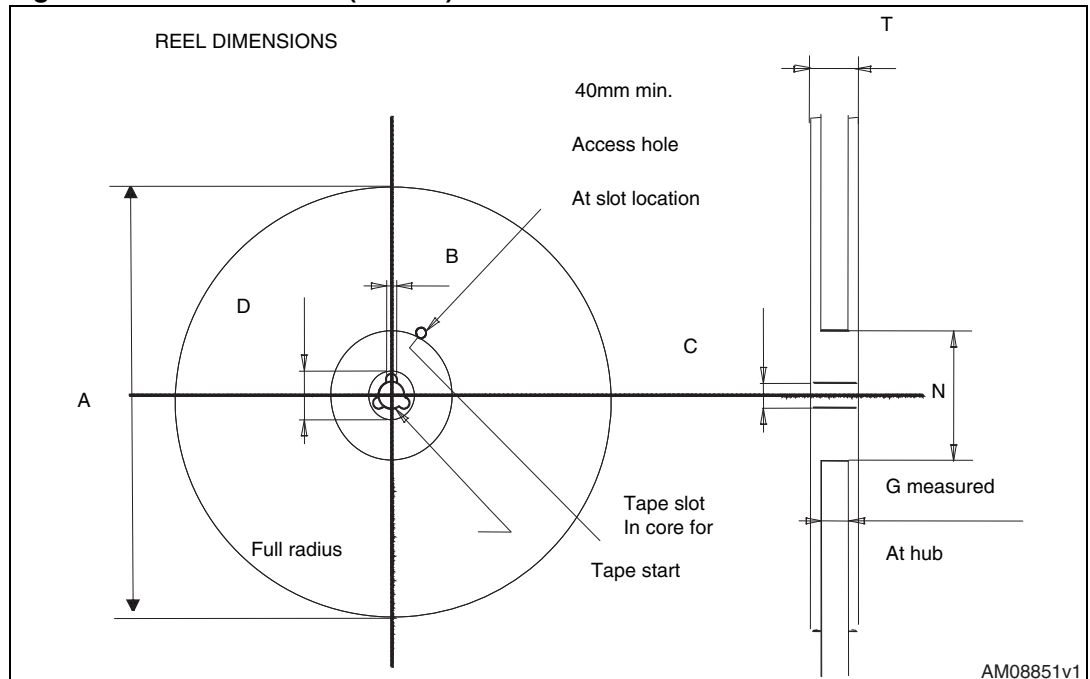


Figure 26. Reel for DPAK (TO-252)



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
20-Apr-2010	1	First release.
03-Sep-2010	2	Document status promoted from preliminary data to datasheet. Inserted Section 2.1: Electrical characteristics (curves) . Corrected $R_{DS(on)}$ max value in: Features .
03-Feb-2011	3	Modified: Figure 4 . Modified: note 1 . Modified: Table 5 .
21-Oct-2011	4	Updated V_{DSS} (@Tjmax) in cover page. Updated Section 4: Package mechanical data . Minor text changes.
15-Nov-2011	5	The part number STP8NM50N has been moved to a separate datasheet.
13-Sep-2012	6	Figure 2 and Figure 4 have been modified. Section 4: Package mechanical data has been updated.

STD8NM50N, STP8NM50N, STU8NM50N

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