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ADS7808



SBAS018A – JANUARY 1992 – REVISED SEPTEMBER 2003

12-Bit 10 μ s Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

FEATURES

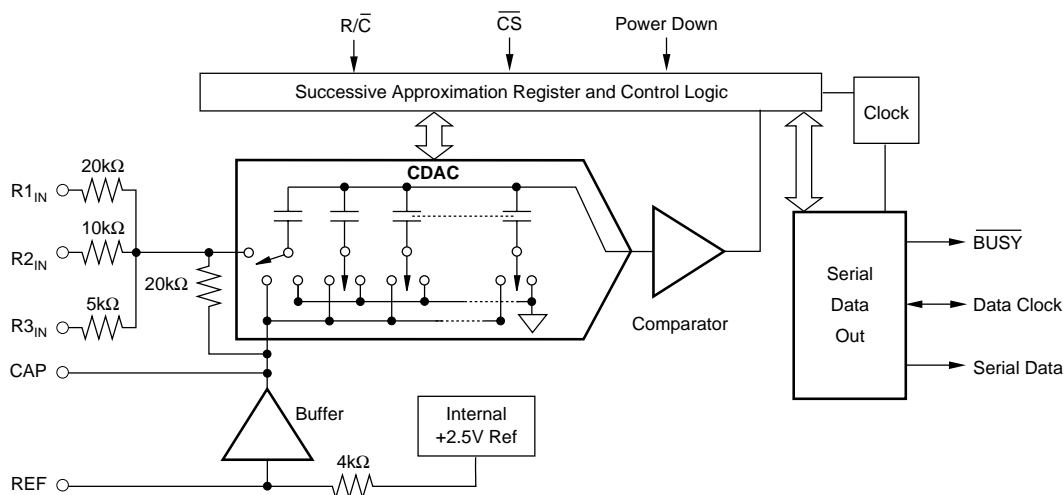
- 100kHz SAMPLING RATE
- 72dB SINAD WITH 45kHz INPUT
- $\pm 1/2$ LSB INL AND DNL
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7809
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 0.3" SO-20
- SIMPLE DSP INTERFACE

DESCRIPTION

The ADS7808 is a complete 12-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a 12-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7808 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7808 is specified at a 100kHz sampling rate, and specified over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ± 10 V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The ADS7808 is available in a 0.3" SO-20, fully specified for operation over the industrial -40°C to $+85^{\circ}\text{C}$ range.



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|---|---|
| Analog Inputs: R1 _{IN} | ±25V |
| R2 _{IN} | ±25V |
| R3 _{IN} | ±25V |
| CAP | V _{ANA} +0.3V to AGND2 -0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to V _{ANA} |
| Ground Voltage Differences: DGND, AGND2 | ±0.3V |
| V _{ANA} | 7V |
| V _{DIG} to V _{ANA} | +0.3 |
| V _{DIG} | 7V |
| Digital Inputs | -0.3V to V _{DIG} +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 700mW |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

| PRODUCT | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (DB) | PACKAGE-LEAD | PACKAGE DESIGNATOR ⁽¹⁾ | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|-----------|--|---|--------------|-----------------------------------|-----------------------------|-----------------|-----------------|---------------------------|
| ADS7808U | ±0.9 | 70 | SO-20 | DW | -40°C to +85°C | ADS7808U | ADS7808U | Tube, 38 |
| " | " | " | " | " | " | " | ADS7808U/1K | Tape and Reel, 1000 |
| ADS7808UB | ±0.45 | 72 | " | " | " | ADS7808UB | ADS7808UB | Tube, 38 |
| " | " | " | " | " | " | " | ADS7808UB/1K | Tape and Reel, 1000 |

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = -40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7808U | | | ADS7808UB | | | UNITS |
|--|--|----------------|---|---|-----------|-----|---|--|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| RESOLUTION | | | | 12 | | | * | Bits |
| ANALOG INPUT Voltage Ranges Impedance Capacitance | | | | ±10V, 0V to 5V, etc. (See Table I) See Table I | | | * | pF |
| THROUGHPUT SPEED Conversion Time Complete Cycle Throughput Rate | Acquire and Convert | 100 | 5.7 | 8 10 | * | * | * | µs µs kHz |
| DC ACCURACY Integral Linearity Error Differential Linearity Error No Missing Codes Transition Noise ⁽²⁾ Full Scale Error ^(3,4) Full Scale Error Drift Full Scale Error ^(3,4) Full Scale Error Drift Bipolar Zero Error ⁽³⁾ Bipolar Zero Error Drift Unipolar Zero Error ⁽³⁾ Unipolar Zero Error Drift Recovery to Rated Accuracy after Power Down Power Supply Sensitivity (V _{DIG} = V _{ANA} = V _D) | Ext. 2.5000V Ref Ext. 2.5000V Ref Bipolar Ranges Bipolar Ranges 0V to 10V Range 0V to 4V Range 0V to 5V Range Unipolar Ranges 1µF Capacitor to CAP +4.75V < V _D < +5.25V | | Specified 0.1 ±7 ±2 ±2 ±2 ±2 ±2 1 | ±0.9 ±0.9 ±0.5 ±0.5 ±10 ±5 ±3 ±3 ±0.5 | | * | ±0.45 ±0.45 ±0.25 ±0.25 * * * * * | LSB ⁽¹⁾ LSB % ppm/°C % ppm/°C mV ppm/°C mV mV ppm/°C ms LSB |
| AC ACCURACY Spurious-Free Dynamic Range Total Harmonic Distortion Signal-to-(Noise+Distortion) Signal-to-Noise Full-Power Bandwidth ⁽⁶⁾ | f _{IN} = 45kHz f _{IN} = 45kHz f _{IN} = 45kHz f _{IN} = 45kHz | 80 70 70 | 90 -90 73 73 250 | -80 | * | * | * | dB ⁽⁵⁾ dB dB dB kHz |

ELECTRICAL CHARACTERISTICS (Cont.)

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $f_S = 100\text{kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$, using internal reference and fixed resistors shown in Figure 4, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7808U | | | ADS7808UB | | | UNITS |
|---|---|---|-------|---------------------|-----------|-----|--------------------|------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SAMPLING DYNAMICS | | | | | | | | |
| Aperture Delay | FS Step | | 40 | | | * | | ns |
| Aperture Jitter | | Sufficient to meet AC specs | | | | * | | ns |
| Transient Response | | | | 2 | | | * | μs |
| Overvoltage Recovery ⁽⁷⁾ | | | 150 | | | * | | ns |
| REFERENCE | | | | | | | | |
| Internal Reference Voltage | No Load | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer) | | | 1 | | | * | | μA |
| External Reference Voltage Range for Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | μA |
| DIGITAL INPUTS | | | | | | | | |
| Logic Levels | $V_{\text{IL}} = 0\text{V}$ $V_{\text{IH}} = 5\text{V}$ | | | | | | | |
| V_{IL} | | -0.3 | | +0.8 | * | | * | V |
| $V_{\text{IH}}^{(8)}$ | | +2.0 | | $V_D + 0.3\text{V}$ | * | | * | V |
| I_{IL} | | | | ± 10 | | | * | μA |
| I_{IH} | | | | ± 10 | | | * | μA |
| DIGITAL OUTPUTS | | | | | | | | |
| Data Format | EXT/ $\overline{\text{INT}}$ LOW | Serial 12 bits | | | | | | |
| Data Coding | | Binary Two's Complement or Straight Binary | | | | | | |
| Pipeline Delay | | Conversion results only available after completed conversion. | | | | | | |
| Data Clock | | Selectable for internal or external data clock | | | | | | |
| Internal (Output Only When Transmitting Data) | EXT/ $\overline{\text{INT}}$ HIGH | | 2.3 | | | * | | MHz |
| External (Can Run Continually) | | 0.1 | | 10 | * | | * | MHz |
| V_{OL} | $I_{\text{SINK}} = 1.6\text{mA}$ | | | +0.4 | | | * | V |
| V_{OH} | $I_{\text{SOURCE}} = 500\mu\text{A}$ | +4 | | | * | | * | V |
| Leakage Current | High-Z State, $V_{\text{OUT}} = 0\text{V}$ to V_{DIG} | | | ± 5 | | | * | μA |
| Output Capacitance | High-Z State | | | 15 | | | 15 | pF |
| POWER SUPPLIES | | | | | | | | |
| Specified Performance | Must be $\leq V_{\text{ANA}}$ +4.75 | +4.75 | +5 | +5.25 | * | * | * | V |
| V_{DIG} | | +5 | +5.25 | * | * | * | * | V |
| V_{ANA} | | 0.3 | | | * | | mA | |
| I_{DIG} | | 16 | | | * | | mA | |
| I_{ANA} | $V_{\text{DIG}} = V_{\text{ANA}} = 5\text{V}$, $f_S = 100\text{kHz}$ | | | 100 | | | * | mW |
| Power Dissipation: PWRD LOW | | | 50 | | | * | | μW |
| Power Dissipation: PWRD HIGH | | | | | | | | |
| TEMPERATURE RANGE | | | | | | | | |
| Specified Performance | | -40 | | +85 | * | | * | $^\circ\text{C}$ |
| Derated Performance | | -55 | | +125 | * | | * | $^\circ\text{C}$ |
| Storage | | -65 | | +150 | * | | * | $^\circ\text{C}$ |
| Thermal Resistance (θ_{JA}) | | | | | | | | |
| SO | | 75 | | | * | | $^\circ\text{C/W}$ | |

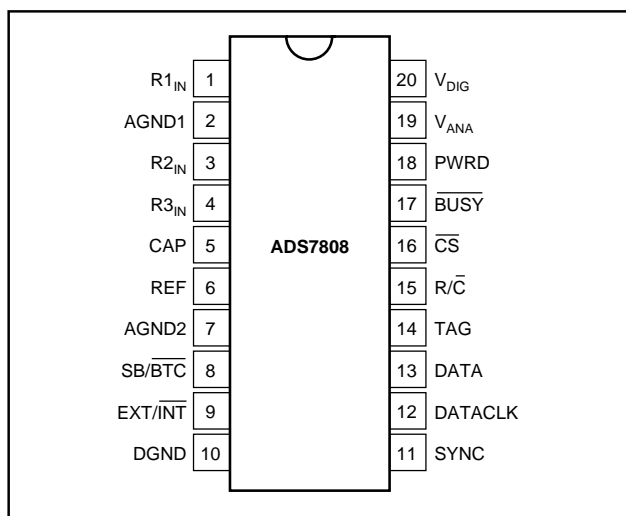
* Specifications same as ADS7808U.

NOTES: (1) LSB means Least Significant Bit. For the $\pm 10\text{V}$ input range, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale $\pm 10\text{V}$ input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to (Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) The minimum V_{IH} level for the DATACLK signal is 3V.

PIN ASSIGNMENTS

| PIN # | NAME | DESCRIPTION |
|-------|------------------|--|
| 1 | R1 _{IN} | Analog Input. See Table I and Figure 4 for input range connections. |
| 2 | AGND1 | Analog Ground. Used internally as ground reference point. Minimal current flow. |
| 3 | R2 _{IN} | Analog Input. See Table I and Figure 4 for input range connections. |
| 4 | R3 _{IN} | Analog Input. See Table I and Figure 4 for input range connections. |
| 5 | CAP | Reference Buffer Capacitor. 2.2μF Tantalum to ground. |
| 6 | REF | Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2μF Tantalum capacitor. |
| 7 | AGND2 | Analog Ground. |
| 8 | SB/BTC | Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's complement format. |
| 9 | EXT/INT | Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 12 clock pulses output on DATACLK. |
| 10 | DGND | Digital Ground. |
| 11 | SYNC | Sync Output. If EXT/INT is HIGH, either a rising edge on R/C with CS LOW or a falling edge on CS with R/C HIGH will output a pulse on SYNC synchronized to the external DATACLK. |
| 12 | DATACLK | Either an input or an output depending on the EXT/INT level. Output data will be synchronized to this clock. If EXT/INT is LOW, DATACLK will transmit 12 pulses after each conversion, and then remain LOW between conversions. |
| 13 | DATA | Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/BTC. In the external clock mode, after 12-bits of data, the ADS7808 will output the level input on TAG as long as CS is LOW and R/C is HIGH (see Figure 3.) If EXT/INT is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started. |
| 14 | TAG | Tag Input for use in external clock mode. If EXT/INT is HIGH, digital data input on TAG will be output on DATA with a delay of 12 DATACLK pulses as long as CS is LOW and R/C is HIGH. See Figure 3. |
| 15 | R/C | Read/Convert Input. With CS LOW, a falling edge on R/C puts the internal sample/hold into the hold state and starts a conversion. When EXT/INT is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/INT is HIGH, a rising edge on R/C with CS LOW, or a falling edge on CS with R/C HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion. |
| 16 | CS | Chip Select. Internally OR'ed with R/C. |
| 17 | BUSY | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. CS or R/C must be HIGH when BUSY rises, or another conversion will start without time for signal acquisition. |
| 18 | PWRD | Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register. |
| 19 | V _{ANA} | Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1μF ceramic and 10μF Tantalum capacitors. |
| 20 | V _{DIG} | Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V _{ANA} . |

PIN CONFIGURATION



| ANALOG INPUT RANGE | CONNECT R1 _{IN} VIA 200Ω TO | CONNECT R2 _{IN} VIA 100Ω TO | CONNECT R3 _{IN} TO | IMPEDANCE |
|--------------------|--------------------------------------|--------------------------------------|-----------------------------|-----------|
| ±10V | V _{IN} | AGND | CAP | 22.9kΩ |
| ±5V | AGND | V _{IN} | CAP | 13.3kΩ |
| ±3.33 | V _{IN} | V _{IN} | CAP | 10.7kΩ |
| 0V to 10V | AGND | V _{IN} | AGND | 13.3kΩ |
| 0V to 5V | AGND | AGND | V _{IN} | 10.0kΩ |
| 0V to 4V | V _{IN} | AGND | V _{IN} | 10.7kΩ |

TABLE I. Input Range Connections. See Figure 4 for complete information.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|-------------|--|-----|--------------|------|---------------|
| t_1 | Convert Pulse Width | 40 | | 4500 | ns |
| t_2 | $\overline{\text{BUSY}}$ Delay | | | 65 | ns |
| t_3 | $\overline{\text{BUSY}}$ LOW | | | 8 | μs |
| t_4 | $\overline{\text{BUSY}}$ Delay after End of Conversion | 220 | | | ns |
| t_5 | Aperture Delay | 40 | | | ns |
| t_6 | Conversion Time | 5.7 | 8 | | μs |
| t_7 | Acquisition Time | | 2 | | μs |
| $t_6 + t_7$ | Throughput Time | 9 | 10 | | μs |
| t_8 | R/C LOW to DATACLK Delay | 450 | | | ns |
| t_9 | DATACLK Period | 440 | | | ns |
| t_{10} | Data Valid to DATACLK HIGH Delay | 20 | 75 | | ns |
| t_{11} | Data Valid after DATACLK LOW Delay | 100 | 125 | | ns |
| t_{12} | External DATACLK Period | 100 | | | ns |
| t_{13} | External DATACLK HIGH | 20 | | | ns |
| t_{14} | External DATACLK LOW | 30 | | | ns |
| t_{15} | DATACLK HIGH Setup Time | 20 | $t_{12} + 5$ | | ns |
| t_{16} | R/C to $\overline{\text{CS}}$ Setup Time | 10 | | | ns |
| t_{17} | SYNC Delay After DATACLK HIGH | 15 | 35 | | ns |
| t_{18} | Data Valid Delay | 25 | 55 | | ns |
| t_{19} | $\overline{\text{CS}}$ to Rising Edge Delay | 25 | | | ns |
| t_{20} | Data Available after $\overline{\text{CS}}$ LOW | 4.5 | | | μs |

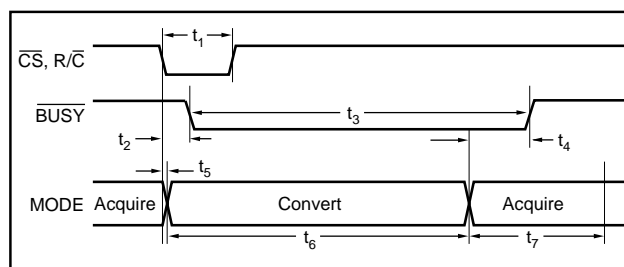


FIGURE 1. Basic Conversion Timing.

TABLE II. Conversion and Data Timing $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

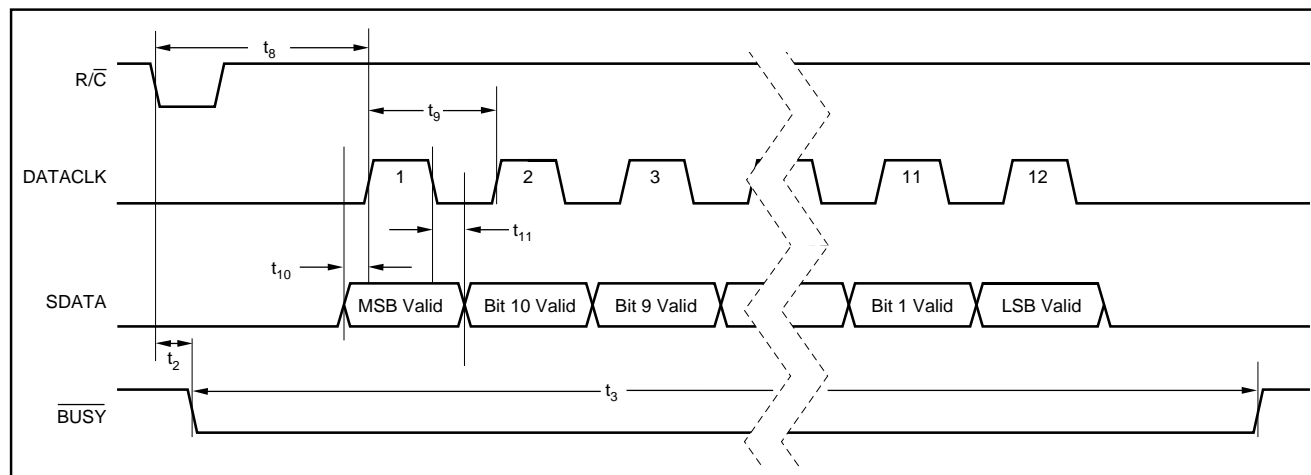


FIGURE 2. Serial Data Timing Using Internal Clock. ($\overline{\text{CS}}$, EXT/INT and TAG Tied LOW.)

| SPECIFIC FUNCTION | \overline{CS} | R/\overline{C} | \overline{BUSY} | $\overline{EXT}/\overline{INT}$ | DATACLK | PWRD | SB/ \overline{BTC} | OPERATION |
|--|-----------------|------------------|-------------------|---------------------------------|---------|------|----------------------|--|
| Initiate Conversion and Output Data Using Internal Clock | 1>0 | 0 | 1 | 0 | Output | 0 | x | Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK. |
| | 0 | 1>0 | 1 | 0 | Output | 0 | x | Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK. |
| Initiate Conversion and Output Data Using External Clock | 1>0 | 0 | 1 | 1 | Input | 0 | x | Initiates conversion "n". |
| | 0 | 1>0 | 1 | 1 | Input | 0 | x | Initiates conversion "n". |
| | 1>0 | 1 | 1 | 1 | Input | x | x | Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK. |
| | 1>0 | 1 | 0 | 1 | Input | 0 | x | Outputs a pulse on SYNC followed by data from conversion "n-1" clocked out synchronized to external DATACLK. ⁽¹⁾ Conversion "n" in process. |
| | 0 | 0>1 | 0 | 1 | Input | 0 | x | Outputs a pulse on SYNC followed by data from conversion "n-1" clocked out synchronized to external DATACLK. ⁽¹⁾ Conversion "n" in process. |
| Incorrect Conversions | 0 | 0 | 0>1 | x | x | 0 | x | \overline{CS} or R/\overline{C} must be HIGH or a new conversion will be initiated without time for acquisition. |
| Power Down | x | x | x | x | x | 0 | x | Analog circuitry powered. Conversion can proceed. |
| | x | x | x | x | x | 1 | x | Analog circuitry disabled. Data from previous conversion maintained in output registers. |
| Selecting Output Format | x | x | x | x | x | x | 0 | Serial data is output in Binary Two's Complement format. |
| | x | x | x | x | x | x | 1 | Serial data is output in Straight Binary format. |

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

Table III. Control Truth Table.

| DESCRIPTION | ANALOG INPUT | | | | | | DIGITAL OUTPUT | | | |
|-----------------------------|--------------|----------|-------------|----------|-----------|----------|--|------|---|------|
| | | | | | | | BINARY TWO'S COMPLEMENT (SB/ \overline{BTC} LOW) | | STRAIGHT BINARY (SB/ \overline{BTC} HIGH) | |
| | | | | | | | HEX BINARY CODE | CODE | HEX BINARY CODE | CODE |
| Full-Scale Range | ± 10 | ± 5 | $\pm 3.33V$ | 0V to 5V | 0V to 10V | 0V to 4V | | | | |
| Least Significant Bit (LSB) | 4.88mV | 2.44mV | 1.63mV | 1.22mV | 2.44mV | 0.98mV | | | | |
| +Full Scale (FS – 1LSB) | 9.99512V | 4.99756V | 3.33171V | 4.99878V | 9.99756V | 3.99902V | 0111 1111 1111 | 7FF | 1111 1111 1111 | FFF |
| Midscale | 0V | 0V | 0V | 2.5V | 5V | 2V | 0000 0000 0000 | 000 | 1000 0000 0000 | 800 |
| One LSB Below Midscale | -4.88mV | -2.44mV | -1.63mV | 2.49878V | 4.99756V | 1.99902V | 1111 1111 1111 | FFF | 0111 1111 1111 | 7FF |
| -Full Scale | -10V | -5V | -3.33333V | 0V | 0V | 0V | 1000 0000 0000 | 800 | 0000 0000 0000 | 000 |

Table IV. Output Codes and Ideal Input Voltages.

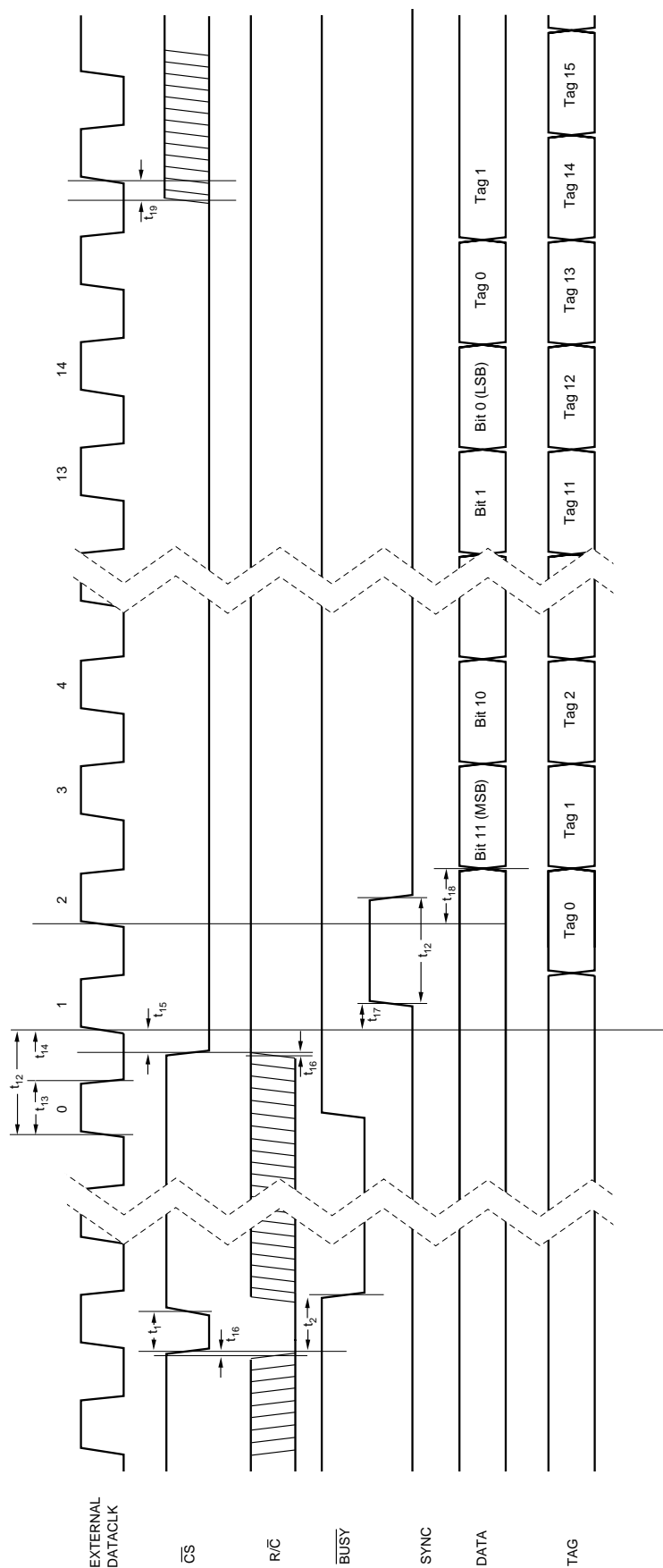


FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/INT Tied HIGH). Read After Conversion.

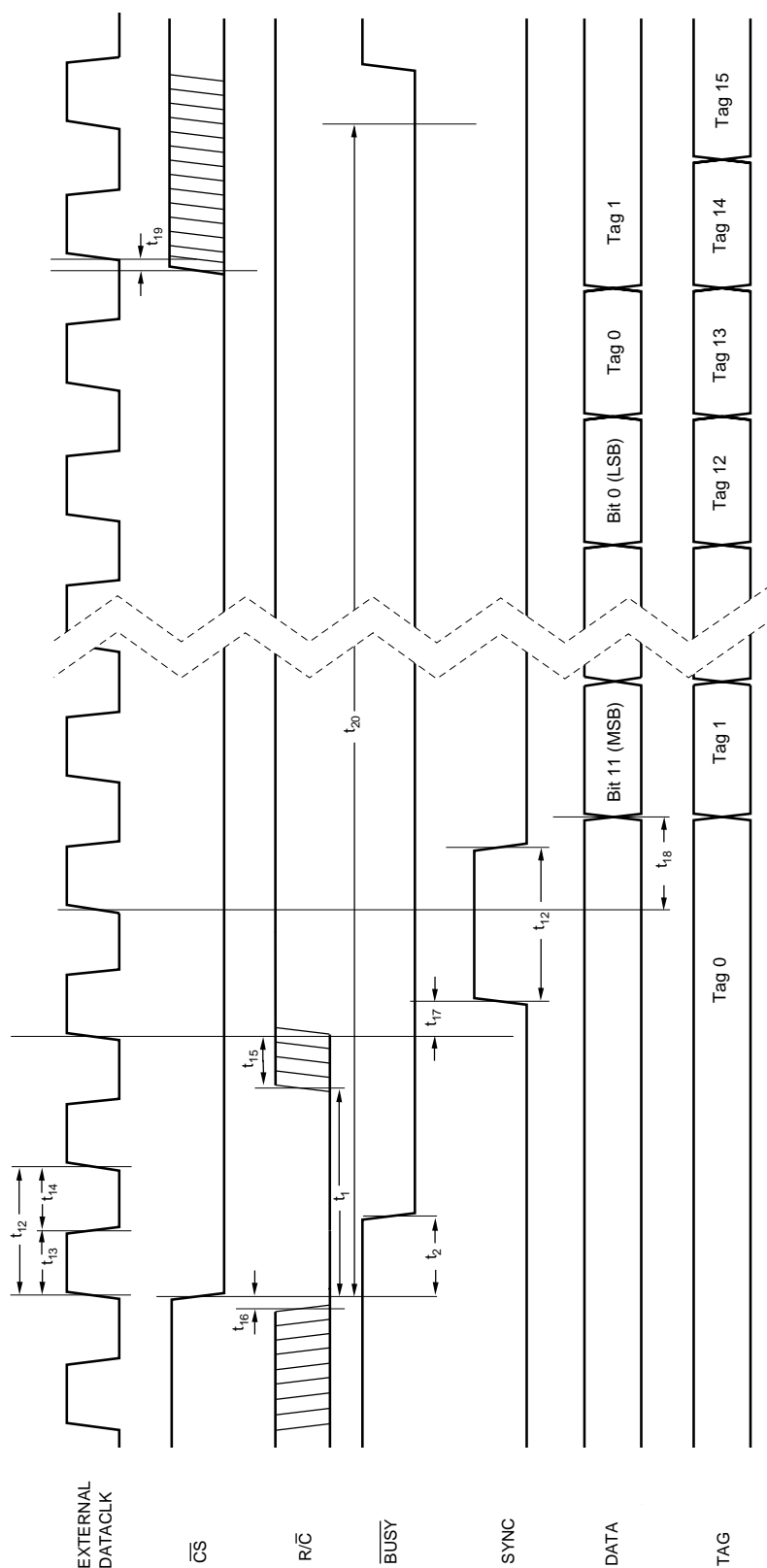


FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/INT Tied HIGH.) Read During Conversion (Previous Conversion Results).

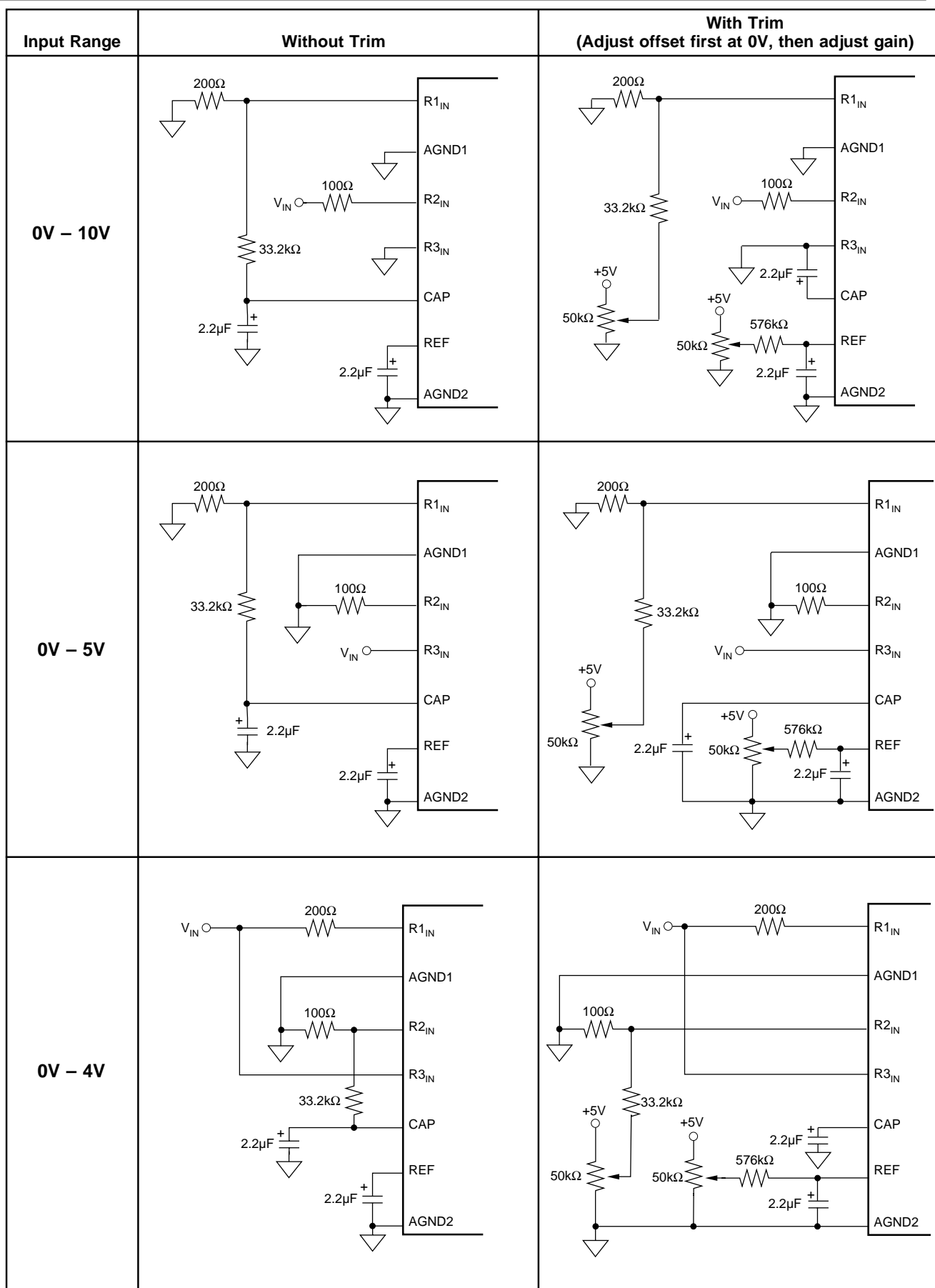


FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

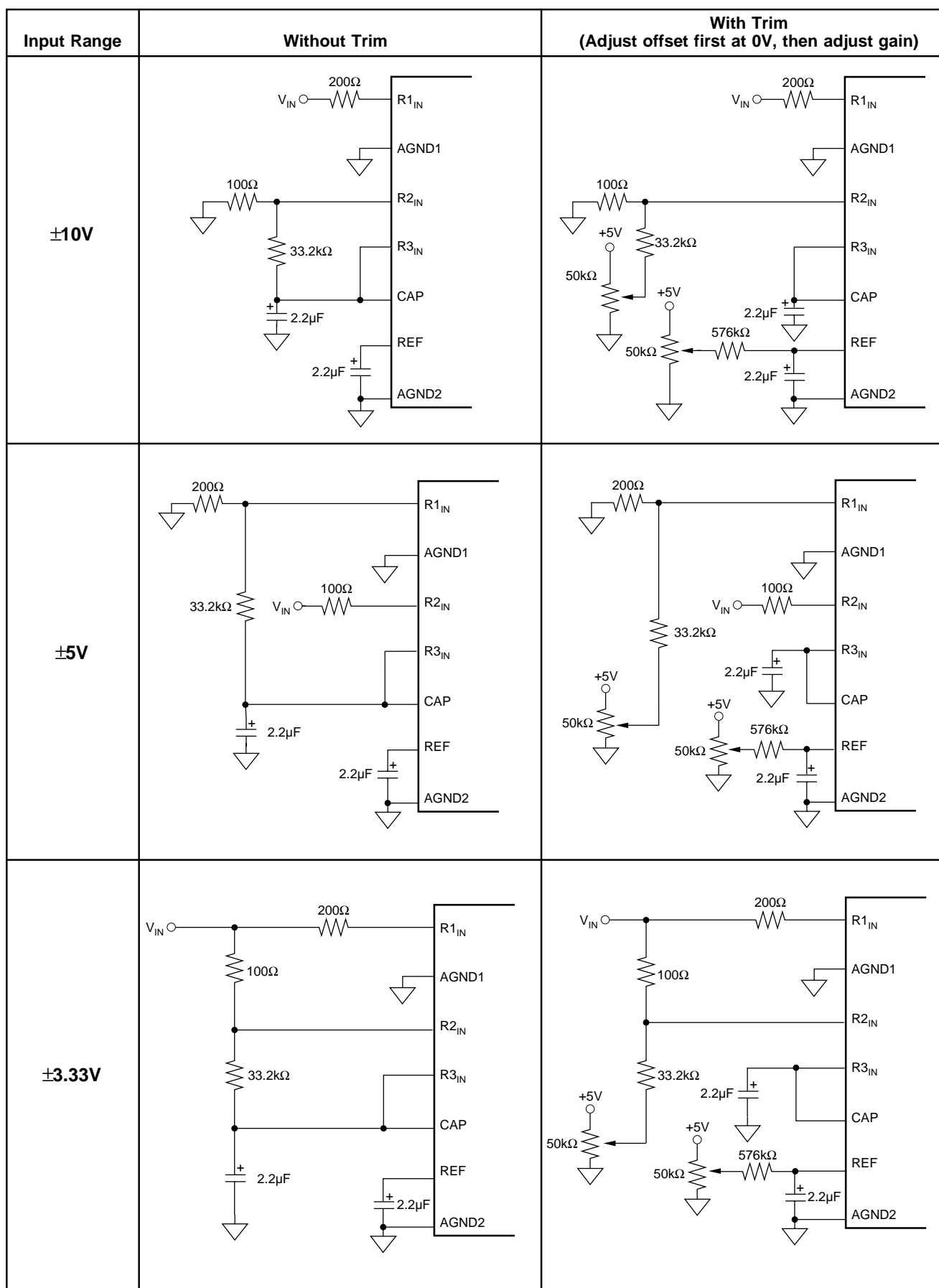


FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| ADS7808P | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI | | | |
| ADS7808PB | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI | | | |
| ADS7808U | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U | |
| ADS7808U/1K | NRND | SOIC | DW | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U | |
| ADS7808U/1KE4 | NRND | SOIC | DW | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U | |
| ADS7808UB | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U B | |
| ADS7808UBG4 | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U B | |
| ADS7808UE4 | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

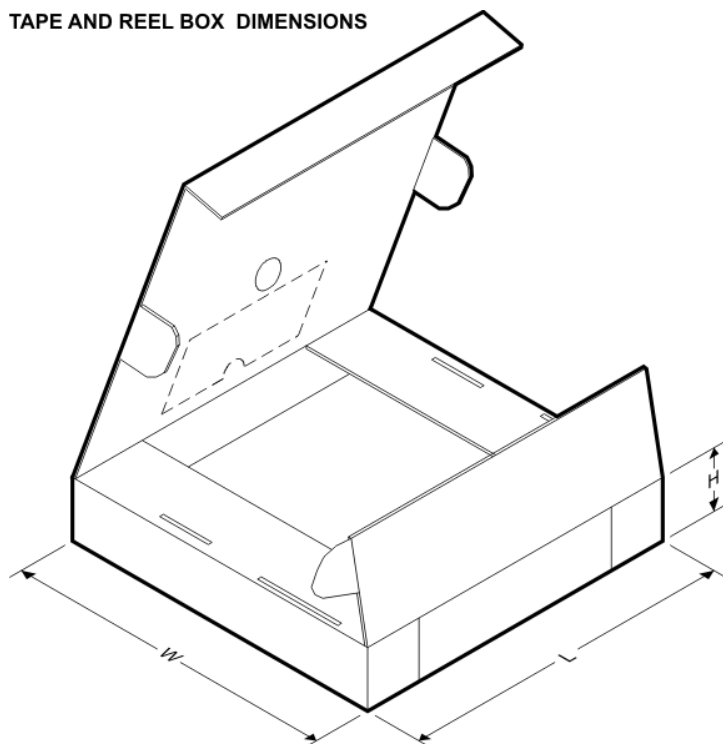
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS7808U/1K | SOIC | DW | 20 | 1000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

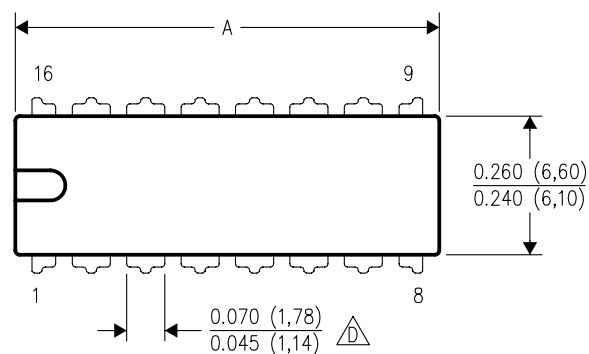
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS7808U/1K | SOIC | DW | 20 | 1000 | 367.0 | 367.0 | 45.0 |

MECHANICAL DATA

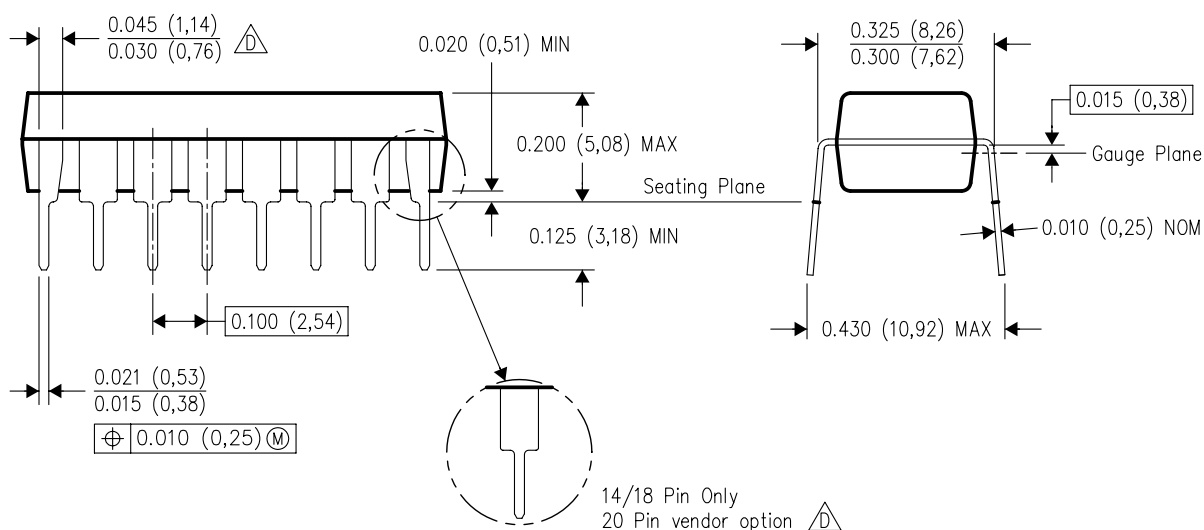
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

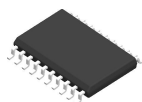


| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (Note C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (Note D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

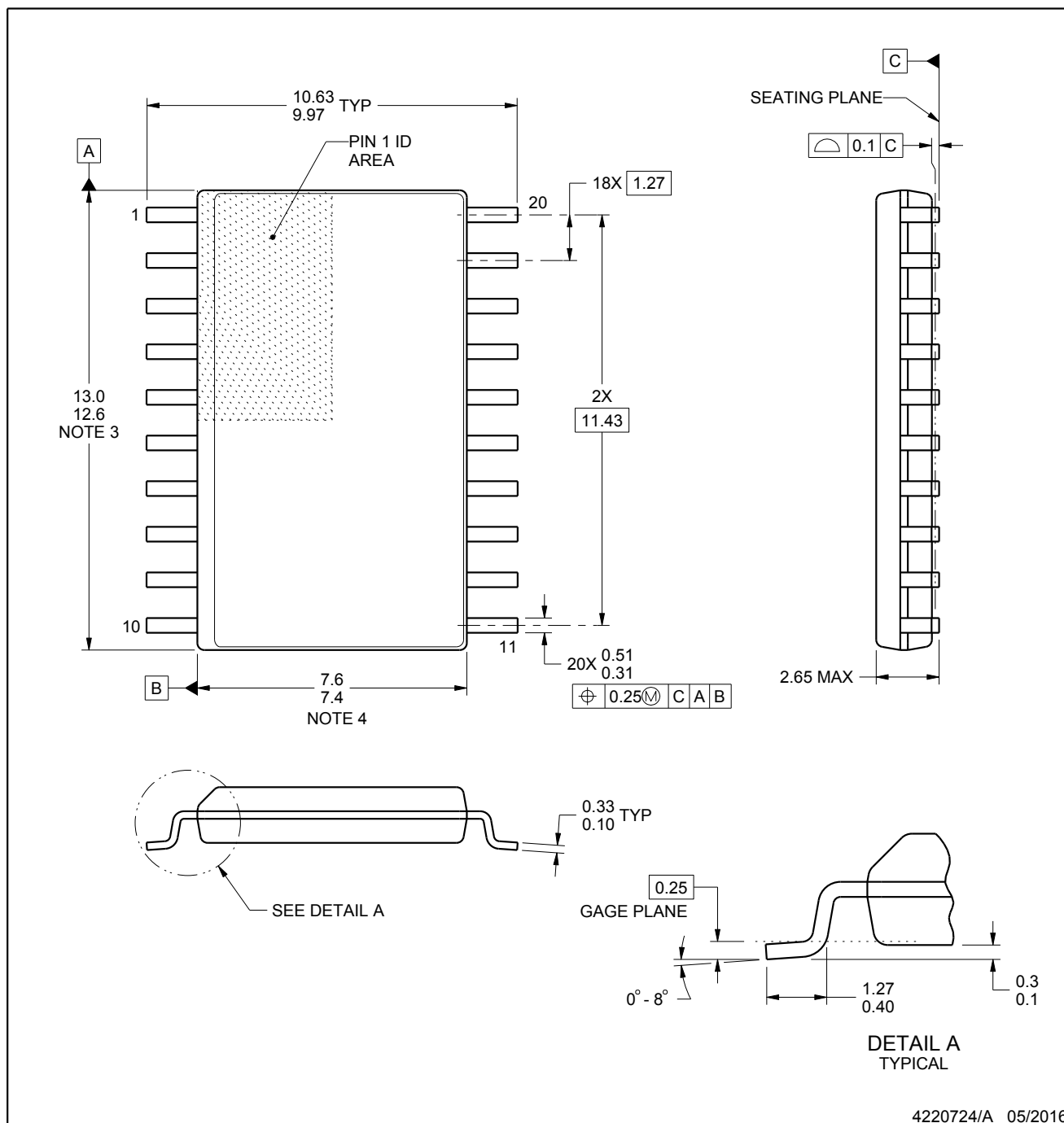


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

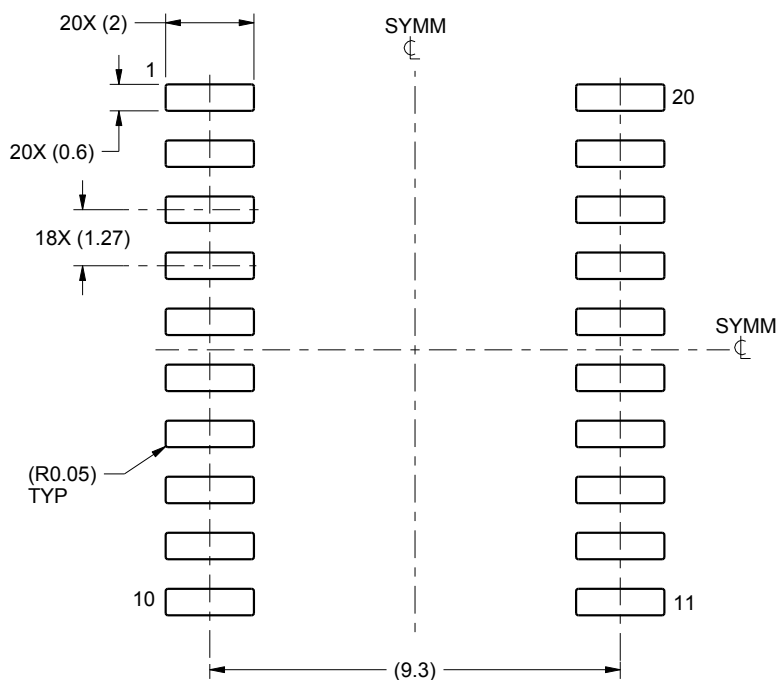
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

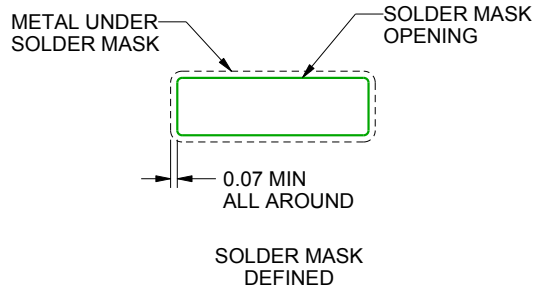
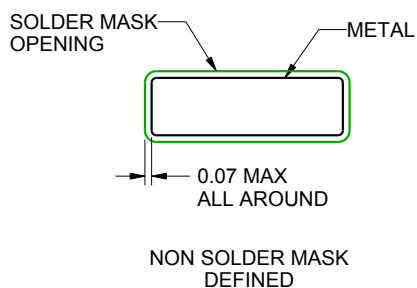
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

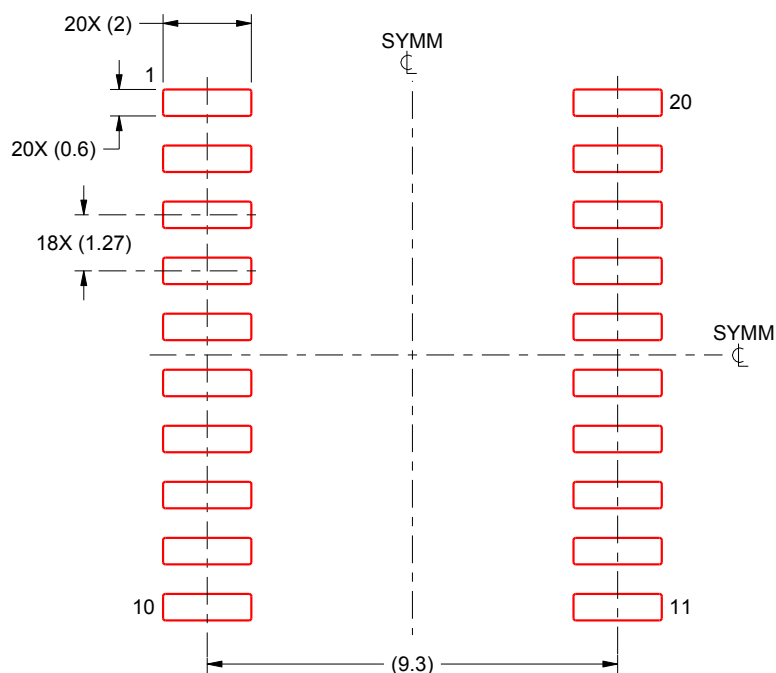
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

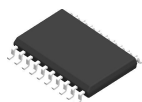


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

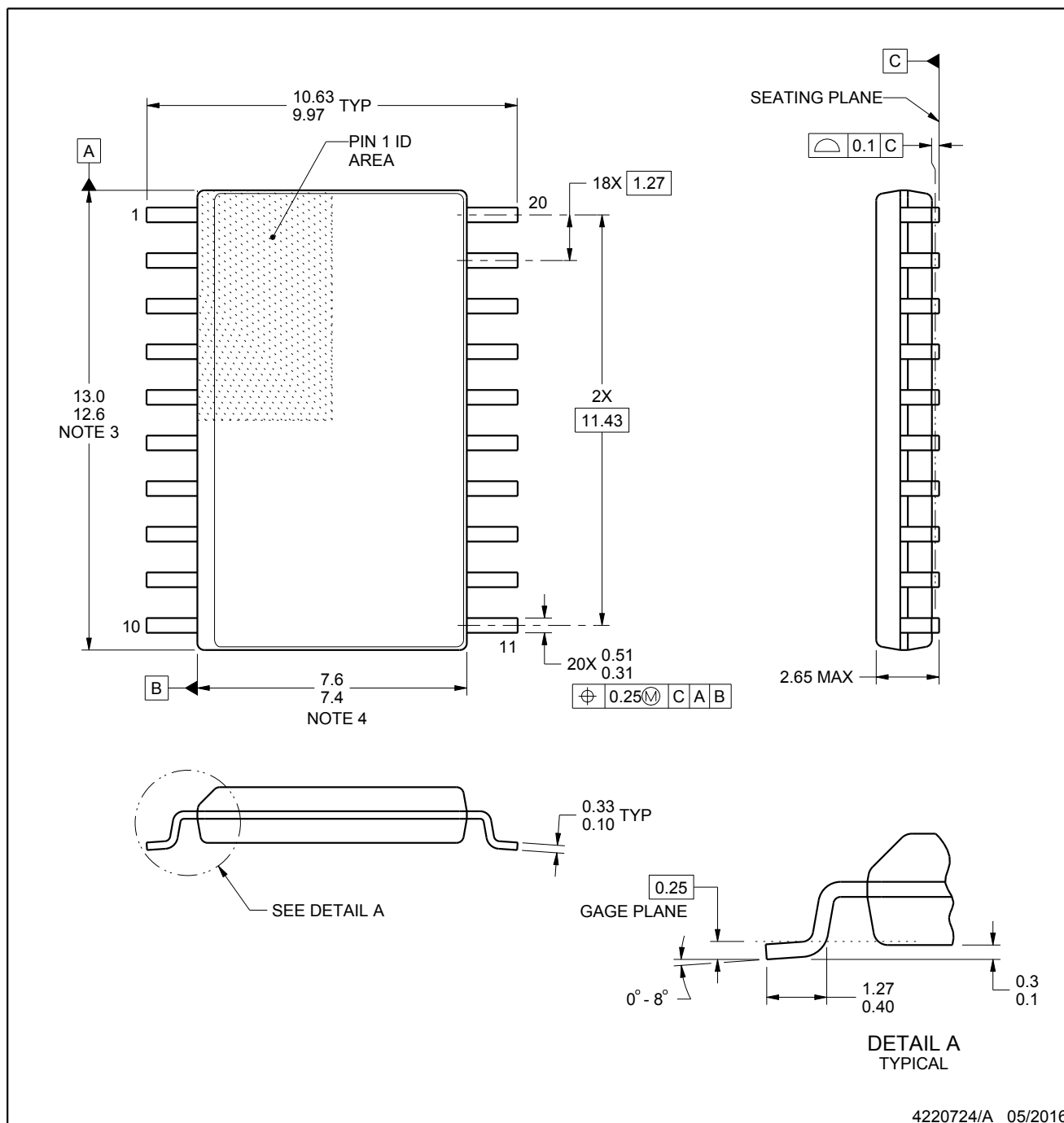


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

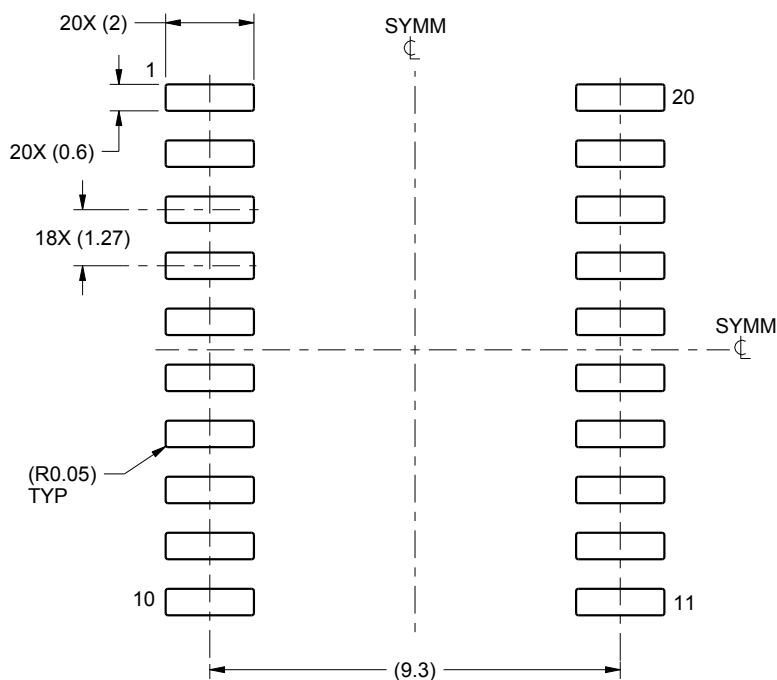
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

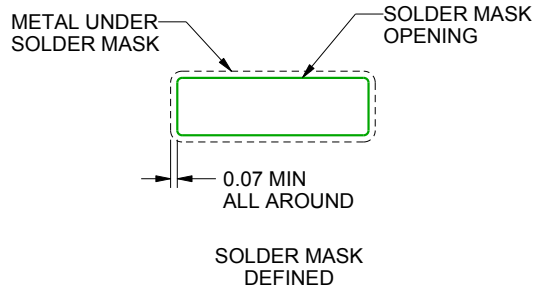
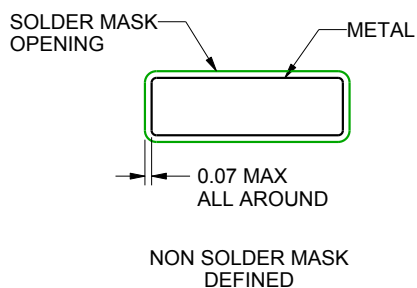
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

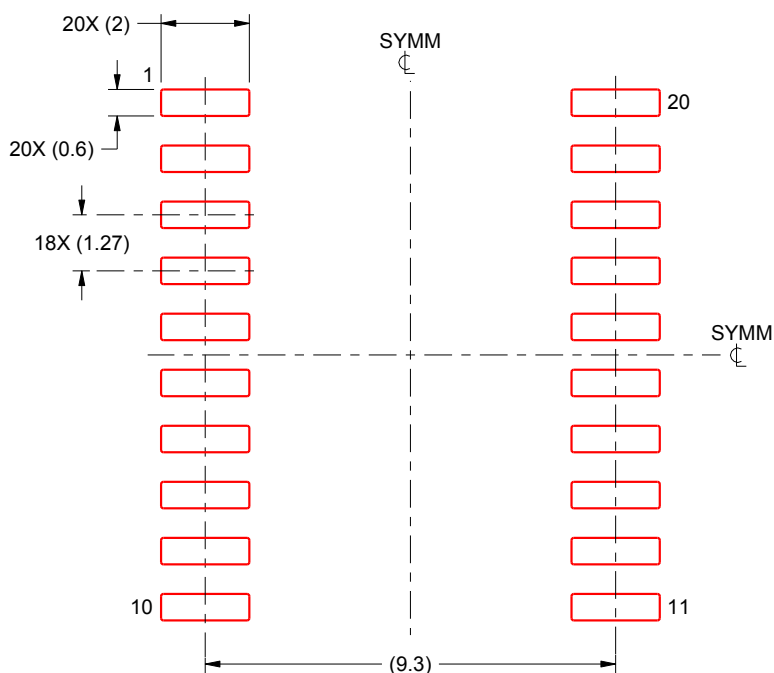
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| ADS7808P | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI | | | |
| ADS7808PB | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI | | | |
| ADS7808U | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U | |
| ADS7808U/1K | NRND | SOIC | DW | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U | |
| ADS7808U/1KE4 | NRND | SOIC | DW | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U | |
| ADS7808UB | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U B | |
| ADS7808UBG4 | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U B | |
| ADS7808UE4 | NRND | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU-DCC | Level-3-260C-168 HR | -40 to 85 | ADS7808U | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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Datasheet of ADS7808U - IC 12-BIT 100KHZ SMPL A/D 20SOIC

Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

PACKAGE OPTION ADDENDUM

11-Apr-2015

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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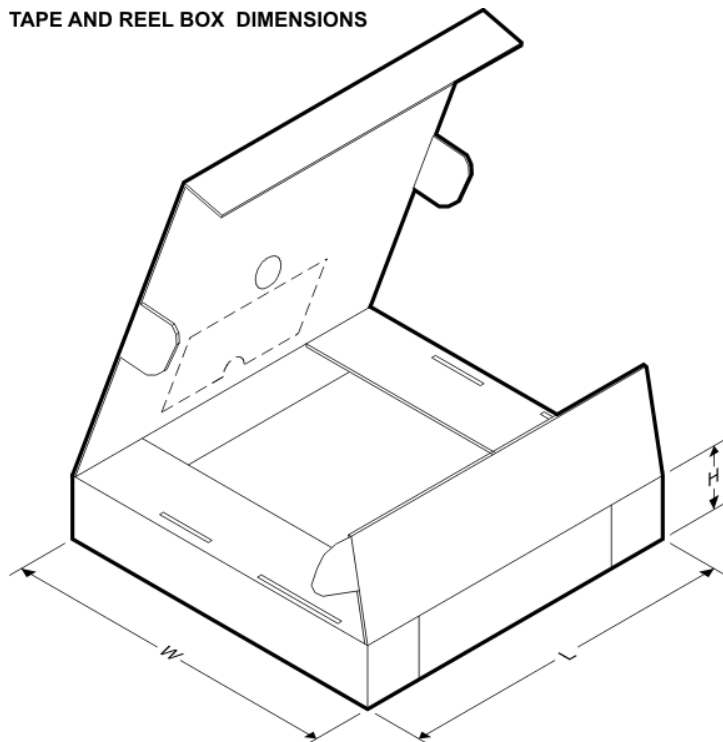
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
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TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

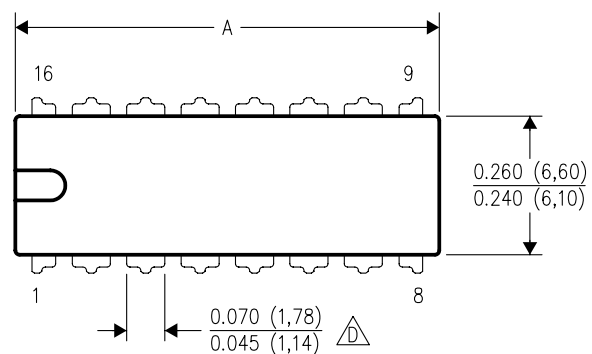
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS7808U/1K | SOIC | DW | 20 | 1000 | 367.0 | 367.0 | 45.0 |

MECHANICAL DATA

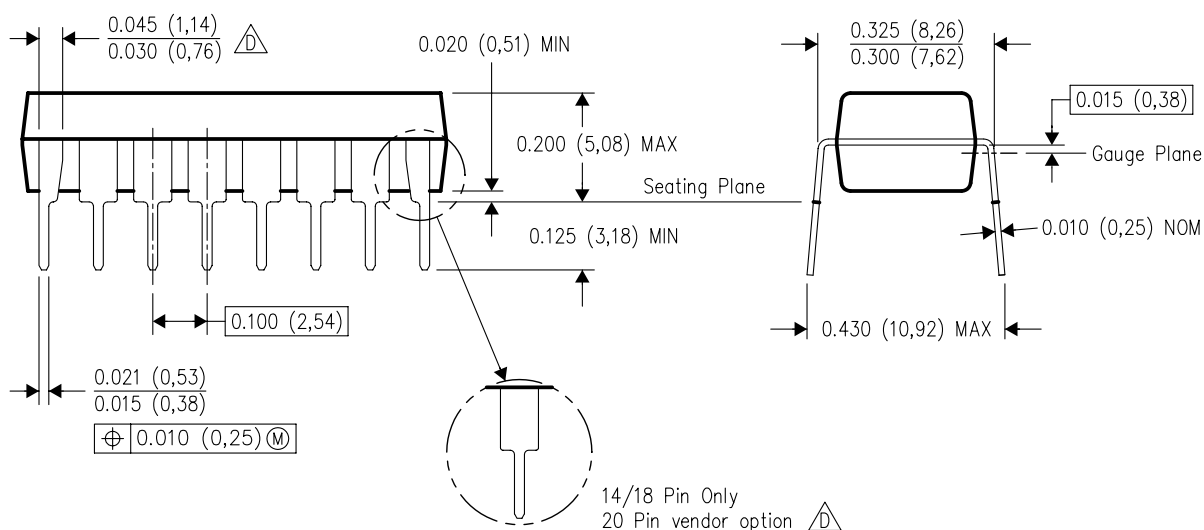
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

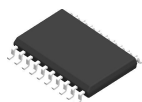


| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - \triangle Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.

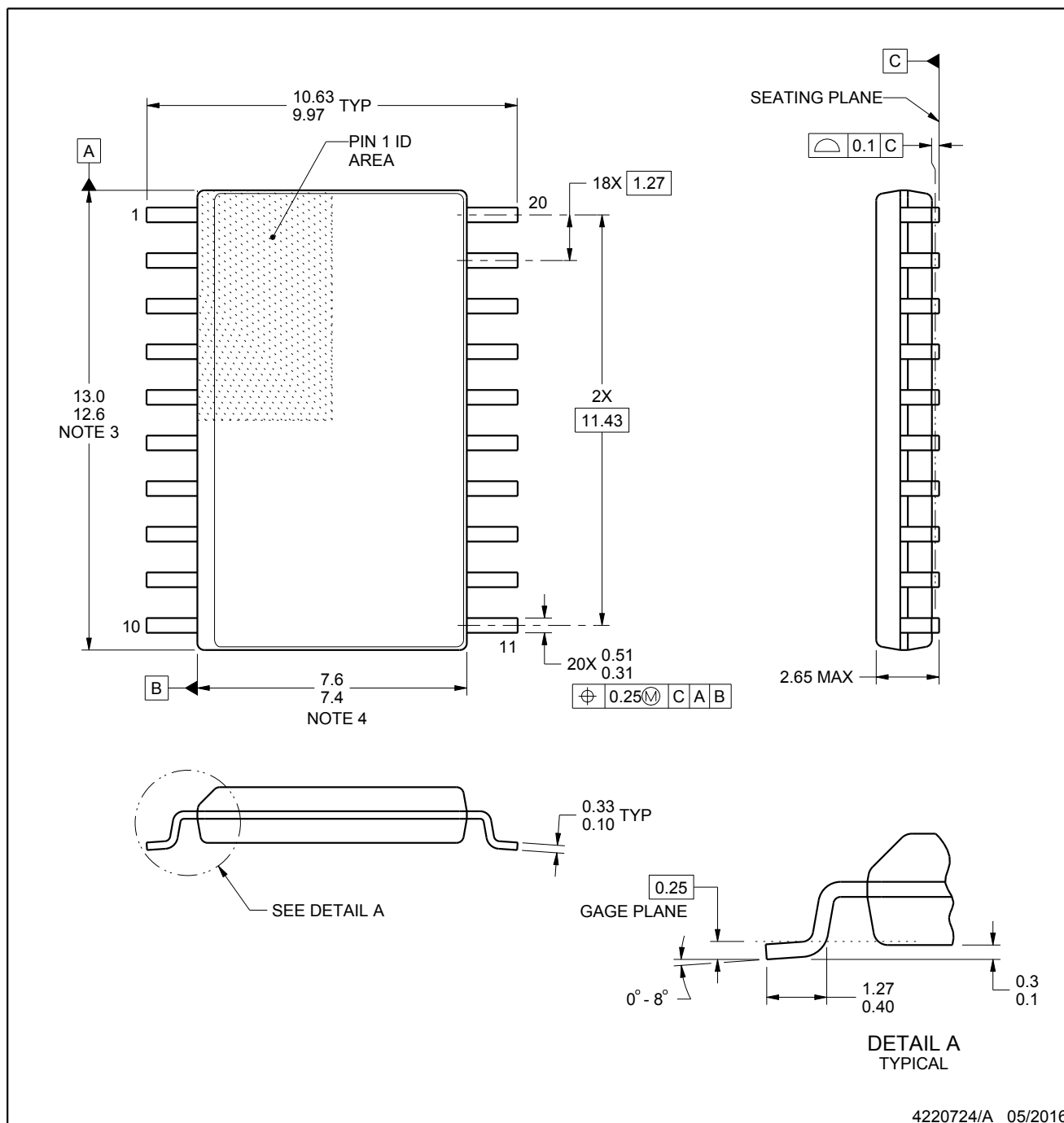


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

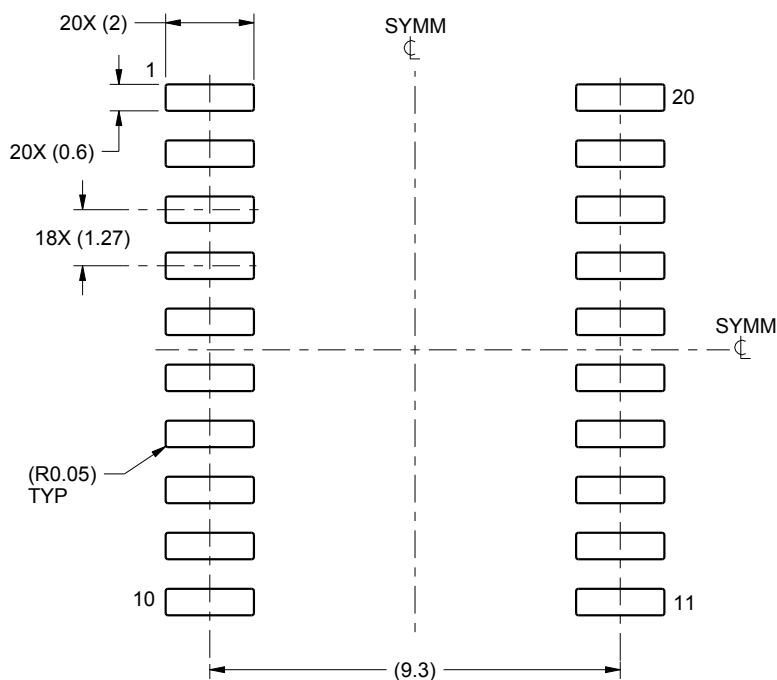
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4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

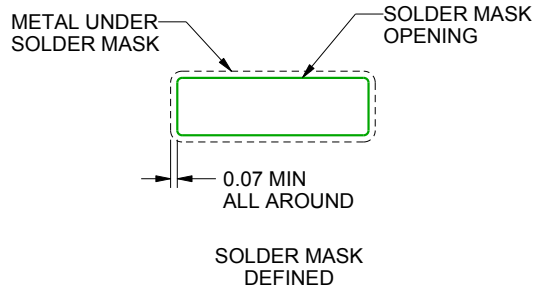
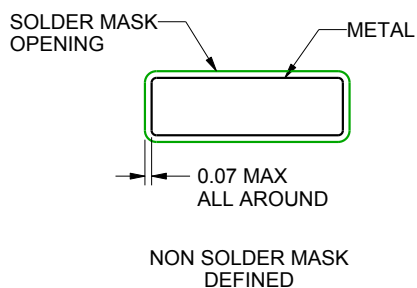
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

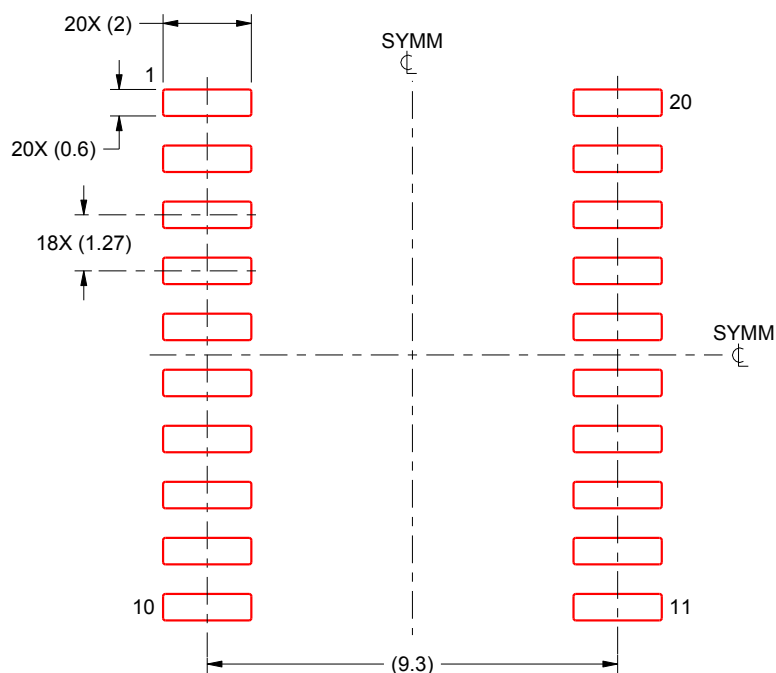
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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