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[Atmel](#)

[AT27C4096-70JC](#)

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## Features

- **Fast Read Access Time - 55 ns**
- **Low Power CMOS Operation**
  - 100  $\mu$ A Maximum Standby
  - 40 mA Maximum Active at 5 MHz
- **JEDEC Standard Packages**
  - 40-Lead 600 mil PDIP
  - 44-Lead PLCC
  - 40-Lead VSOP (10 mm x 14 mm)
- **Direct Upgrade from 512K-bit, 1M-bit, and 2M-bit (AT27C516, AT27C1024, and AT27C2048) EPROMs**
- **5V  $\pm$  10% Power Supply**
- **High Reliability CMOS Technology**
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- **Rapid<sup>TM</sup> Programming Algorithm - 50  $\mu$ s/word (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**



## 4-Megabit (256K x 16) OTP EPROM

## AT27C4096

### Description

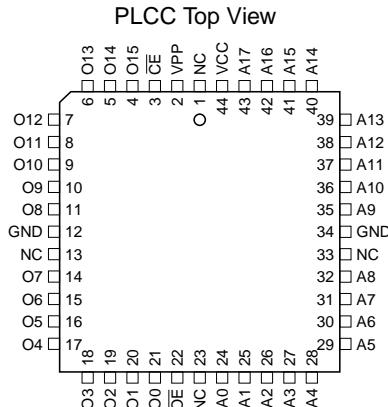
The AT27C4096 is a low-power, high-performance 4,194,304-bit one-time programmable read only memory (OTP EPROM) organized 256K by 16 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in

*(continued)*

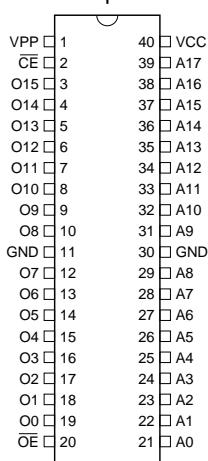
### Pin Configurations

Pin Name	Function
A0 - A17	Addresses
O0 - O15	Outputs
CE	Chip Enable
OE	Output Enable
NC	No Connect

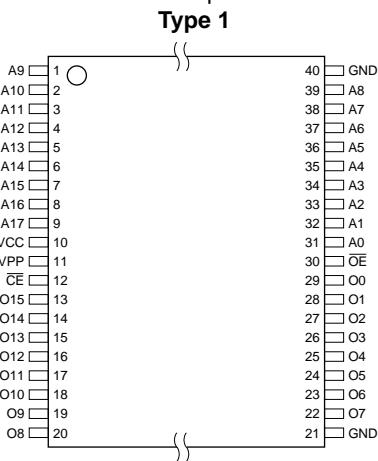
Note: Both GND pins must be connected.



PDIP Top View



VSOP Top View





less than 55 ns, eliminating the need for speed-reducing WAIT states. The by-16 organization makes this part ideal for high-performance 16- and 32-bit microprocessor systems.

In read mode, the AT27C4096 typically consumes 15 mA. Standby mode supply current is typically less than 10  $\mu$ A.

The AT27C4096 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, and VSOP packages. The device features two-line control (CE, OE) to eliminate bus contention in high-speed systems.

With high density 256K word storage capability, the AT27C4096 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

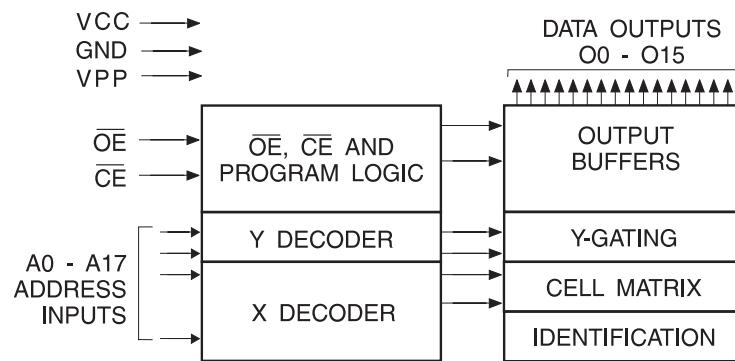
Atmel's AT27C4096 has additional features that ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50  $\mu$ s/word. The Integrated Product Identification Code electronically identifies the device

and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

## System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu$ F high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the  $V_{CC}$  and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu$ F bulk electrolytic capacitor should be utilized, again connected between the  $V_{CC}$  and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## Block Diagram



## Absolute Maximum Ratings\*

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
V <sub>PP</sub> Supply Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Maximum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V<sub>CC</sub> + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

## Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	Ai	V <sub>PP</sub>	Outputs
Read	V <sub>IL</sub>	V <sub>IL</sub>	Ai	X <sup>(1)</sup>	D <sub>OUT</sub>
Output Disable	X	V <sub>IH</sub>	X	X	High Z
Standby	V <sub>IH</sub>	X	X	X <sup>(5)</sup>	High Z
Rapid Program <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	Ai	V <sub>PP</sub>	D <sub>IN</sub>
PGM Verify	V <sub>IH</sub>	V <sub>IL</sub>	Ai	V <sub>PP</sub>	D <sub>OUT</sub>
PGM Inhibit	V <sub>IH</sub>	V <sub>IH</sub>	X	V <sub>PP</sub>	High Z
Product Identification <sup>(4)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	A9 = V <sub>H</sub> <sup>(3)</sup> A0 = V <sub>IH</sub> or V <sub>IL</sub> A1 - A17 = V <sub>IL</sub>	V <sub>CC</sub>	Identification Code

Notes: 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.

2. Refer to the Programming characteristics.

3. V<sub>H</sub> = 12.0 ± 0.5V.

4. Two identifier words may be selected. All Ai inputs are held low (V<sub>IL</sub>), except A9, which is set to V<sub>H</sub>, and A0, which is toggled low (V<sub>IL</sub>) to select the Manufacturer's Identification word and high (V<sub>IH</sub>) to select the Device Code word.

5. Standby V<sub>CC</sub> current (I<sub>SB</sub>) is specified with V<sub>PP</sub> = V<sub>CC</sub>. V<sub>CC</sub> > V<sub>PP</sub> will cause a slight increase in I<sub>SB</sub>.



## DC and AC Operating Conditions for Read Operation

		AT27C4096				
		-55	-70	-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C				
	Ind.	-40°C - 85°C				
V <sub>CC</sub> Power Supply		5V ± 10%				

## DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>		± 1	µA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub>		± 5	µA
I <sub>PP1</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	V <sub>PP</sub> = V <sub>CC</sub>		10	µA
		I <sub>SB1</sub> (CMOS) CĒ = V <sub>CC</sub> ± 0.3V		100	µA
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	I <sub>SB2</sub> (TTL) CĒ = 2.0 to V <sub>CC</sub> + 0.5V		1	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz, I <sub>OUT</sub> = 0 mA, CĒ = V <sub>IL</sub>		40	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 µA	2.4		V

Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>

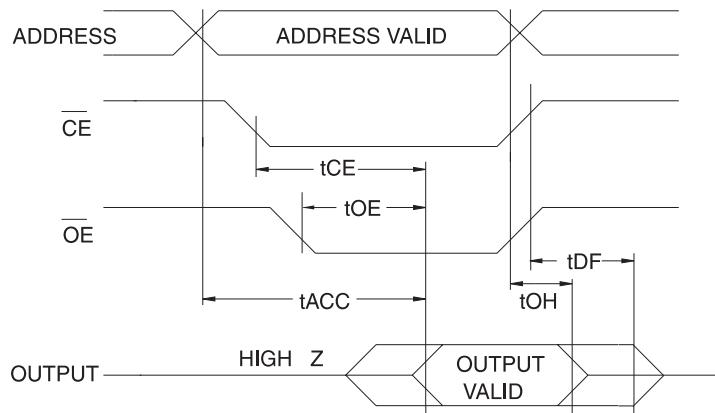
2. V<sub>PP</sub> may be connected directly to V<sub>CC</sub>, except during programming. The supply current would then be the sum of I<sub>CC</sub> and I<sub>PP</sub>

## AC Characteristics for Read Operation

Symbol	Parameter	Condition	AT27C4096									Units
			-55		-70		-90		-12		-15	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t <sub>ACC</sub> <sup>(3)</sup>	Address to Output Delay	CĒ = OĒ = V <sub>IL</sub>	55		70		90		120		150	ns
t <sub>CE</sub> <sup>(2)</sup>	CĒ to Output Delay	OĒ = V <sub>IL</sub>	55		70		90		120		150	ns
t <sub>OE</sub> <sup>(2)(3)</sup>	OĒ to Output Delay	CĒ = V <sub>IL</sub>	20		30		35		40		50	ns
t <sub>DF</sub> <sup>(4)(5)</sup>	OĒ or CĒ High to Output Float, whichever occurred first		20		20		20		30		35	ns
t <sub>OH</sub> <sup>(4)</sup>	Output Hold from Address, CĒ or OĒ, whichever occurred first		7		7		0		0		0	ns

Note: 2, 3, 4, 5. See the AC Waveforms for Read Operation diagram.

## AC Waveforms for Read Operation<sup>(1)</sup>

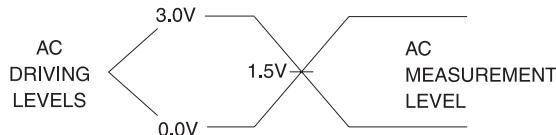


Notes:

1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2.  $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
3.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

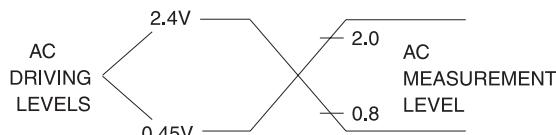
## Input Test Waveforms and Measurement Levels

For -55 devices only:



$t_R, t_F < 5$  ns (10% to 90%)

For -70, -90, -12 and -15 devices:



$t_R, t_F < 20$  ns (10% to 90%)

## Pin Capacitance

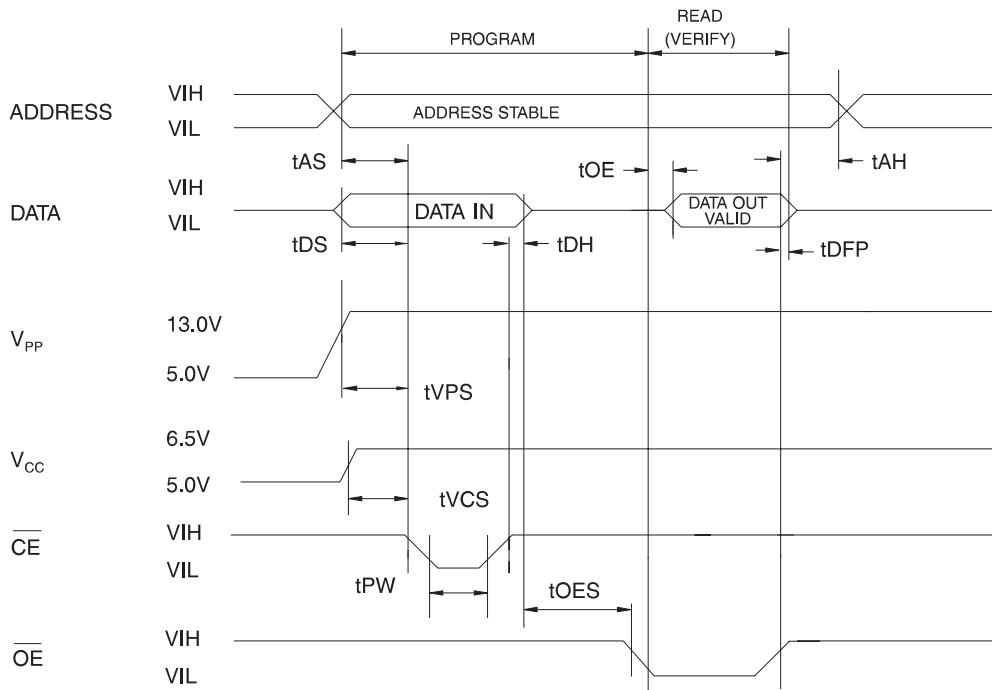
$f = 1$  MHz,  $T = 25^\circ\text{C}$ <sup>(1)</sup>

Symbol	Typ	Max	Units	Conditions
$C_{IN}$	4	10	pF	$V_{IN} = 0\text{V}$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0\text{V}$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.



## Programming Waveforms<sup>(1)</sup>



Notes:

1. The Input Timing Reference is 0.8V for  $V_{IL}$  and 2.0V for  $V_{IH}$ .
2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C4096, a 0.1  $\mu$ F capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients.

## DC Programming Characteristics

$T_A = 25 \pm 5^\circ C$ ,  $V_{CC} = 6.5 \pm 0.25V$ ,  $V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$I_{LI}$	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		$\pm 10$	$\mu A$
$V_{IL}$	Input Low Level		-0.6	0.8	V
$V_{IH}$	Input High Level		2.0	$V_{CC} + 0.7$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1 \text{ mA}$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -400 \mu A$	2.4		V
$I_{CC2}$	$V_{CC}$ Supply Current (Program and Verify)			50	$mA$
$I_{PP2}$	$V_{PP}$ Supply Current	$\overline{CE} = V_{IL}$		30	$mA$
$V_{ID}$	A9 Product Identification Voltage		11.5	12.5	V

## AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Limits		Units
			Min	Max	
$t_{AS}$	Address Setup Time	Input Rise and Fall Times : (10% to 90%) 20 ns Input Pulse Levels: 0.45V to 2.4V Input Timing Reference Level: 0.8V to 2.0V Output Timing Reference Level: 0.8V to 2.0V	2		μs
$t_{OES}$	$\overline{OE}$ Setup Time		2		μs
$t_{DS}$	Data Setup Time		2		μs
$t_{AH}$	Address Hold Time		0		μs
$t_{DH}$	Data Hold Time		2		μs
$t_{DFP}$	$\overline{OE}$ High to Output Float Delay <sup>(2)</sup>		0	130	ns
$t_{VPS}$	$V_{PP}$ Setup Time		2		μs
$t_{VCS}$	$V_{CC}$ Setup Time		2		μs
$t_{PW}$	$\overline{CE}$ Program Pulse Width <sup>(3)</sup>		47.5	52.5	μs
$t_{OE}$	Data Valid from $\overline{OE}$			150	ns
$t_{PRT}$	$V_{PP}$ Pulse Rise Time During Programming		50		ns

Notes:

1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven —see timing diagram.
3. Program Pulse width tolerance is 50 μsec ± 5%.

## Atmel's 27C4096 Intergrated Product Identification Code

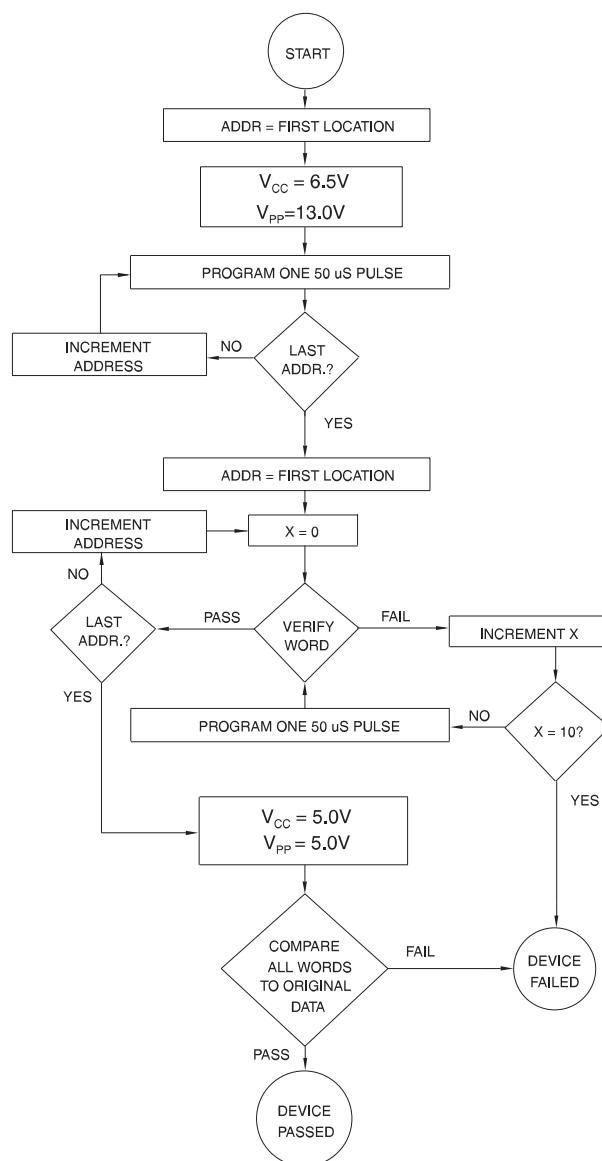
Codes	Pins										Hex Data
	A0	O15-O8	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	1	0	0	00F4



## Rapid Programming Algorithm

A 50  $\mu$ s  $\overline{CE}$  pulse width is used to program. The address is set to the first location.  $V_{CC}$  is raised to 6.5V and  $V_{PP}$  is raised to 13.0V. Each address is first programmed with one 50  $\mu$ s  $\overline{CE}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50  $\mu$ s pulses are applied with a verification after each

pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked.  $V_{PP}$  is then lowered to 5.0V and  $V_{CC}$  to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



# AT27C4096

## Ordering Information

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	40	0.1	AT27C4096-55JC AT27C4096-55PC AT27C4096-55VC	44J 40P6 40V	Commercial (0°C to 70°C)
	40	0.1	AT27C4096-55JI AT27C4096-55PI AT27C4096-55VI	44J 40P6 40V	Industrial (-40°C to 85°C)
70	40	0.1	AT27C4096-70JC AT27C4096-70PC AT27C4096-70VC	44J 40P6 40V	Commercial (0°C to 70°C)
	40	0.1	AT27C4096-70JI AT27C4096-70PI AT27C4096-70VI	44J 40P6 40V	Industrial (-40°C to 85°C)
90	40	0.1	AT27C4096-90JC AT27C4096-90PC AT27C4096-90VC	44J 40P6 40V	Commercial (0°C to 70°C)
	40	0.1	AT27C4096-90JI AT27C4096-90PI AT27C4096-90VI	44J 40P6 40V	Industrial (-40°C to 85°C)
120	40	0.1	AT27C4096-12JC AT27C4096-12PC AT27C4096-12VC	44J 40P6 40V	Commercial (0°C to 70°C)
	40	0.1	AT27C4096-12JI AT27C4096-12PI AT27C4096-12VI	44J 40P6 40V	Industrial (-40°C to 85°C)
150	40	0.1	AT27C4096-15JC AT27C4096-15PC AT27C4096-15VC	44J 40P6 40V	Commercial (0°C to 70°C)
	40	0.1	AT27C4096-15JI AT27C4096-15PI AT27C4096-15VI	44J 40P6 40V	Industrial (-40°C to 85°C)

### Package Type

44J	44-Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
40V	40-Lead, Plastic Thin Small Outline Package (VSOP) 10 x 14 mm



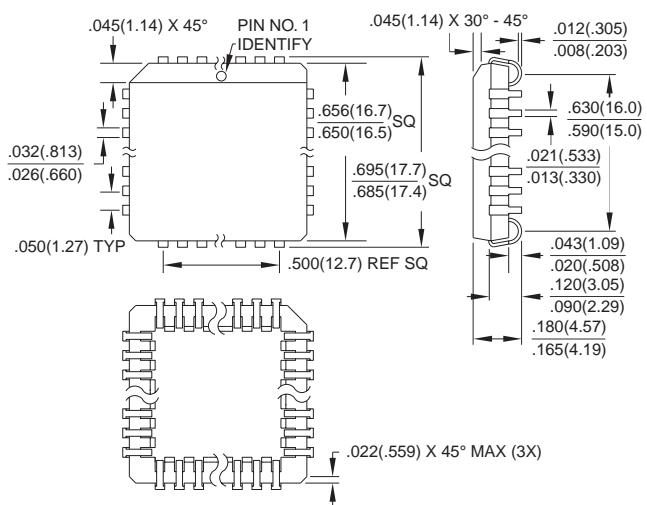


## Packaging Information

### 44J, 44-Lead, Plastic J-Leaded Chip Carrier (PLCC)

Dimensions in Inches and (Millimeters)

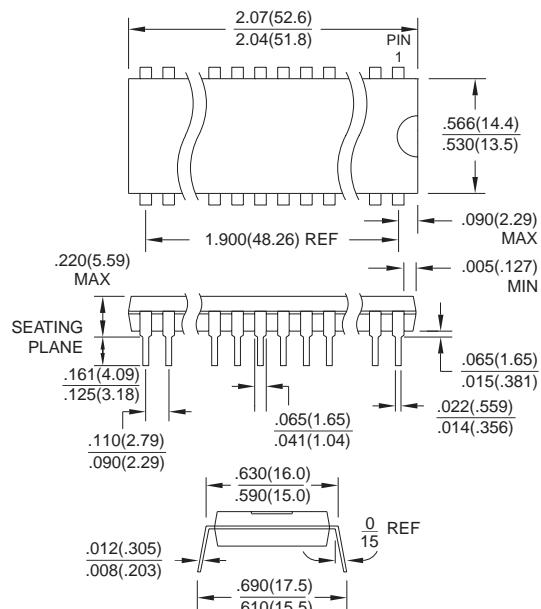
JEDEC STANDARD MS-018 AC



### 40P6, 40-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Dimensions in Inches and (Millimeters)

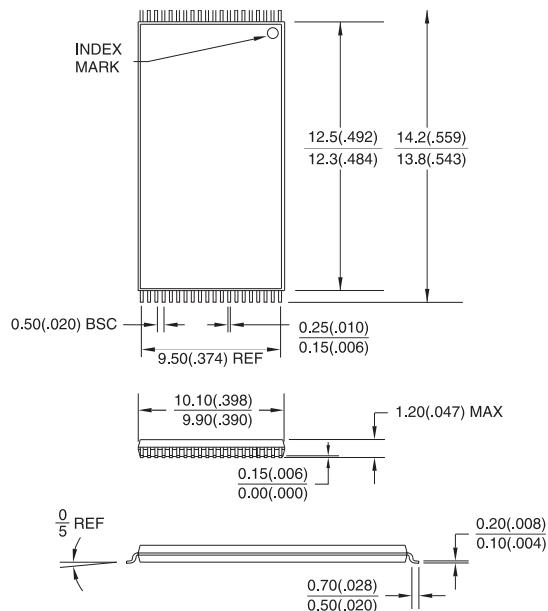
JEDEC STANDARD MS-011 AC



### 40V, 40-Lead, Plastic Thin Small Outline Package (TSOP)

Dimensions in Millimeters and (Inches)

JEDEC OUTLINE MO-142 CA





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