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# AON7462

## 300V, 2.5A N-Channel MOSFET

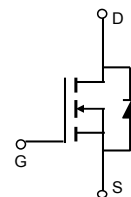
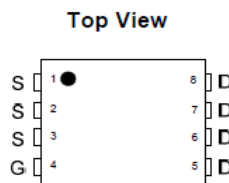
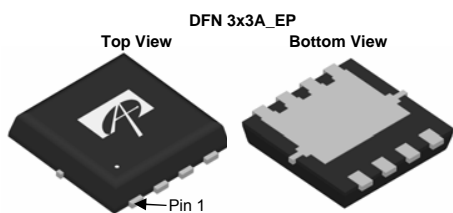
### General Description

The AON7462 is fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low  $R_{DS(on)}$ ,  $C_{iss}$  and  $C_{rss}$  along with guaranteed avalanche capability this device can be adopted quickly into new and existing offline power supply designs. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

### Product Summary

$V_{DS}$	350V@150°C
$I_D$ (at $V_{GS}=10V$ )	2.5A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 1.5Ω

100% UIS Tested!  
100%  $R_g$  Tested!



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	300	V
Gate-Source Voltage	$V_{GS}$	±30	V
Continuous Drain Current <sup>B</sup>	$T_C=25^\circ C$	2.5	A
	$T_C=100^\circ C$	1.6	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	7.2	
Continuous Drain Current	$T_A=25^\circ C$	0.9	A
	$T_A=70^\circ C$	0.7	
Avalanche Current <sup>C</sup>	$I_{AR}$	1.4	A
Repetitive avalanche energy <sup>C</sup>	$E_{AR}$	29	mJ
Single pulsed avalanche energy <sup>G</sup>	$E_{AS}$	58	mJ
Peak diode recovery dv/dt	dv/dt	5	V/ns
Power Dissipation <sup>B</sup>	$T_C=25^\circ C$	25	W
	$T_C=100^\circ C$	10	
Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	3.1	W
	$T_A=70^\circ C$	2	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-50 to 150	°C

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	30	40	°C/W
Maximum Junction-to-Ambient <sup>A D</sup>		60	75	
Maximum Junction-to-Case	$R_{\theta JC}$	4.2	5	°C/W

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	300			V
		I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C		350		
BV <sub>DSS</sub> /ΔT <sub>J</sub>	Zero Gate Voltage Drain Current	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V		0.3		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =300V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =240V, T <sub>J</sub> =125°C			10	
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA	3.5	4.2	4.5	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =0.9A		1.2	1.5	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =40V, I <sub>D</sub> =0.9A		1.5		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.8	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2.5	A
I <sub>SM</sub>	Maximum Body-Diode Pulsed Current				9	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz	155	197	240	pF
C <sub>oss</sub>	Output Capacitance		20	30	40	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			2		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1.9	3.8	5.7	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =240V, I <sub>D</sub> =0.9A	3.5	4.6	5.6	nC
Q <sub>gs</sub>	Gate Source Charge				1.3	nC
Q <sub>gd</sub>	Gate Drain Charge				1.5	nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =150V, I <sub>D</sub> =0.9A, R <sub>G</sub> =25Ω		17		ns
t <sub>r</sub>	Turn-On Rise Time			8		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			26		ns
t <sub>f</sub>	Turn-Off Fall Time			13		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =0.9A, di/dt=100A/μs, V <sub>DS</sub> =100V	62	95	125	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =0.9A, di/dt=100A/μs, V <sub>DS</sub> =100V	0.14	0.22	0.3	μC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power Dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> t ≤ 10s value and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

H. L=60mH, I<sub>AS</sub>=1.4A, V<sub>DD</sub>=150V, R<sub>G</sub>=10Ω, Starting T<sub>J</sub>=25°C

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

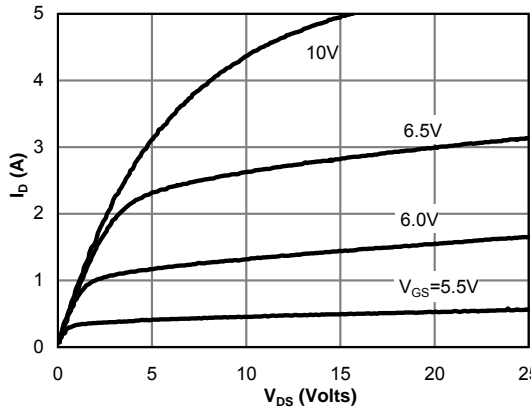


Figure 1: On-Region Characteristics

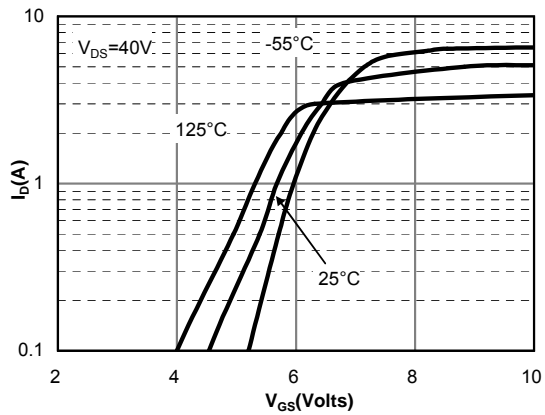


Figure 2: Transfer Characteristics

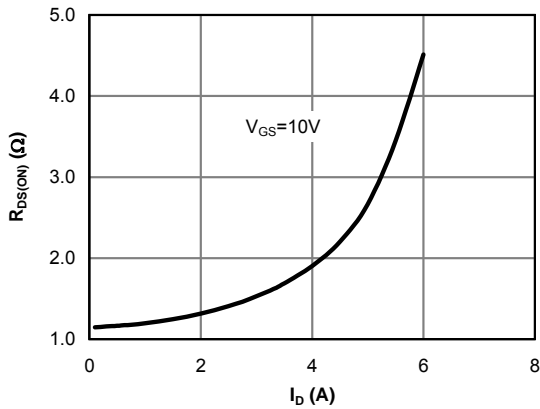


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

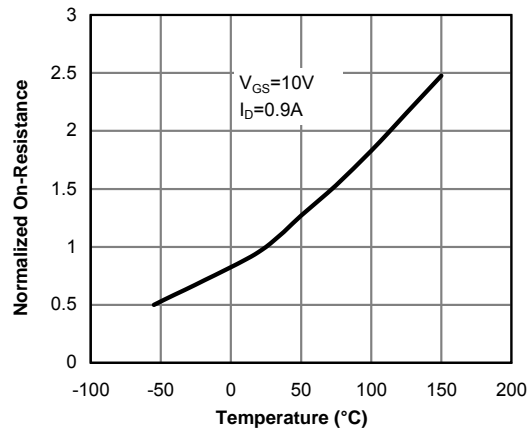


Figure 4: On-Resistance vs. Junction Temperature

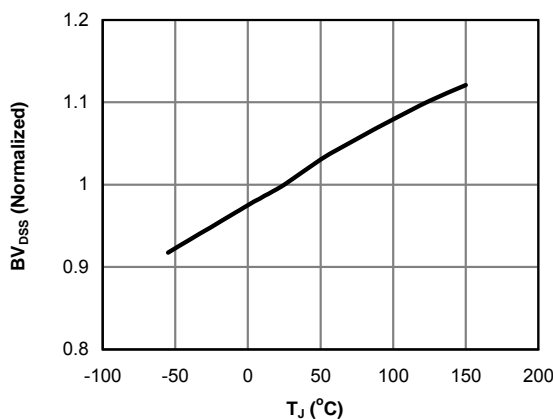


Figure 5: Break Down vs. Junction Temperature

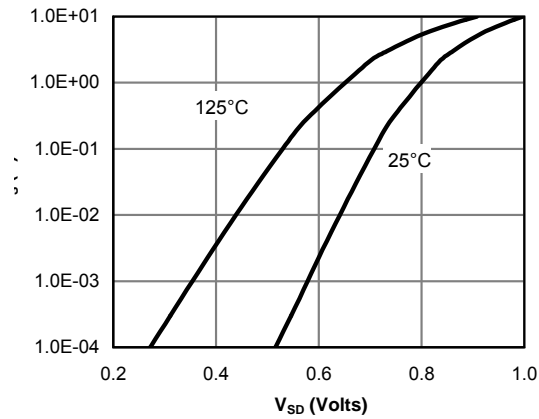


Figure 6: Body-Diode Characteristics

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

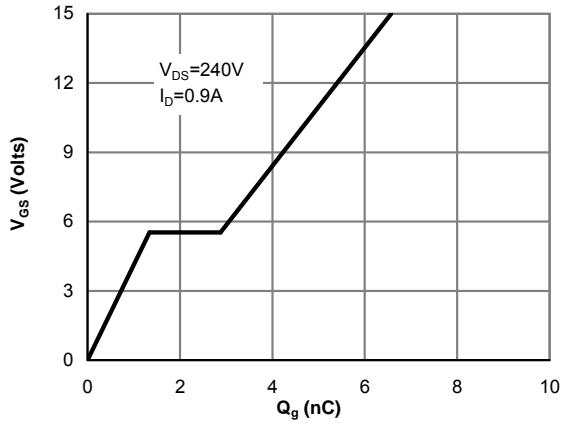


Figure 7: Gate-Charge Characteristics

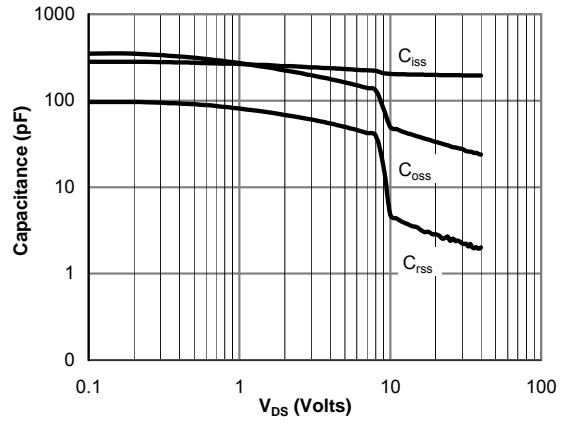


Figure 8: Capacitance Characteristics

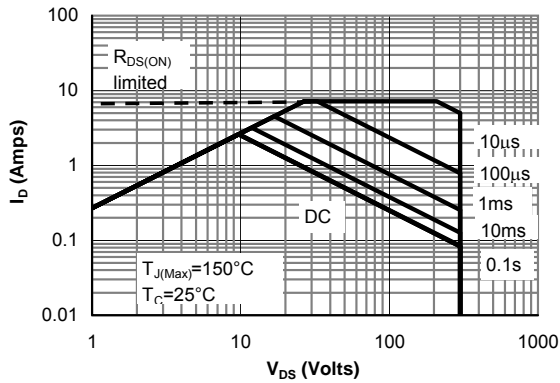


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

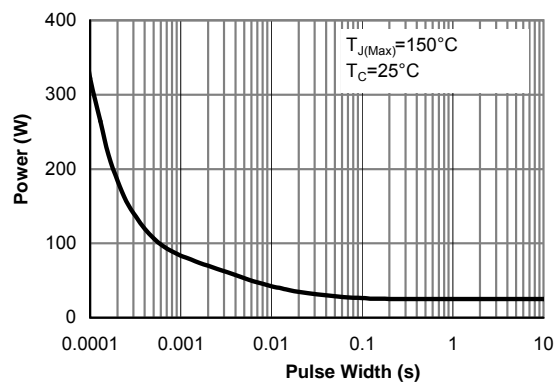


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

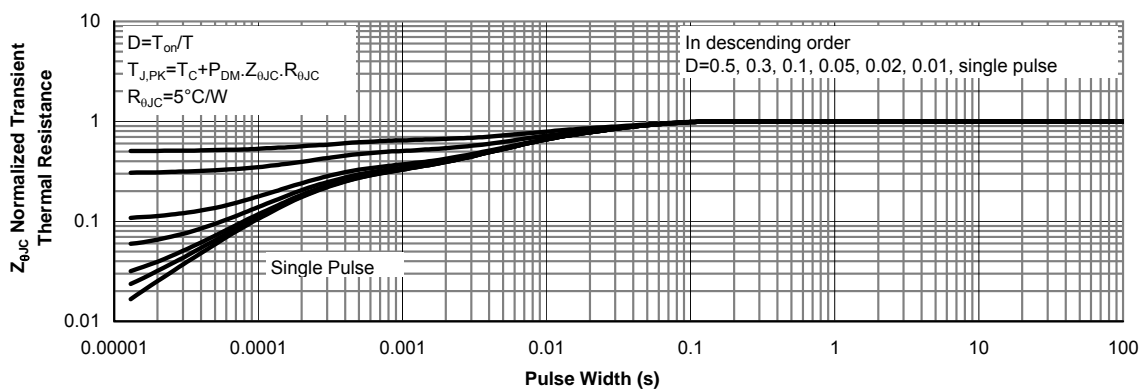


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

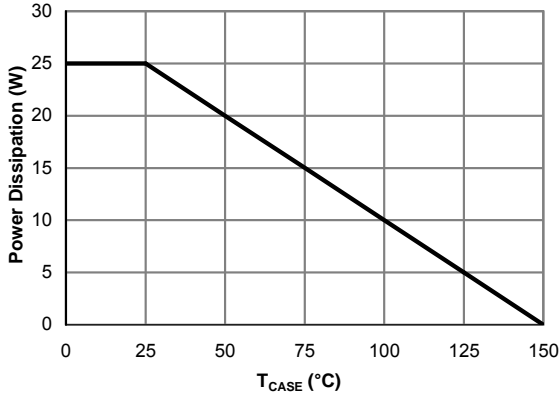


Figure 12: Power De-rating (Note B)

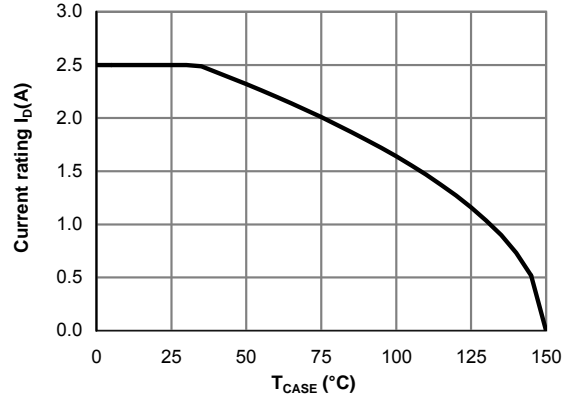


Figure 13: Current De-rating (Note B)

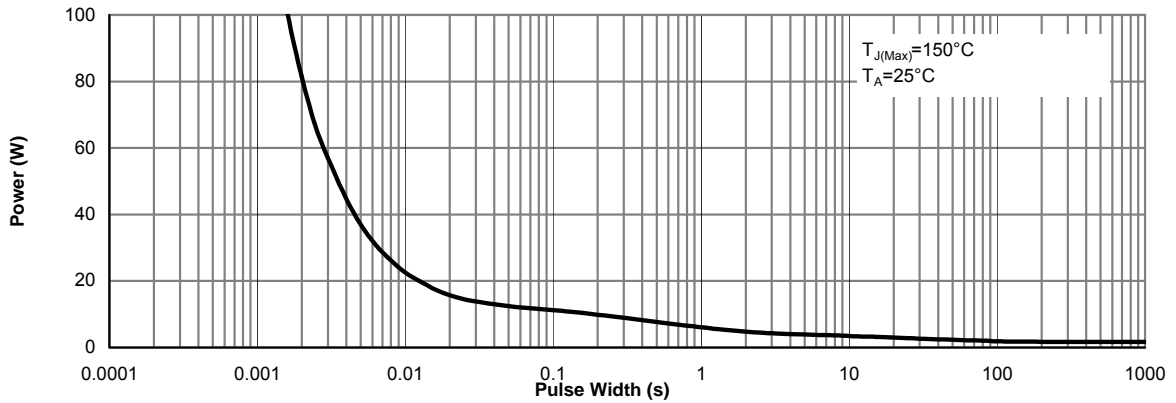


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

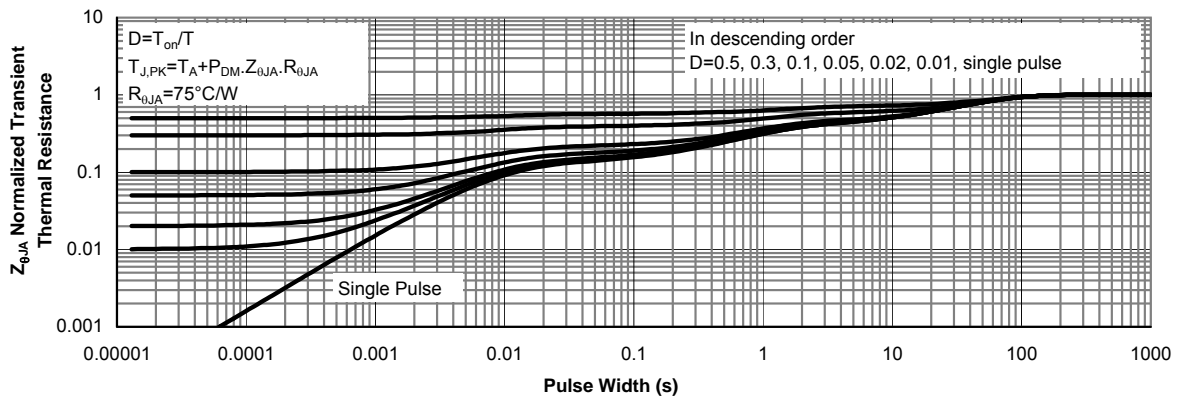
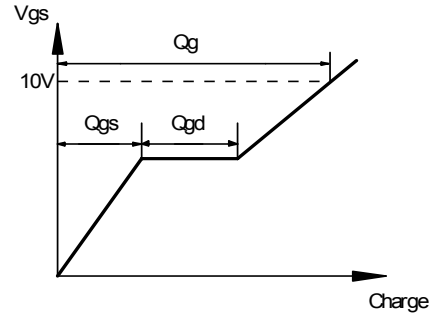
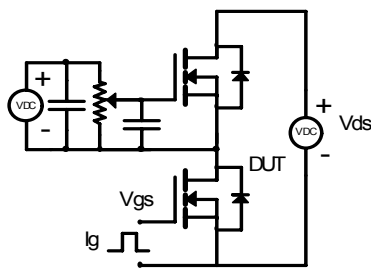
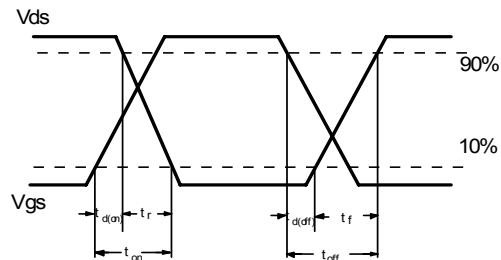
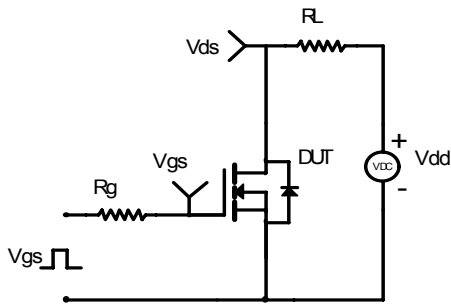


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

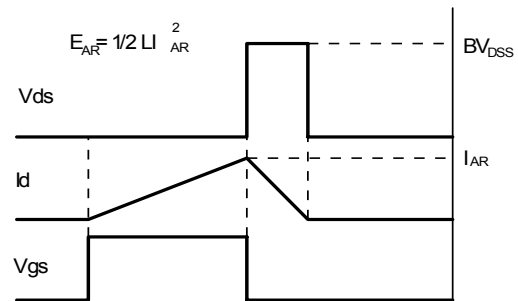
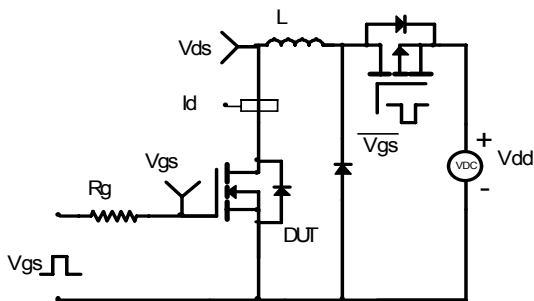
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

