

## Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#)  
[NTDV20P06LT4G](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

# NTD20P06L, NTDV20P06L

## Power MOSFET

-60 V, -15.5 A, Single P-Channel, DPAK

### Features

- Withstands High Energy in Avalanche and Commutation Modes
- Low Gate Charge for Fast Switching
- AEC Q101 Qualified – NTDV20P06L
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Bridge Circuits
- Power Supplies, Power Motor Controls
- DC-DC Conversion

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	-60	V
Gate-to-Source Voltage	Continuous		V <sub>GS</sub> ± 20 V
	Non-Repetitive	t <sub>p</sub> ≤ 10 ms	V <sub>GSM</sub> ± 30
Continuous Drain Current (Note 1)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub> -15.5 A
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub> 65 W
Pulsed Drain Current	t <sub>p</sub> = 10 μs	I <sub>DM</sub>	± 50 A
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>STG</sub>	-55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy (V <sub>DD</sub> = 25 V, V <sub>GS</sub> = 5 V, I <sub>PK</sub> = 15 A, L = 2.7 mH, R <sub>G</sub> = 25 Ω)	E <sub>AS</sub>	304	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain)	R <sub>θJC</sub>	2.3	°C/W
Junction-to-Ambient – Steady State (Note 1)	R <sub>θJA</sub>	80	
Junction-to-Ambient – Steady State (Note 2)	R <sub>θJA</sub>	110	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq.)

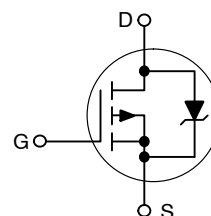


ON Semiconductor®

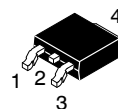
http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX (Note 1)
-60 V	130 mΩ @ -5.0 V	-15.5 A

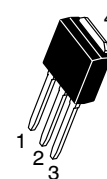
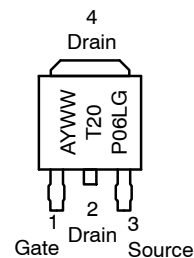
### P-Channel



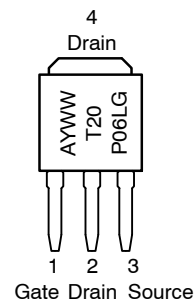
### MARKING DIAGRAMS



DPAK CASE 369C STYLE 2



IPAK/DPAK CASE 369D STYLE 2



20P06L Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

## NTD20P06L, NTDV20P06L

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
-----------	--------	----------------	-----	-----	-----	-------

**OFF CHARACTERISTICS**

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-60	-74		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			-64		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = -60\text{ V}$			-1.0	$\mu\text{A}$
					-10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

**ON CHARACTERISTICS** (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-1.0	-1.5	-2.0	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.1		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -5.0\text{ V}, I_D = -7.5\text{ A}$		0.130	0.150	$\Omega$
		$V_{GS} = -5.0\text{ V}, I_D = -15\text{ A}$		0.143		
Forward Transconductance	$g_{FS}$	$V_{DS} = -10\text{ V}, I_D = -7.5\text{ A}$		11		S
Drain-to-Source On-Voltage	$V_{DS(on)}$	$V_{GS} = -5.0\text{ V}, I_D = -7.5\text{ A}$			-1.2	V
					-1.9	

**CHARGES AND CAPACITANCES**

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -25\text{ V}$		740	1190	pF
Output Capacitance	$C_{OSS}$			207	300	
Reverse Transfer Capacitance	$C_{RSS}$			66	120	
Total Gate Charge	$Q_G(TOT)$	$V_{GS} = -5.0\text{ V}, V_{DS} = -48\text{ V}, I_D = -18\text{ A}$		15	26	nC
Gate-to-Source Charge	$Q_{GS}$			4.0		
Gate-to-Drain Charge	$Q_{GD}$			7.0		

**SWITCHING CHARACTERISTICS** (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5.0\text{ V}, V_{DD} = -30\text{ V}, I_D = -15\text{ A}, R_G = 9.1\ \Omega$		11	20	ns
Rise Time	$t_r$			90	180	
Turn-Off Delay Time	$t_{d(OFF)}$			28	50	
Fall Time	$t_f$			70	135	

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = -15\text{ A}$	$T_J = 25^\circ\text{C}$		1.5	2.5	V
			$T_J = 150^\circ\text{C}$		1.3		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = -12\text{ A}$			60		ns
Charge Time	$t_a$				39		
Discharge Time	$t_b$				21		
Reverse Recovery Charge	$Q_{RR}$				0.13		

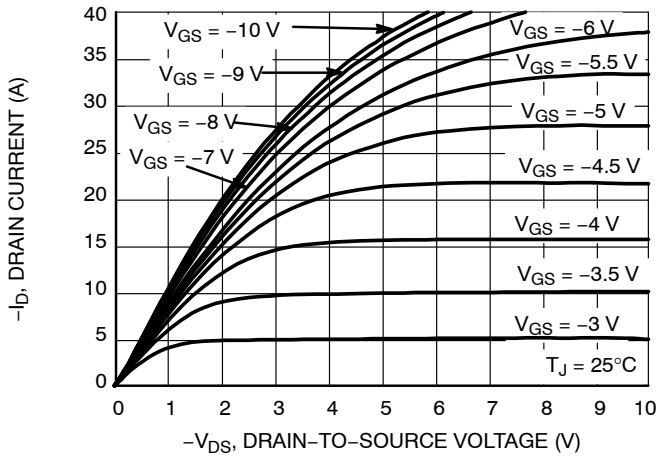
 3. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ 

4. Switching characteristics are independent of operating junction temperatures

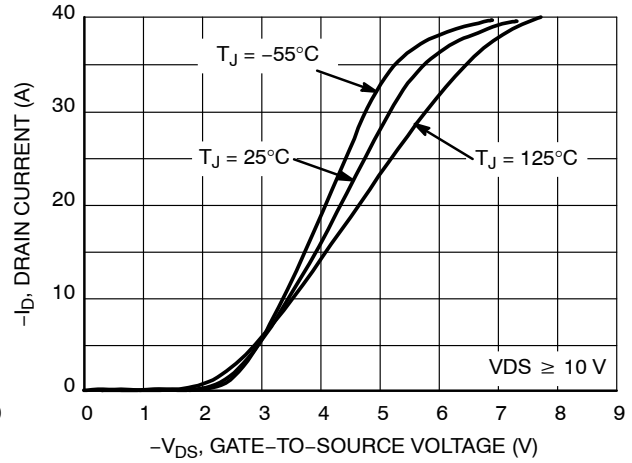
**NTD20P06L, NTDV20P06L**

**TYPICAL PERFORMANCE CURVES**

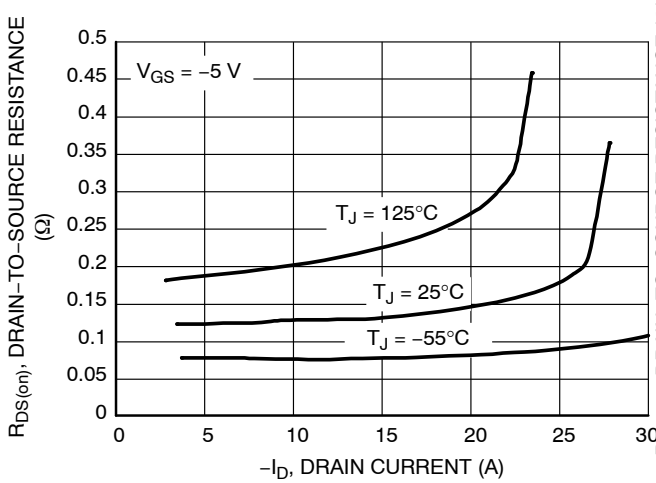
( $T_J = 25^\circ\text{C}$  unless otherwise noted)



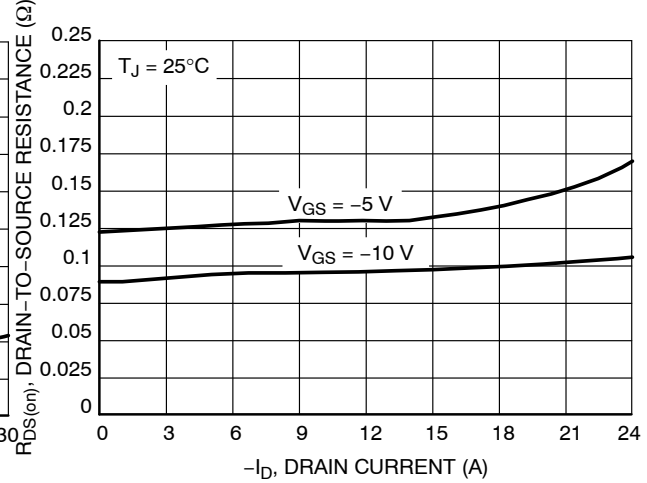
**Figure 1. On-Region Characteristics**



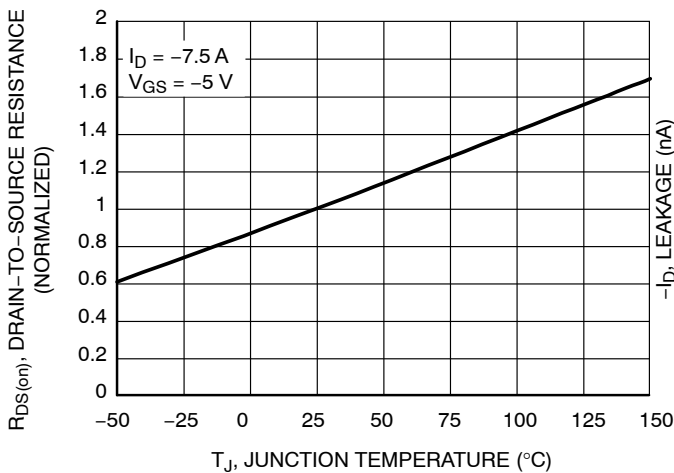
**Figure 2. Transfer Characteristics**



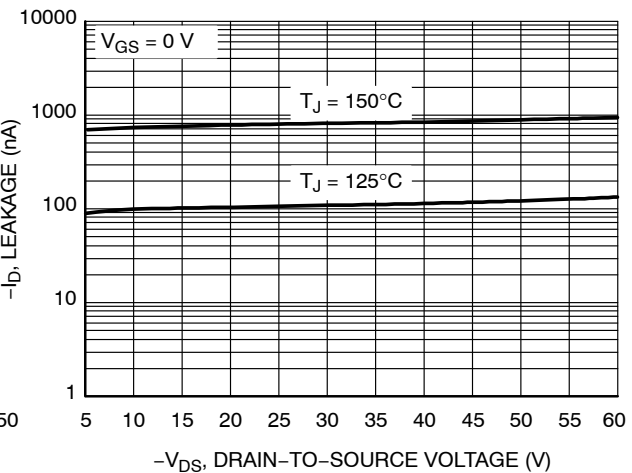
**Figure 3. On-Resistance versus Drain Current and Temperature**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

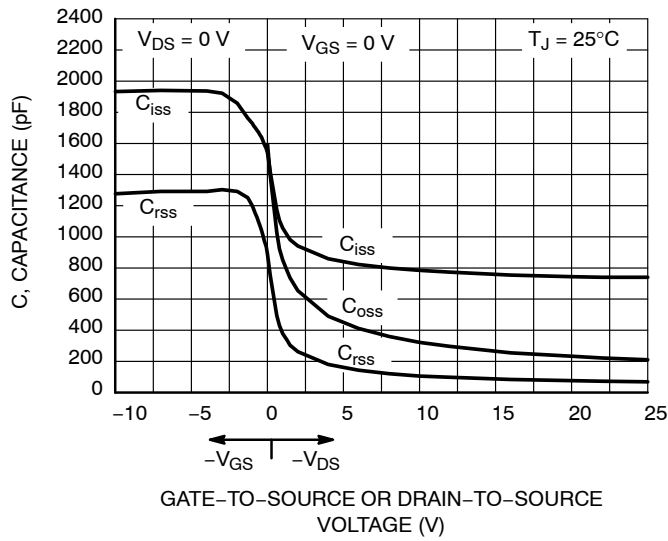


**Figure 5. On-Resistance Variation with Temperature**

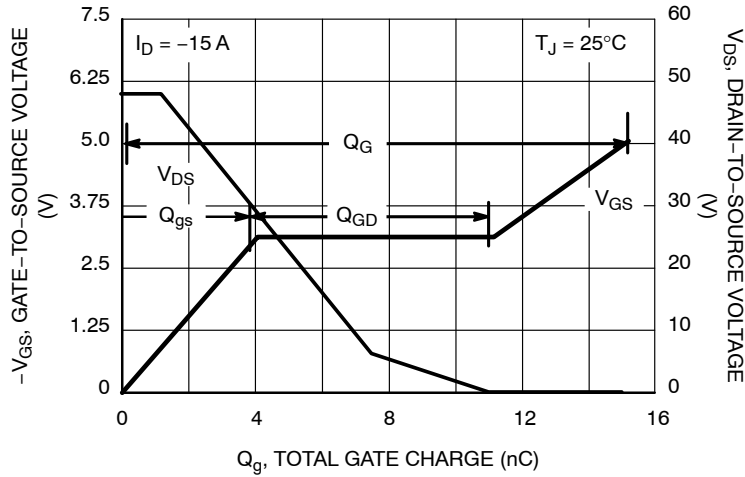


**Figure 6. Drain-to-Source Leakage Current versus Voltage**

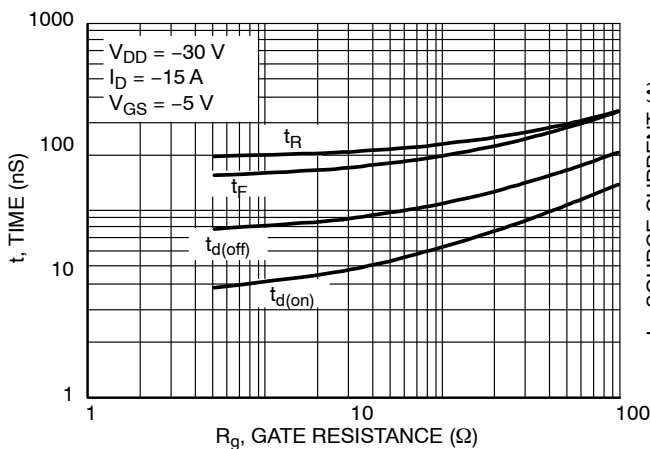
**NTD20P06L, NTDV20P06L**



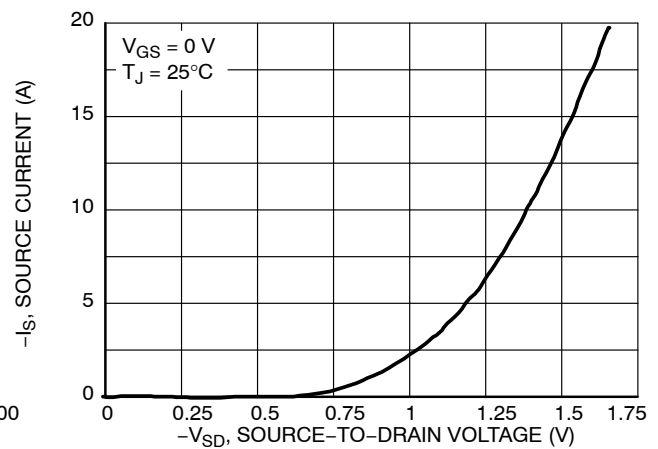
**Figure 7. Capacitance Variation**



**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**

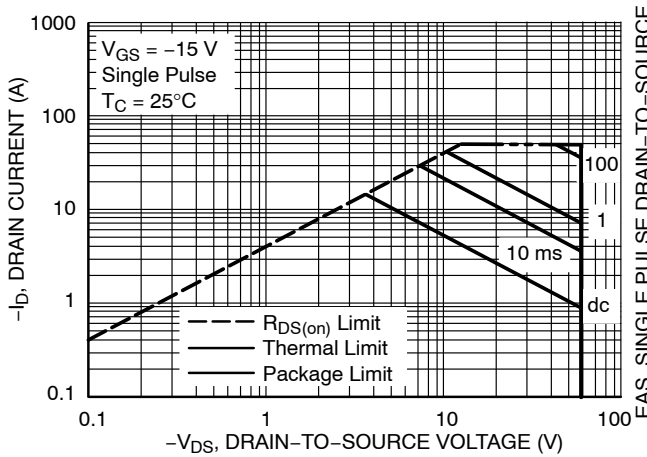


**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

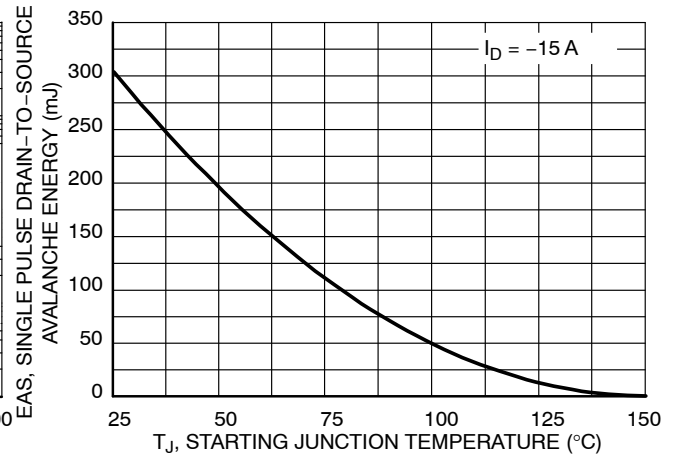


**Figure 10. Diode Forward Voltage versus Current**

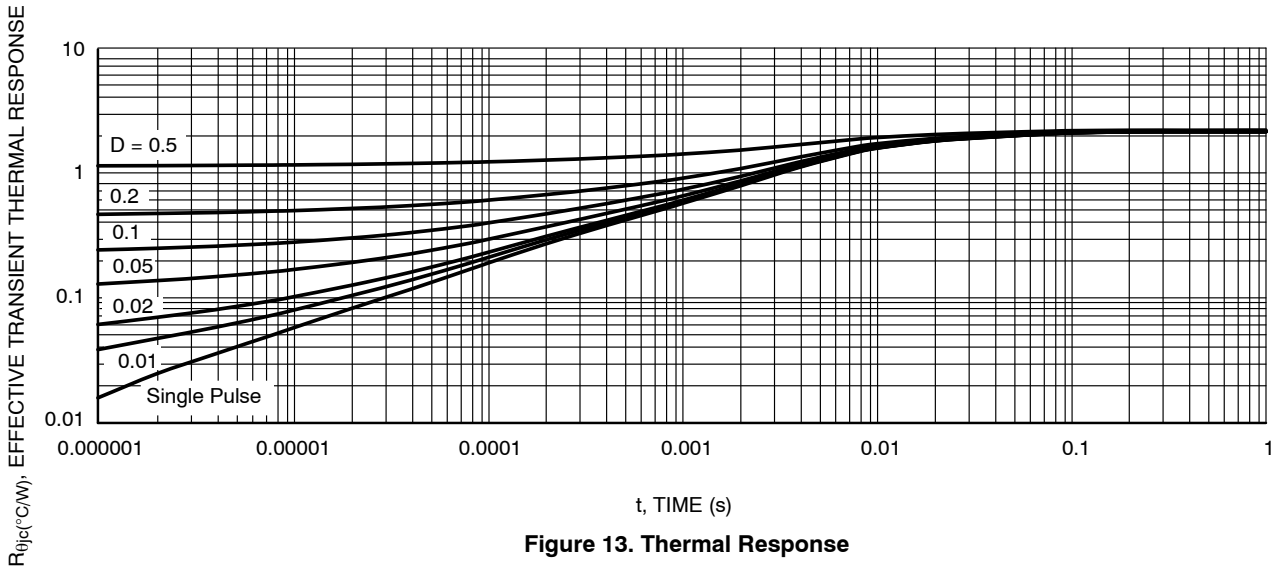
**NTD20P06L, NTDV20P06L**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**



**Figure 13. Thermal Response**

**ORDERING INFORMATION**

Device	Package	Shipping†
NTD20P06LG	DPAK (Pb-Free)	75 Units / Rail
NTD20P06LT4G		2500 / Tape & Reel
NTDV20P06LT4G		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

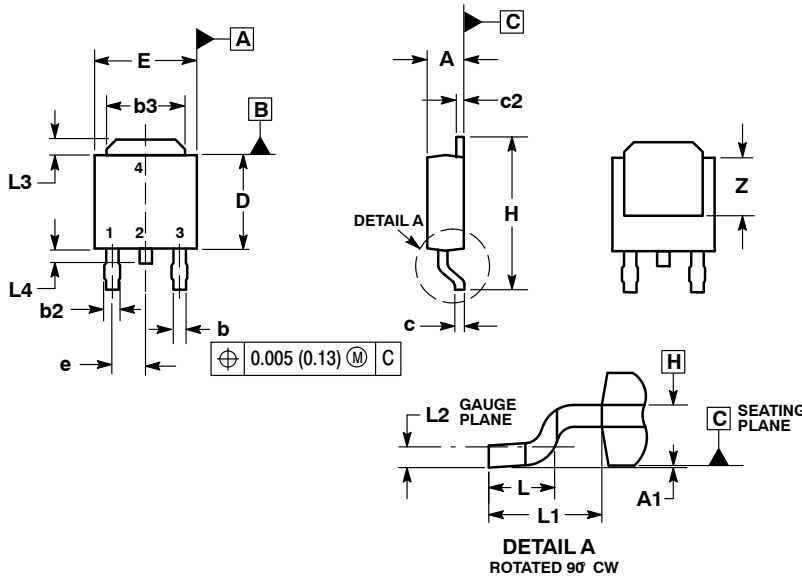
### NTD20P06L, NTDV20P06L

#### PACKAGE DIMENSIONS

#### DPAK (SINGLE GAUGE)

CASE 369C-01

ISSUE D

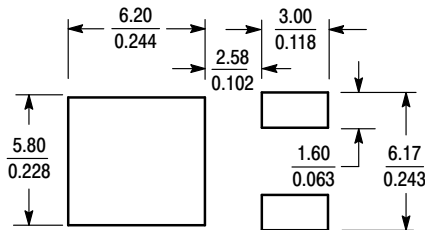


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

#### SOLDERING FOOTPRINT\*



SCALE 3:1 ( $\frac{mm}{inches}$ )

STYLE 2:

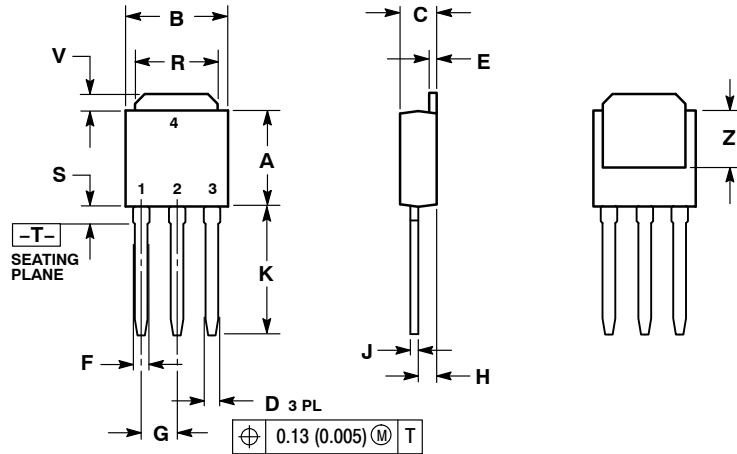
- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## NTD20P06L, NTDV20P06L

### PACKAGE DIMENSIONS


IPAK  
 CASE 369D-01  
 ISSUE C



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

##### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
 P.O. Box 5163, Denver, Colorado 80217 USA  
 Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
 Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
 Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free  
 USA/Canada  
 Europe, Middle East and Africa Technical Support:  
 Phone: 421 33 790 2910  
 Japan Customer Focus Center  
 Phone: 81-3-5773-3850

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative