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Texas Instruments
TPS54120RGYR

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Low-Noise, 1-A Power Supply with Integrated DC-DC Converter and Low-Dropout Regulator

FEATURES

- **Low-Noise Output: 17 μV_{RMS} at 100 Hz to 1 MHz**
- **Wide Input Voltage Range: 4.5 V to 17 V**
- **High Efficiency: 72% at 1 A, 12V Input**
- **Excellent Load/Line Transient Response**
- **Synchronizable to External Clock: 200 kHz to 1.2 MHz**
- **Small Package: 3.5 mm × 5.5 mm QFN-24**

APPLICATIONS

- **Telecom Infrastructure**
- **Pico and Femto Base Stations**
- **Powering Sensitive Clocking Distribution Circuits**
- **Test and Measurement**
- **Powering RF Components: VCOs, Receivers, ADCs**
- **Professional Audio**

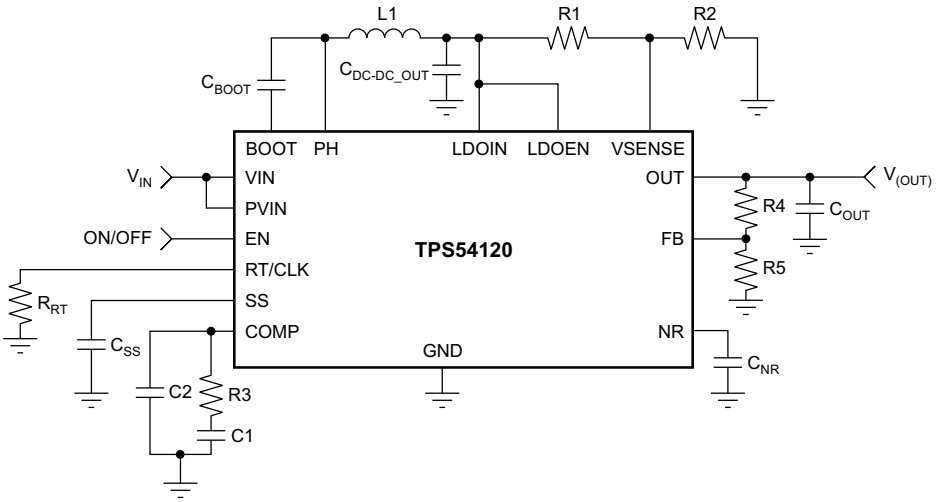
DESCRIPTION

The TPS54120 combines the high-efficiency of a step-down switching (dc-dc) converter with a high power-supply rejection (PSR), low-noise, low-dropout regulator (LDO) to provide an ultra low-noise power supply that delivers quiet power rails to noise-sensitive applications.

With a wide input range of 4.5 V to 17 V, the TPS54120 is ideally suited for systems with 12-V power busses, and supports a 1-A continuous output current. The output voltage can be set from 0.8 V to 6.0 V using external resistors. The dc-dc converter and LDO are completely configurable, allowing the TPS54120 to be used in a wide range of low-noise applications. In addition, the TPS54120 includes features such as softstart, switching frequency synchronization, and a power-good signal.

The device is available in a space-saving, 3.5-mm × 5.5-mm QFN package, and is specified to operate over a –40°C to +125°C junction temperature range.

FUNCTIONAL BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED JUNCTION TEMPERATURE RANGE
TPS54120	QFN-24	RGY	-40°C to +125°C

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	VIN, PVIN	–0.3	20	V
	PH	–1	20	V
	PH (10ns transient)	–3	–1	V
	BOOT	–0.3	27	V
	BOOT – PH	0	7	V
	LDOIN, OUT	–0.3	7	
	LDOEN	–0.3	V_{LDOIN} + 0.3(2)	V
	EN, RT/CLK, PWRGD	–0.3	6	V
	VSENSE, COMP, SS	–0.3	3	V
	FB, NR	–0.3	3.6	V
Current	OUT	Internally limited		A
	RT/CLK	±100		µA
	PH	Internally limited		A
	PVIN	Internally limited		A
	COMP	±200		µA
	PWRGD (sinking)	–0.1	5	mA
Temperature	Operating junction, T_J	–40	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge ratings	Human body model (HBM)		2	kV
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) V_{EN} absolute maximum rating is V_{LDOIN} + 0.3 V or +7.0 V, whichever is smaller.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54120 RGY (QFN) 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	45.1	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	48.2	
θ_{JB}	Junction-to-board thermal resistance	22.0	
ψ_{JT}	Junction-to-top characterization parameter	2.1	
ψ_{JB}	Junction-to-board characterization parameter	21.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	8.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At T_J = –40°C to +125°C, $V_{(PVIN)}$ = $V_{(VIN)}$ = 12 V, $V_{(LDOIN)}$ = DC-DC_OUT(1) = 4.1 V, $V_{(OUT)}$ = 3.3 V, $I_{(OUT)}$ = 10 mA, $V_{(EN)}$ = floating, $C_{(OUT)}$ = 100 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS54120 MIN	TPS54120 TYP	TPS54120 MAX	UNIT
POWER SUPPLY (VIN AND PVIN PINS)						
$V_{(PVIN)}$	PVIN pin input voltage range		1.6		17	V
$V_{(VIN)}$	VIN pin input voltage range		4.5		17	V
	UVLO threshold	VIN rising		4.0	4.5	V
	UVLO hysteresis			150		mV
$I_{SD(VIN)}$	VIN pin shutdown current	$V_{(EN)}$ = 0 V		2	5	µA
I_{OP}	VIN pin operating current (no switching)	$V_{(VSENSE)}$ = 810 mV		600	800	µA
DC-DC BOOT (BOOT PIN)						
	(V_{BOOT} – V_{PH}) UVLO			2.1	3	V
DC-DC CONVERTER ENABLE (EN PIN)						
$V_{IL(EN)}$	EN pin low-level input voltage	Falling	1.10	1.17		V
$V_{IH(EN)}$	EN pin threshold	Rising		1.21	1.26	V
$I_{(EN)}$	EN pin input current	$V_{(EN)}$ = 1.1 V		1.15		µA
	EN pin hysteresis current	$V_{(EN)}$ = 1.3 V		3.4		µA
DC-DC CONVERTER VOLTAGE REFERENCE						
V_{ref}	Reference voltage	0 A ≤ $I_{(OUT)}$ ≤ 1 A	0.792	0.800	0.808	V
DC-DC MOSFET						
R_{HS}	High-side switch resistance	$V_{(BOOT)}$ – $V_{(PH)}$ = 3 V		77		mΩ
		$V_{(BOOT)}$ – $V_{(PH)}$ = 6 V		57	103	mΩ
R_{LS}	Low-side switch resistance	$V_{(VIN)}$ = 12 V		50	87	mΩ
DC-DC ERROR AMPLIFIER						
g_M	Error amplifier transconductance	–2 µA ≤ $I_{(COMP)}$ ≤ 2 µA, $V_{(COMP)}$ = 1 V		1300		µMho
	Error amplifier dc gain	$V_{(SENSE)}$ = 0.8 V	1000	3100		V/V
$I_{(COMP)}$	Error amplifier output current	$V_{(COMP)}$ = 1 V, 100-mV input overdrive		±110		µA
	Switching start threshold			0.25		V
	COMP pin to I_{SWITCH} g_M			12		A/V
DC-DC CURRENT LIMIT						
$I_{LIM(HS)}$	High-side switch current limit		4.2	6.2		A
$I_{LIM(LS)}$	Low-side switch current limit	Sourcing	3.8	5.8		A
		Sinking	1	2.6		A
	Wait time before triggering protection			512		cycles
	Wait time before start			16384		cycles
DC-DC SOFT-START (SS PIN)						
	SS pin charge current			2.3		µA
	SS pin to VSENSE pin matching	$V_{(SS)}$ = 0.4 V		29	60	mV
DC-DC POWER GOOD (PWRGD PIN)						
	VSENSE pin threshold	VSENSE falling (fault, undervoltage)		0.91V_{ref}		V
		VSENSE rising (good, undervoltage)		0.94V_{ref}		V
		VSENSE rising (fault, overvoltage)		1.09V_{ref}		V
		VSENSE falling (good, overvoltage)		1.06V_{ref}		V
	High-level output leakage current	$V_{(VSENSE)}$ = V_{ref}, $V_{(PWRGD)}$ = 5.5 V		30	100	nA
	Low-level output voltage	$I_{(PWRGD)}$ = 2 mA			0.3	V
	Minimum VIN voltage for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		0.6	1	V
	Minimum SS voltage for PWRGD valid			1.2	1.4	V

(1) DC-DC_OUT refers to the regulated output voltage of the switching regulator (see Figure 28).

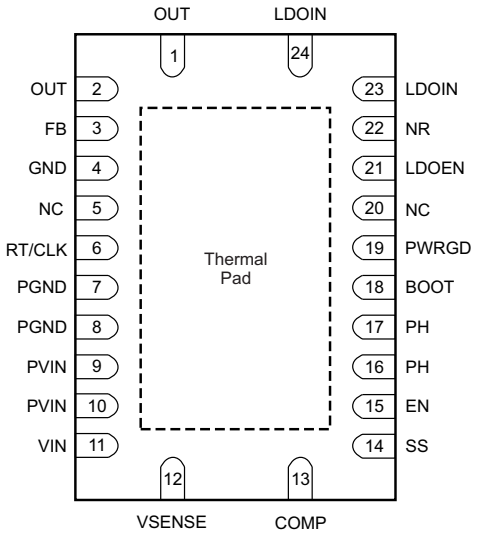
ELECTRICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, $V_{(PVIN)}$ = $V_{(VIN)}$ = 12 V, $V_{(LDOIN)}$ = DC-DC_OUT[1] = 4.1 V, $V_{(OUT)}$ = 3.3 V, $I_{(OUT)}$ = 10 mA, $V_{(EN)}$ = floating, $C_{(OUT)}$ = 100 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS54120			UNIT
			MIN	TYP	MAX	
LDO						
$V_{(LDOIN)}$	LDO input voltage range		2.2		6.5	V
$V_{(FB)}$	FB pin voltage			0.8		V
$V_{(OUT)}$	OUT pin voltage range		$V_{(FB)}$		6.0	V
	OUT pin voltage accuracy	$I_{(OUT)}$ ≤ 1 A, $V_{(OUT\_nom)}$ + 0.5 V ≤ $V_{(LDOIN)}$ ≤ 6.5 V, $V_{(FB)}$ ≤ $V_{(OUT)}$ < 6.0 V	–3.0%	±0.3%	3.0%	
$\Delta V_{O(\Delta IL)}$	Load regulation	100 mA ≤ $I_{(OUT)}$ ≤ 1 A		5		µV/mA
$\Delta V_{O(\Delta VI)}$	Line regulation	$I_{(OUT)}$ = 100 mA, $V_{(OUT\_nom)}$ + 0.5 V ≤ $V_{(LDOIN)}$, 4.5 V ≤ $V_{(VIN)}$ ≤ 17 V		100		µV/V
V_{DO}	LDO dropout voltage	$I_{(OUT)}$ ≤ 1 A, 2.5 V ≤ $V_{(LDOIN)}$ ≤ 6.5 V, $V_{(FB)}$ = GND			500	mV
I_{LIM}	Output current limit	$V_{(OUT)}$ = 0.85 × $V_{(OUT\_nom)}$	1.1	1.4	2	A
$I_{(GND)}$	GND pin current	$I_{(OUT)}$ ≤ 1 A			350	µA
$I_{L(sd\_LDO)}$	Shutdown current ($I_{(GND)}$)	$V_{(EN)}$ < 0.3 V		2		µA
$I_{(FB)}$	FB pin current				1.0	µA
$I_{(LDOEN)}$	LDOEN pin input current	$V_{(EN)}$ = $V_{(LDOIN)}$		20		nA
$V_{IL(LDOEN)}$	LDOEN pin low-level input voltage (disable)				0.4	V
$V_{IH(LDOEN)}$	LDOEN pin high-level input voltage (enable)		1.4			V
DC-DC TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching frequency range (RT mode set point and PLL mode)		200		1200	kHz
	Minimum switching frequency	$R_{(RT)}$ = 240 kΩ (1%)	160	200	240	kHz
	Switching frequency	$R_{(RT)}$ = 100 kΩ (1%)	400	480	560	kHz
	Maximum switching frequency	$R_{(RT)}$ = 40.2 kΩ (1%)	1080	1200	1320	kHz
	RT/CLK high threshold		2			V
	RT/CLK low threshold				0.8	V
	Minimum pulse width			20		ns
	RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		62		ns
PH PIN						
	minimum on time	Measured at 90% of PH, T_A = 25°C, I_{PH} = 2 A		97		ns
	minimum off time	BOOT – PH > 3 V		0		ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+160		°C
		Reset, temperature decreasing		+140		°C
NOISE						
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, $C_{(OUT)}$ = 100 µF, $C_{(NR)}$ = 0.01 µF, $C_{(FB)}$ = 0.01 µF, $I_{(OUT)}$ = 100 mA		9		μV_{RMS}
		BW = 100 Hz to 1 MHz, $C_{(OUT)}$ = 100 µF, $C_{(NR)}$ = 0.01 µF, $C_{(FB)}$ = 0.01 µF, $I_{(OUT)}$ = 100 mA		17		μV_{RMS}
		BW = 10 Hz to 1 MHz, $C_{(OUT)}$ = 100 µF, $C_{(NR)}$ = 0.01 µF, $C_{(FB)}$ = 0.01 µF, $I_{(OUT)}$ = 100 mA		21		μV_{RMS}
		W = 10 Hz to 10 MHz, $C_{(OUT)}$ = 100 µF, $C_{(NR)}$ = 0.01 µF, $C_{(FB)}$ = 0.01 µF, $I_{(OUT)}$ = 100 mA		38		μV_{RMS}

PIN CONFIGURATION

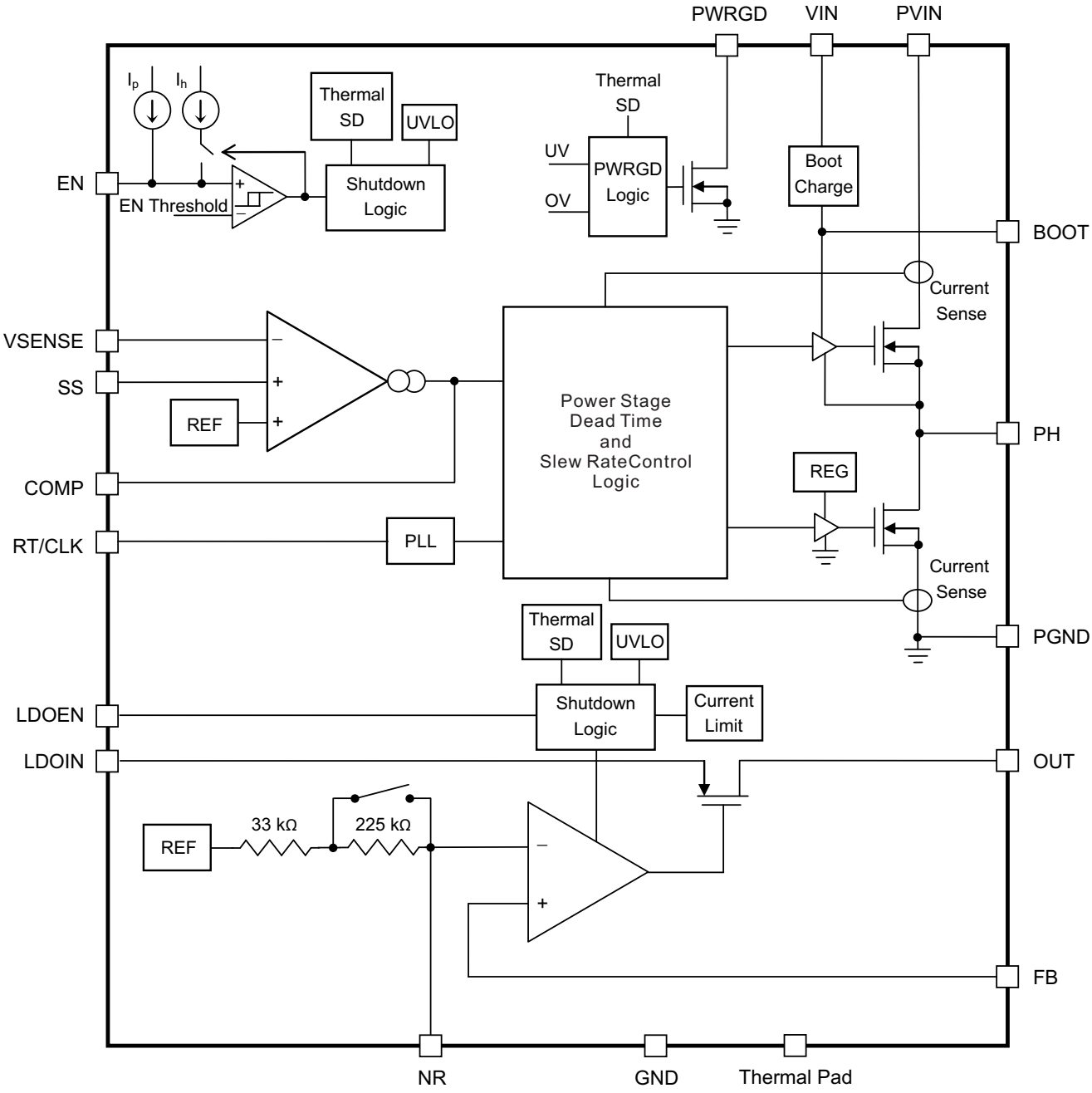
RGY PACKAGE
QFN-24
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
BOOT	18	A bootstrap capacitor is required between the BOOT and PH pins. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET of the dc-dc converter.
COMP	13	DC-DC error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
EN	15	Active-high enable pin for dc-dc converter. Float this pin to enable. Adjust the input undervoltage lockout with two resistors.
FB	3	This pin is the input to the control-loop error amplifier of the LDO and is used to set its output voltage.
GND	4	LDO ground
LDOEN	21	Driving this pin high turns on the LDO regulator. Driving this pin low puts the LDO regulator into shutdown mode. The EN pin must not be left floating and can be connected to LDOIN if not used.
LDOIN	23, 24	LDO input
NC	5, 20	No internal connection
NR	22	LDO noise reduction pin. Connect an external capacitor between this pin and ground to reduce output noise to very low levels, and slow down the VOUT ramp (RC soft-start) of the LDO.
OUT	1, 2	LDO output. A 4.7-µF or larger capacitor is required for stability.
PGND	7, 8	Return for the dc-dc control circuitry and low-side power MOSFET of the dc-dc converter.
PH	16, 17	DC-DC converter switch node
PVIN	9, 10	DC-DC converter power input. Supplies the power switches of the dc-dc converter.
PWRGD	19	Open-drain power good fault pin for the dc-dc converter output. Asserts low as a result of thermal shutdown, undervoltage, overvoltage, EN pin shutdown, or during soft-start of the dc-dc converter.
RT/CLK	6	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock.
SS	14	DC-DC converter soft-start pin. Connect an external capacitor to this pin to set the internal reference voltage rise time on the dc-dc converter. The voltage on this pin overrides the internal reference on the dc-dc converter.
VIN	11	Supplies the control circuitry of the dc-dc converter.
VSENSE	12	Inverting input of the g_M error amplifier of the dc-dc converter.
Thermal pad		GND; for best noise performance, the thermal pad should be connected to the LDO GND and to a large ground pad for thermal dissipation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At $V_{(PVIN)} = V_{(VIN)}$= 12 V, $V_{(LDOIN)}$ = DC-DC_OUT = 4.1 V, $V_{(OUT)}$ = 3.3 V, $I_{(OUT)}$ = 10 mA, $V_{(EN)}$ = floating, C_{OUT} = 100 µF, and $C_{SS} = C_{NR}$ = 0.01µF (see Figure 28), unless otherwise noted.

LOAD REGULATION

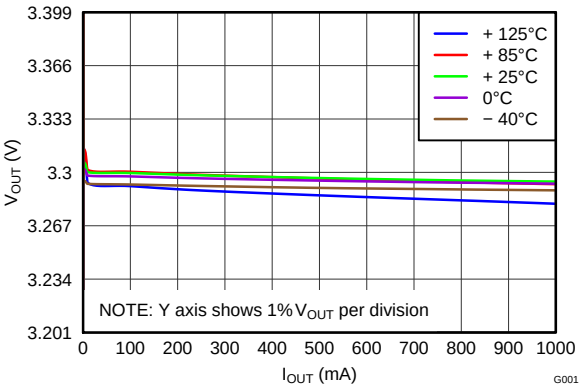


Figure 1.

LOAD REGULATION UNDER LIGHT LOADS

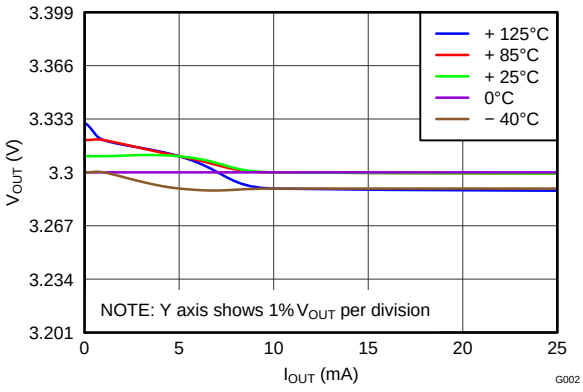


Figure 2.

LINE REGULATION

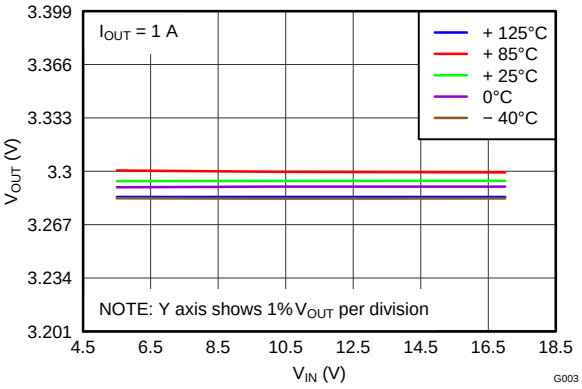


Figure 3.

LINE REGULATION UNDER LIGHT LOADS

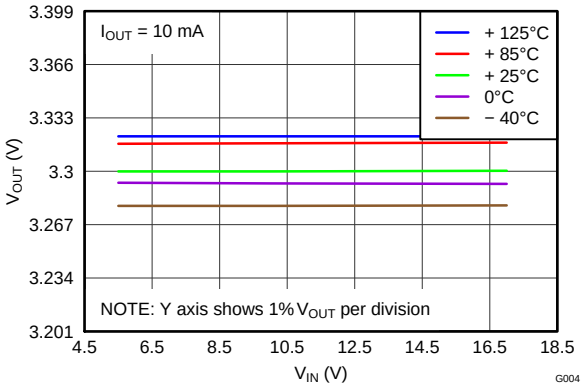


Figure 4.

LDO DROPOUT VOLTAGE vs LDO INPUT VOLTAGE

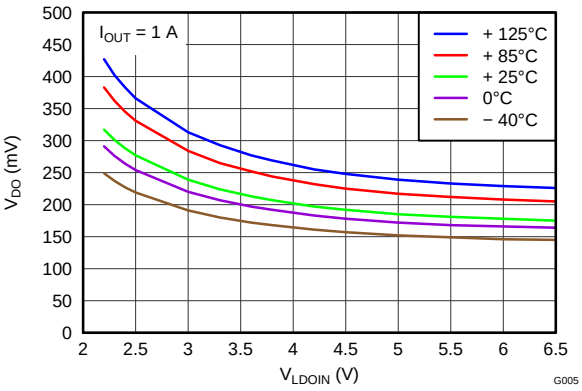


Figure 5.

POWER-SUPPLY RIPPLE REJECTION vs LDO DROPOUT VOLTAGE

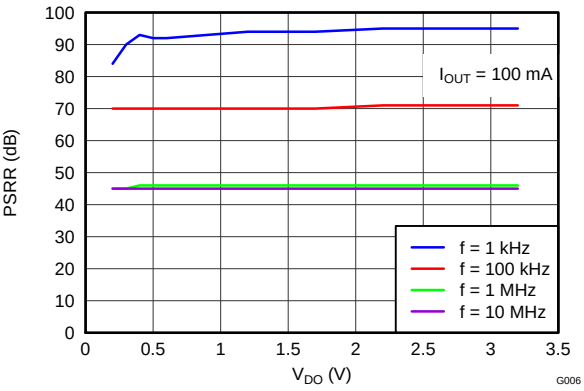


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $V_{(PVIN)}$ = $V_{(VIN)}$= 12 V, $V_{(LDOIN)}$ = DC-DC_OUT = 4.1 V, $V_{(OUT)}$ = 3.3 V, $I_{(OUT)}$ = 10 mA, $V_{(EN)}$ = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01µF (see Figure 28), unless otherwise noted.

POWER-SUPPLY RIPPLE REJECTION vs LDO DROPOUT VOLTAGE

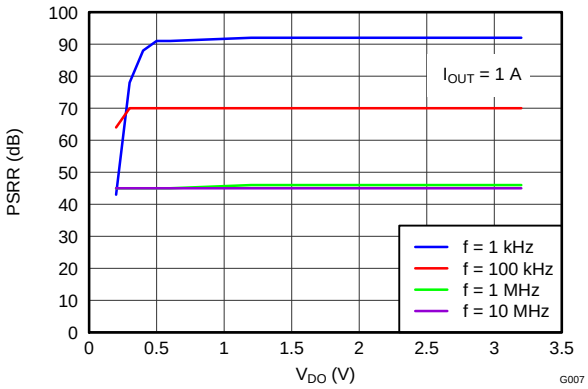


Figure 7.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

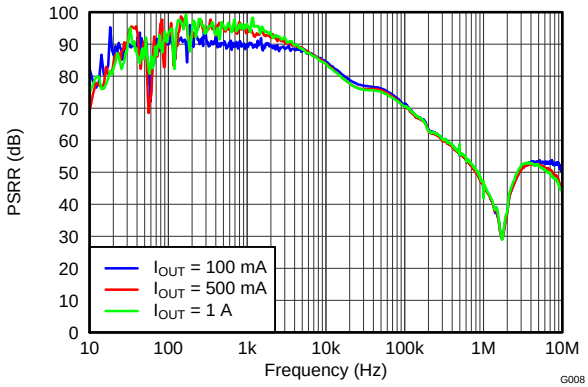


Figure 8.

LDO OUTPUT CURRENT LIMIT vs TEMPERATURE

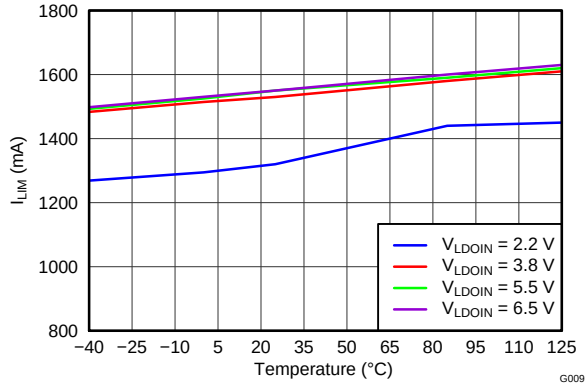


Figure 9.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

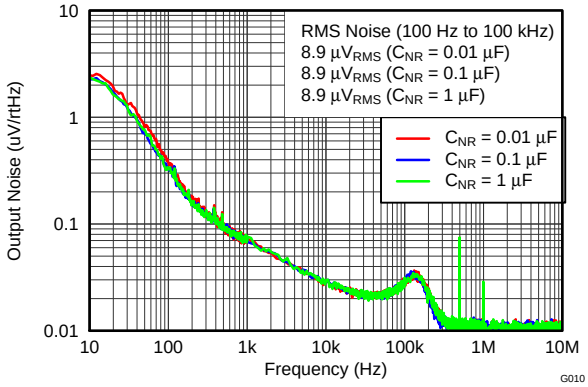


Figure 10.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

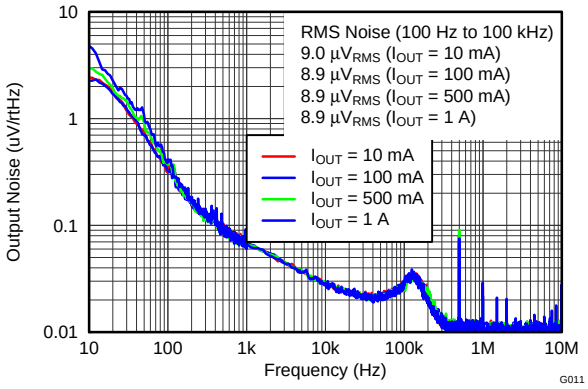


Figure 11.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

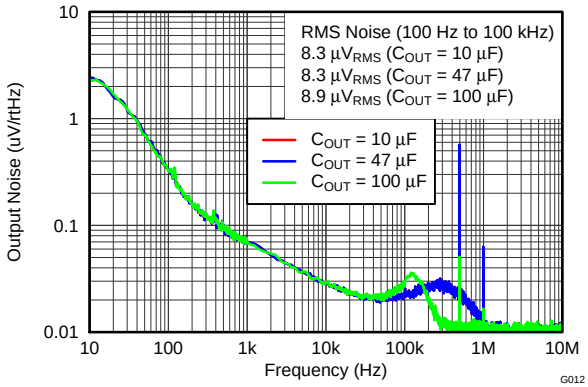


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At $V_{(PVIN)}$ = $V_{(VIN)}$= 12 V, $V_{(LDOIN)}$ = DC-DC_OUT = 4.1 V, $V_{(OUT)}$ = 3.3 V, $I_{(OUT)}$ = 10 mA, $V_{(EN)}$ = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01µF (see Figure 28), unless otherwise noted.

START-UP TIME vs LDO NOISE-REDUCTION CAPACITANCE

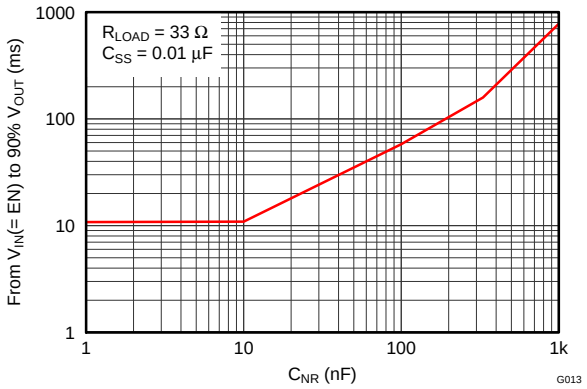


Figure 13.

LINE TRANSIENT RESPONSE

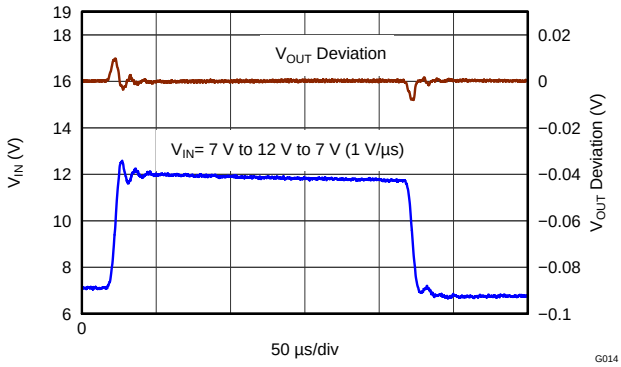


Figure 14.

LOAD TRANSIENT RESPONSE

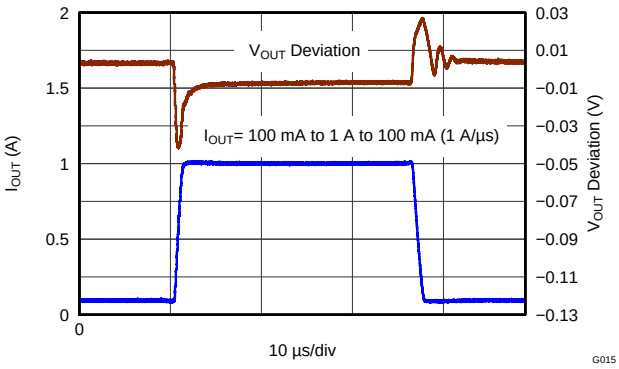


Figure 15.

ENABLE PULSE RESPONSE

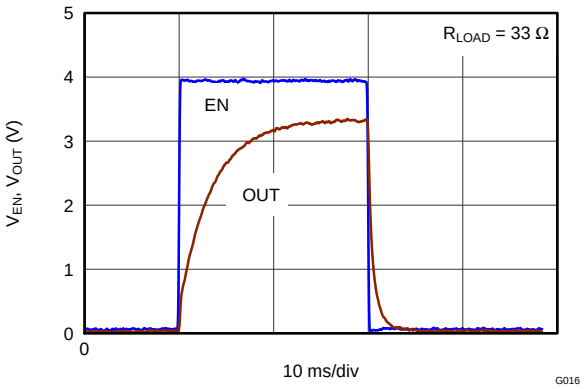


Figure 16.

POWER-UP/POWER-DOWN RESPONSE

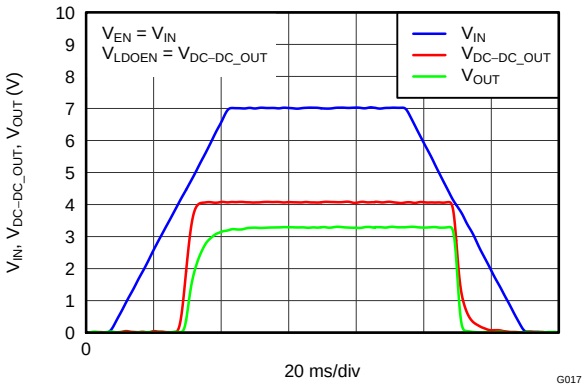


Figure 17.

OSCILLATOR FREQUENCY vs TEMPERATURE

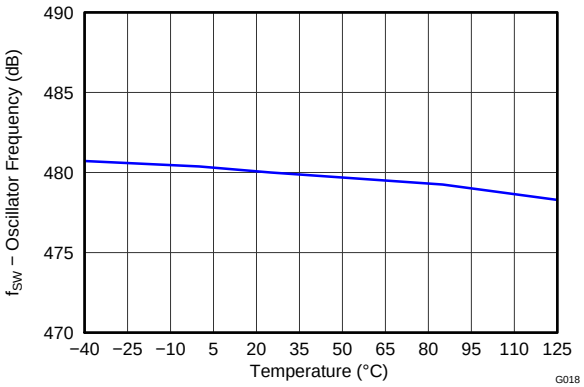


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At $V_{(PVIN)}$ = $V_{(VIN)}$= 12 V, $V_{(LDOIN)}$ = DC-DC_OUT = 4.1 V, $V_{(OUT)}$ = 3.3 V, $I_{(OUT)}$ = 10 mA, $V_{(EN)}$ = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01µF (see Figure 28), unless otherwise noted.

EN PIN HYSTERESIS CURRENT vs TEMPERATURE

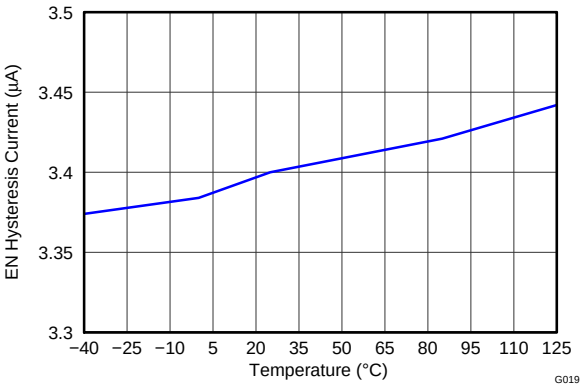


Figure 19.

EN PIN PULL-UP CURRENT vs TEMPERATURE

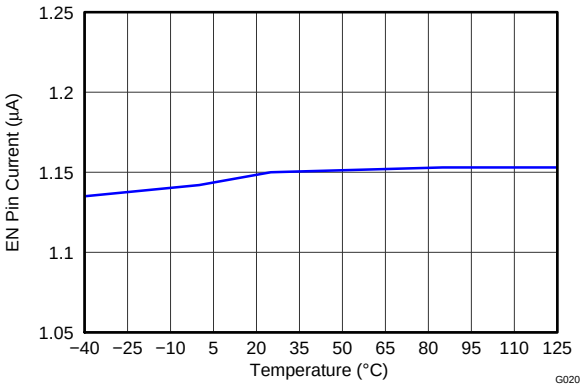


Figure 20.

EN PIN UVLO THRESHOLD vs TEMPERATURE

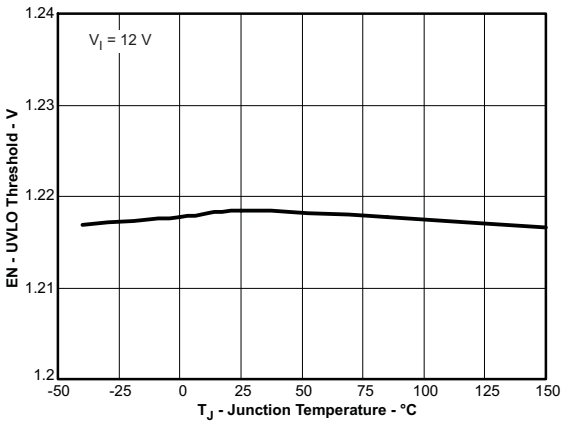


Figure 21.

SLOW-START CHARGE CURRENT vs TEMPERATURE

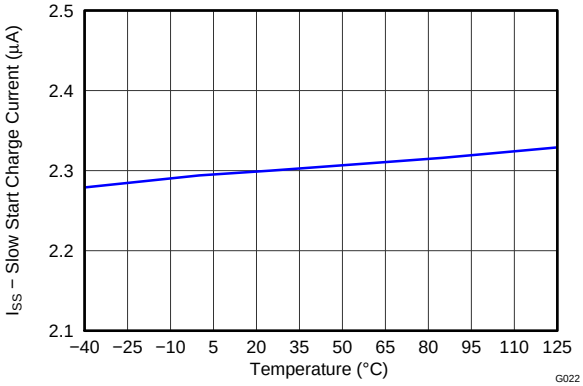


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At $V_{(PVIN)}$ = $V_{(VIN)}$= 12 V, $V_{(LDOIN)}$ = DC-DC_OUT = 4.1 V, $V_{(OUT)}$ = 3.3 V, $I_{(OUT)}$ = 10 mA, $V_{(EN)}$ = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01µF (see Figure 28), unless otherwise noted.

PWRGD PIN THRESHOLD vs TEMPERATURE

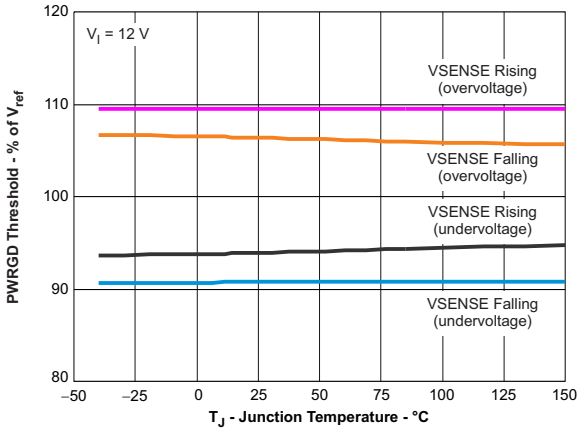


Figure 23.

HIGH-SIDE CURRENT LIMIT vs TEMPERATURE

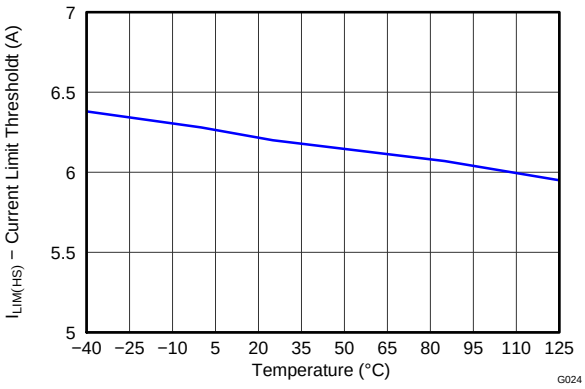


Figure 24.

MINIMUM CONTROLLABLE ON-TIME vs TEMPERATURE

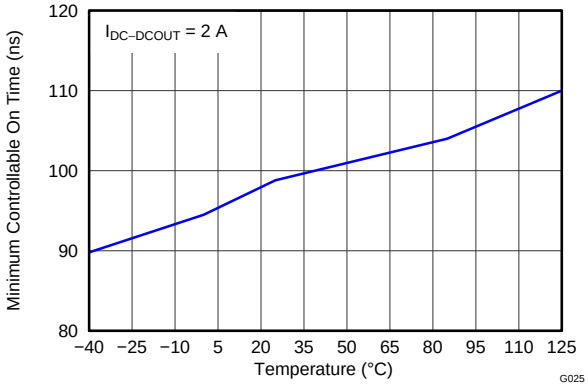


Figure 25.

MINIMUM CONTROLLABLE DUTY RATIO vs TEMPERATURE

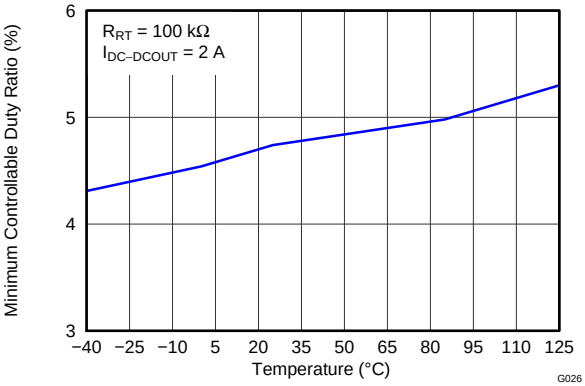


Figure 26.

EFFICIENCY vs LOAD CURRENT

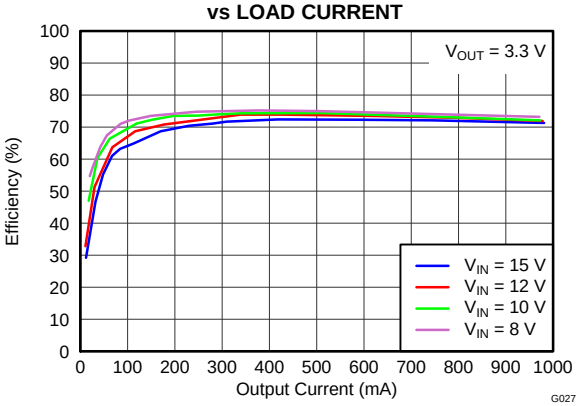


Figure 27.

DETAILED DESCRIPTION

TYPICAL APPLICATION

Figure 28 shows a typical application diagram for the TPS54120.

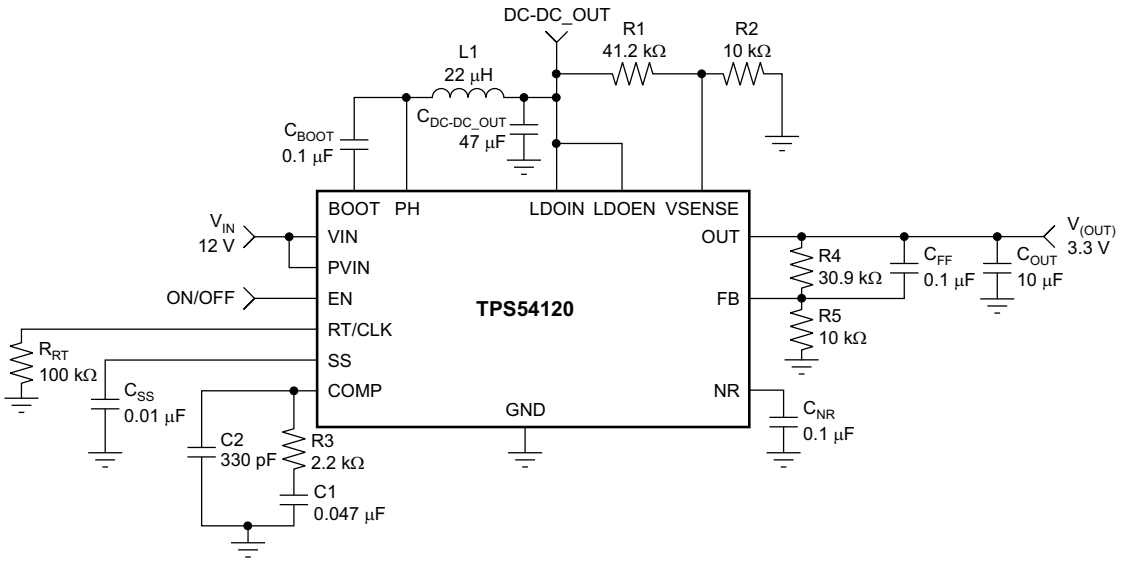


Figure 28. Typical Application

OVERVIEW

The TPS54120 is a low-noise power supply that delivers a quiet power rail to noise-sensitive components. This device combines a current mode-controlled, dc-dc step-down (buck) regulator and a low-noise, wide-bandwidth low dropout (LDO) regulator to create an efficient, stable, low-noise power supply. The TPS54120 is fully characterized for noise performance, thus allowing for easy creation of a quiet power supply. The device includes features such as soft-start, clock synchronization, and a power-good signal, making it well suited as a power supply for communication, test and measurement, and audio equipment applications. Both the integrated switching regulator and LDO are fully configurable, allowing for complete design flexibility. In addition, a simplified design procedure enables quick development of a power supply custom-suited to specific requirements.

INPUT VOLTAGE RANGE

VIN AND POWER VIN (PVIN)

The TPS54120 allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the switching regulator. The PVIN pin voltage provides the input voltage to the power converter system of the switching regulator.

If tied together, the input voltage for VIN and PVIN can range from 4.5 V to 17 V. If using the VIN separately from PVIN, the VIN pin must be between 4.5 V and 17 V, and the PVIN pin can range from as low as 1.6 V to 17 V. A voltage divider connected to the EN pin can adjust either input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power up behavior; refer to the *Device Enable and Undervoltage Lockout Adjustment* section for more information.

LDO INPUT VOLTAGE (LDOIN)

The minimum input voltage that can be applied to the LDO of the TPS54120 is LDOVIN = (VOUT + VDO) or 2.2 V, whichever is greater. The maximum rated voltage into this pin should not exceed 6.5 V. This pin is designed to be connected to the output inductor of the integrated switcher, and should be decoupled to the GND pin with a 1.0 µF ceramic capacitor.

ADJUSTING THE OUTPUT VOLTAGE

The output voltage of both the switcher and the LDO are adjustable. They are set with a resistor divider from the output voltage to the feedback sensing pin. Use 1%-tolerance or better divider resistors for best accuracy.

The values of the LDO feedback resistors can be calculated using Equation 1:

$$V_{(OUT)} = (R_4 + R_5)\, V_{ref} / R_5$$

Where:

V_{ref} = 0.8 V
R4 = The resistor from the output to the FB pin of the LDO.
R5 = The resistor from the FB pin to ground of the LDO. (1)

The values of the switching regulator feedback resistors can be calculated using Equation 2:

$$\text{DC-DC\_OUT} = (R_1 + R_2)\, V_{ref} / R_2$$

Where:

V_{ref} = 0.8 V
R1 = The resistor from the switcher output at the inductor to the VSENSE pin of the switching regulator.
R2 = The resistor from the VSENSE pin to ground switching regulator. (2)

To improve efficiency at light loads, consider using larger-value resistors. Larger-value resistors may increase the noise sensitivity at the VSENSE and FB pins and error from the VSENSE and FB pin input currents. Using a value of 10 kΩ for R2 and R5 provides a good trade-off between these two issues.

POWER CONVERSION EFFICIENCY VERSUS OUTPUT NOISE

The configuration of the TPS54120 consists of a switching regulator followed by an LDO. The ability of the LDO to reject the noise created by the switching regulator and not pass it to the LDO output is determined by the power supply rejection (PSR) of the LDO. The PSR of an LDO depends on the LDO input to LDO output voltage difference. The higher the voltage difference, the better the LDO ability to reject noise at its input. The LDO in the TPS54120 has been designed to provide high, wide-bandwidth PSR with a minimum of input to output voltage differential. At 1 A for the highest PSR performance, the input-to-output voltage differential should be set to 0.8 V or greater.

The LDO voltage differential is also a primary contributor to the overall power loss in the TPS54120. The LDO input and output voltage differentials contribution to the power loss is defined as the output current times the input-to-output voltage differential, as shown in Equation 3:

$$\text{Power Loss from the LDO} = I_{(OUT)} \times (V_{(LDOIN)} - V_{(OUT)}) \quad (3)$$

Therefore, for a 0.8-V drop at 1 A, this loss is 0.8 W. The impact of the power loss can be reduced by lowering V_{DO}; however, the PSR of the LDO may be impacted. In the Typical Characteristics section, Figure 6 and Figure 7 show the trade-off between PSR and V_{DO} for various output current levels and frequencies. For currents less than 500mA, a V_{DO} of 0.5 V does not have significant impact on PSR performance and provides a substantial improvement to the power loss from the V_{DO}.

BOOTSTRAP VOLTAGE AND LOW DROPOUT OPERATION

The TPS54120 has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and the (BOOT – PH) voltage is below regulation. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R- or X5R-grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve dropout, the device is designed to operate at 100% duty cycle, as long as the BOOT to PH pin voltage is greater than the (BOOT – PH) UVLO threshold (typically 2.1 V). When the voltage between BOOT and PH drops below the (BOOT – PH) UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails, 100% duty-cycle operation can be achieved as long as (VIN – PVIN) > 4V and ($V_{(BOOT)}$ – $V_{(PH)}$) > 2.1V; the UVLO threshold for the BOOT pin.

NOTE

A boot resistor in series with the boot capacitor should never be used on the TPS54120.

OUTPUT OVERVOLTAGE PROTECTION (OVP)

The TPS54120 has an overvoltage protection (OVP) circuit on the switcher output to minimize overshoots on the switcher output. This also protects the input of the LDO from experiencing overshoot above its rated values.

CAUTION

Any voltage above the absolute maximum rated input voltage into the LDOIN pin can damage the device.

When the power-supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable amount of time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the dc-dc output voltage can respond faster than the error amplifier. This leads to the possibility of a switcher output overshoot.

The OVP feature minimizes overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops below the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

OVERCURRENT PROTECTION

SWITCHER OVERCURRENT PROTECTION

The integrated switcher of the TPS54120 is protected from overcurrent conditions by using cycle-by-cycle current limiting on both MOSFETs, the low-side and the high-side.

HIGH-SIDE MOSFET OVERCURRENT PROTECTION

High-side MOSFET overcurrent protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET on a cycle-by-cycle basis. If this current exceeds the current limit threshold, the high-side MOSFET is turned off for the remainder of that switching cycle. During normal operation, the device implements current mode control. Current mode control uses the COMP pin voltage to control the turn-off of the high-side MOSFET and the turn-on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle, the switch current and the current reference generated by the COMP pin voltage are compared. When the peak switch current intersects the current reference, the high-side switch is turned off.

LOW-SIDE MOSFET OVERCURRENT PROTECTION

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current falls below the low-side sourcing current limit at the start of a cycle. The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs remain off until the start of the next cycle.

If an output overload condition (as measured by the COMP pin voltage) has lasted longer than the current-limit protection mode wait time (programmed for 512 switching cycles), the device shuts down and restarts after the current-limit protection mode time (set for 16384 cycles). The current-limit protection mode helps to reduce device power dissipation under severe overcurrent conditions

LDO INTERNAL CURRENT LIMIT

In addition to the switcher overcurrent protection, the TPS54120 has an internal current limit on the integrated LDO. The LDO internal current limit helps protect the LDO during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current-limit state for extended periods of time. The PMOS pass element in the integrated LDO has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at LDOIN. This current is not limited, so if extended reverse-voltage operation is anticipated, external limiting may be required.

THERMAL INFORMATION

The internal protection circuitry of the device has been designed to protect against overload conditions. However, this circuitry was not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades device reliability. The TPS54120 has thermal protection for both the switcher and the LDO, and they operate independently of each other.

THERMAL PROTECTION OF THE SWITCHER

The internal thermal-shutdown circuitry of the switcher forces the device to stop switching if the junction temperature exceeds +175°C, typically. The device turns back on when the junction temperature drops below +165°C typically.

THERMAL PROTECTION OF THE LDO

Thermal protection of the integrated LDO disables the output of the TPS54120 when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

ADJUSTABLE SWITCHING FREQUENCY AND SYNCHRONIZATION (RT/CLK)

The RT/CLK pin can be used to set the switching frequency of the device in two modes: RT and CLK.

RT MODE

A resistor, $R_{(RT)}$, is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1200 kHz by using a maximum of 240 kΩ and minimum of 40.2 kΩ, respectively. To determine the value of the RT resistor for a given switching frequency (f_{SW}), use Equation 4 or the curve in Figure 1:

$$R_{RT}\ (k\Omega) = 60281\ f_{SW}^{-1.033}\ (kHz) \quad (4)$$

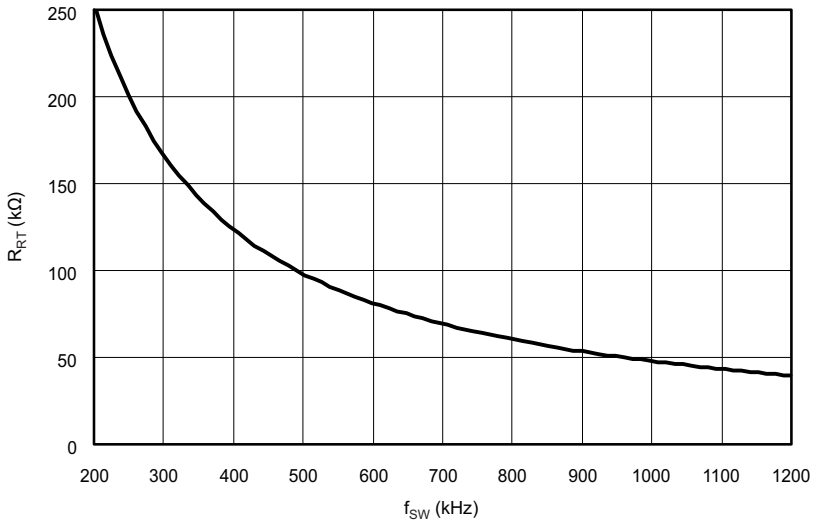


Figure 29. RT Set Resistor vs Switching Frequency

CLK MODE

In CLK mode, an external clock is connected directly to the RT/CLK pin. The device is synchronized to the external clock frequency with a phase-locked loop (PLL). CLK mode overrides RT mode. The device is able to automatically detect the required mode and switch from RT mode to CLK mode. An internal PLL has been implemented to allow synchronization between 200 kHz and 1.2 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square-wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition less than 0.8 V and greater than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are required, the device can be configured to have both RT resistor and external clock connected at the same time to RT/CLK pin. Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, CLK mode overrides RT mode and ignores the RT resistor. The first time the SYNC pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock on to the frequency of the external clock. It is not recommended to switch from the CLK mode back to the RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by RT resistor.

START-UP TIME

SOFT-START OF THE SWITCHER

The rate at which the output voltage of the switcher rises up to the full operational level during the start-up phase is controlled through the SS pin. A capacitor, C_{SS}, is connected between the SS pin and the IC ground. The size of the capacitor determines the soft-start ramp-up time (t_{ss}, 10% to 90%), as shown in Equation 5:

$$t_{SS}\ (ms) = C_{(SS)}\ (nF)\ V_{ref}\ (V)) / I_{SS}\ (\mu A) \quad (5)$$

The device has an internal pull-up current source of 2.3 µA = I_{ss} that charges the external soft-start capacitor, C_{SS}. The voltage reference, V_{ref}, for this device is 0.8 V. Thus, by sourcing a constant current onto the capacitor, the device linearly ramps up the voltage on the SS pin, which corresponds to the voltage on the FB pin and thus, the output voltage of the switcher.

If the input UVLO is triggered, the EN pin is pulled below 1.21 V, or a thermal shutdown event occurs, then the device stops switching and enters low-current operation. At the subsequent power-up, when the shutdown condition is removed, the device does not start switching until it has discharged the SS/TR pin to ground, ensuring proper soft-start behavior.

NR SOFT-START TIME AND LDO START-UP

The NR capacitors main purpose is to filter the noise from the LDO bandgap, and thereby reduce the LDO output noise. However, these capacitors also affect the start-up time of the LDO. The TPS54120 has a quick-start circuit to quickly charge $C_{(NR)}$, if it is present; see the Functional Block Diagram. At start-up, this quick-start switch is closed, creating only 33 kΩ of resistance between the band gap reference and the NR pin. The quick-start switch opens approximately 2 ms after any device enabling event, and the resistance between the band gap reference and the NR pin becomes higher in value (approximately 250 kΩ) to form a very good low-pass (RC) filter. This low-pass filter achieves very good noise reduction for the reference voltage.

Inrush current can be a problem in many applications. The 33-kΩ resistance during the start-up period is intentionally added to slow down the reference voltage ramp up, thus reducing the inrush current. For example, the capacitance of connecting the recommended $C_{(NR)}$ value of 0.01 µF along with the 33-kΩ resistance causes an approximately 1-ms RC delay. Start-up time for the LDO with other $C_{(NR)}$ values can be determined by using Figure 13 or calculated as shown in Equation 6:

$$t_{STR}(s) = 76000 \times C_{(NR)}\ (F) \quad (6)$$

Although the noise reduction effect is nearly saturated at 0.01 µF, connecting a $C_{(NR)}$ value greater than 0.01 µF can help reduce noise slightly more; however, start-up time may become longer because the quick-start switch opens after approximately 2 ms. That is, if CNR is not fully charged during this 2-ms period, $C_{(NR)}$ finishes charging through a higher resistance of 250 kΩ, and takes much longer to fully charge. Note that a low leakage $C_{(NR)}$ should be used; most ceramic capacitors are suitable.

POWER GOOD (PWRGD)

The PWRGD pin is an open drain output. Once the VSENSE pin is between 94% and 106% of the internal voltage reference, the PWRGD pin pull-down is de-asserted and the pin floats. It is recommended to place a 10-kΩ to 100-kΩ pull-up resistor to a voltage source that is less than or equal to 5.5 V. The PWRGD is in a defined state after the VIN input voltage is greater than 1 V, but with reduced current-sinking capability. The PWRGD pin achieves full current-sinking capability after the VIN input voltage is greater than 4.5 V.

The PWRGD pin is pulled low when VSENSE is lower than 91% or greater than 109% of the nominal internal reference voltage. The PWRGD is also pulled low if the input UVLO or thermal shutdown are asserted, the EN pin is pulled low, or the SS/TR pin is less than 1.2 V, typically.

DEVICE ENABLE AND UNDERVOLTAGE LOCKOUT ADJUSTMENT

SWITCHER ENABLE AND UNDERVOLTAGE LOCKOUT

The EN pin is used to turn the switcher on and off. When the EN pin voltage exceeds the threshold voltage, the device begins operating. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low I_Q state.

The EN pin has an internal pull-up current source; float or drive the EN pin to enable the device. If an application requires control of the EN pin, use an open-drain or open-collector output logic to interface with the pin.

The TPS54120 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150 mV.

If an application requires either a higher UVLO threshold on the VIN pin, or a secondary UVLO on the PVIN pin in split-rail applications, then the EN pin can be configured as shown in Figure 30, Figure 31, or Figure 32. When using the external UVLO function, it is recommended to set the hysteresis to be greater than 500 mV.

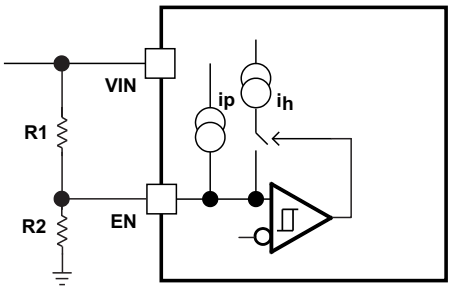


Figure 30. Adjustable VIN Under Voltage Lock Out

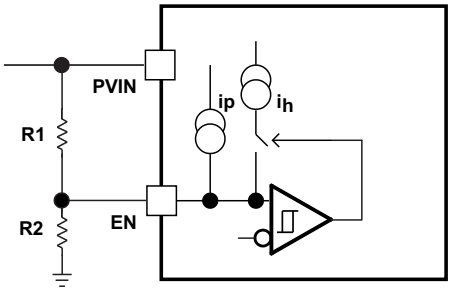


Figure 31. Adjustable PVIN Under Voltage Lock Out, VIN ≥ 4.5V

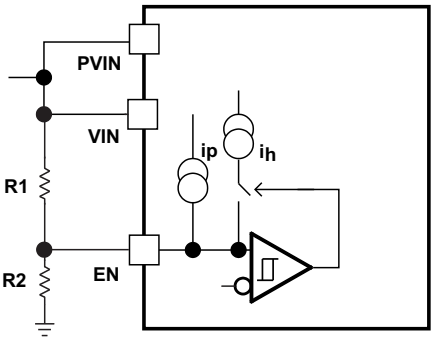


Figure 32. Adjustable VIN and PVIN Under Voltage Lock Out

The EN pin has a small pull-up current (I_p) that sets the state of the pin to enable (default) when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h when the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 7 and Equation 8.

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1-\frac{V_{ENFALLING}}{V_{ENRISING}}\right)+I_h} \quad (7)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (8)$$

LDO ENABLE AND UNDERVOLTAGE LOCKOUT

The LDO enable pin (LDOEN) is active-high and compatible with standard and low-voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

The LDO also has a fixed UVLO to keep the output shut off until the LDO internal circuitry is working properly. The LDO UVLO circuit has a deglitch feature that ignores undershoot transients on the LDO input if they are less than 50 µs in duration.

SEQUENCING

The TPS54120 is easy to use and suited for applications that require tracking and sequencing. It has a built-in power good function to indicate the status of the device, a soft-start circuit to control the output voltage slope during start-up, noise reduction with start-up time for the LDO, and an enable function for independently controlling the start-up of both the LDO and the switcher. Each of these functions is useful for tracking and sequencing applications. See Application Report SLVA497, *TPS54120 Sequencing and Tracking*, for more details regarding the sequencing application setup of the TPS54120.

SWITCHER PWM CONTROL AND CONTINUOUS CURRENT MODE OPERATION (CCM)

The integrated switcher of the TPS54120 uses adjustable, fixed-frequency, peak-current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier that drives the COMP pin. An internal oscillator turns on the high-side power switch. The error amplifier output is converted into a current reference that is compared to the high-side power switch current. When the power-switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on. The device normally works in continuous conduction mode (CCM) under all load conditions.

SMALL-SIGNAL MODEL FOR LOOP RESPONSE

Figure 33 shows an equivalent model for the device control loop. This model can be run in a circuit simulation program to check frequency and transient responses. The error amplifier is a transconductance amplifier with a g_M of 1300 mA/V, and can be modeled using an ideal voltage-controlled current source. Resistor Roea (2.38 MΩ) and capacitor Coea (20.7 pF) model the open-loop gain and frequency response of thSLVA497e error amplifier.

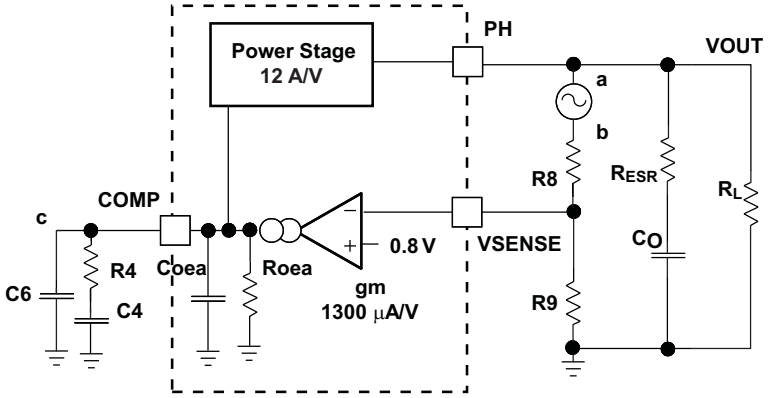


Figure 33. Small-Signal Model for Loop Response

The 1-mV ac voltage source between nodes *a* and *b* effectively breaks the control loop for the frequency-response measurements. Plotting a/c and c/b show the small-signal responses of the power stage and frequency compensation, respectively. Plotting a/b shows the small-signal response of the overall loop. The dynamic loop response can be checked by replacing R_L with a current source that has the appropriate load step amplitude and step rate in a time-domain analysis. Refer to Application Report SLVA503, *Understanding Compensation Network for the TPS54120*, for a more detailed treatment of the small-signal model and compensation for the TPS54120.

APPLICATION INFORMATION

DESIGN METHODOLOGY

The TPS54120 has a low-noise output voltage range from 0.8 V to 6.0 V with an output current of up to 1 A. To simplify design efforts using the TPS54120, typical designs for common applications are listed in Table 1 according to the typical schematic diagram shown in Figure 34. For more details about designing with the TPS54120, refer to Application Report SLVA506, *Design Procedure for the TPS54120*, and SLVC411, the *TPS54120 Design Tool Calculator*.

The TPS54120 can also be configured to provide two separate power rails: one from the switching regulator and one from the LDO. For more information on how to create a dual-rail power supply from the TPS54120, refer to Application Report SLVA502, *Design Guidelines for TPS54120 as a 3-A Switcher and 1-A Switcher Plus LDO*.

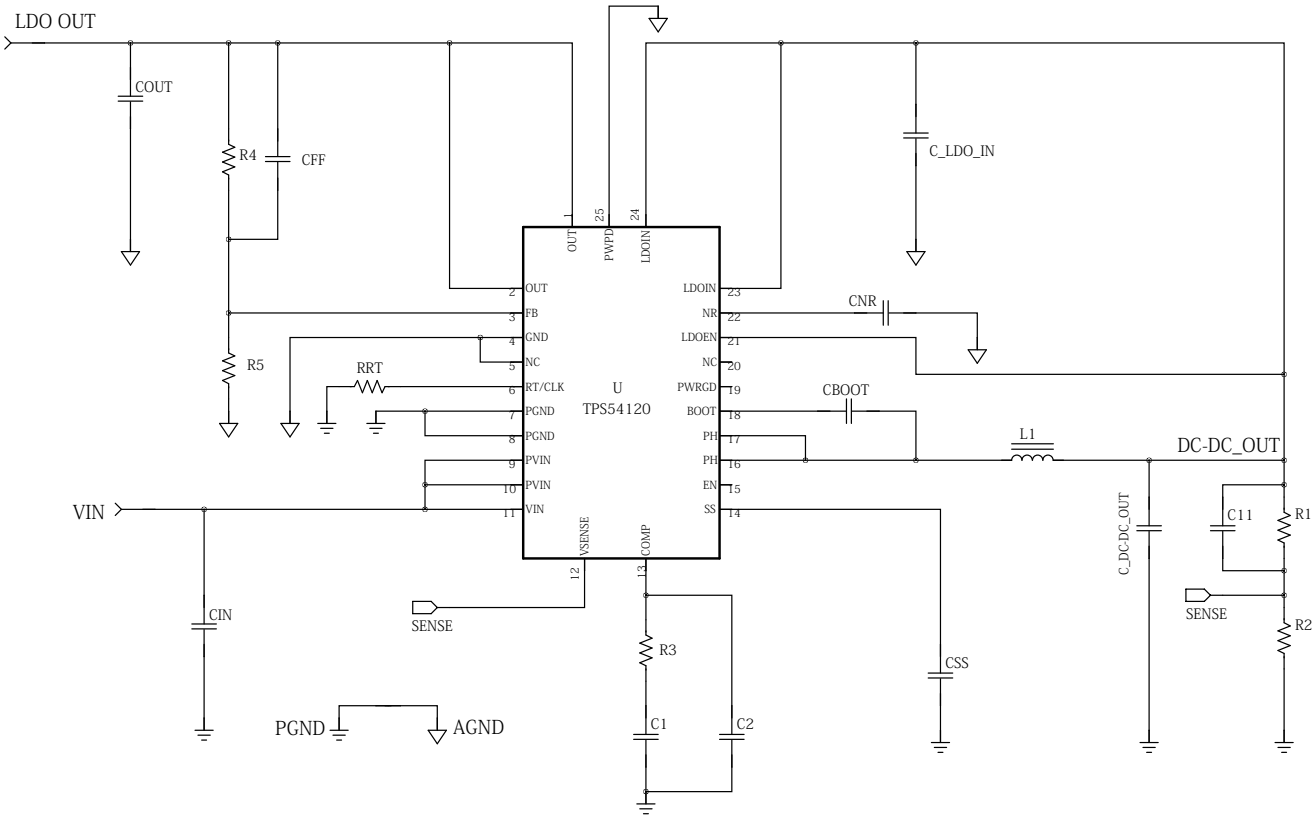


Figure 34. Application Circuit

Figure 34 shows a typical application diagram for the TPS54120. The first step in the design process is to select the switching frequency for the regulator. Higher switching frequencies may produce a smaller solution size using lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, higher switching frequencies causes additional switching losses that negatively impact converter efficiency and thermal performance.

After a switching frequency is determined, the inductor and output capacitor values of the switcher are selected. These two component values are related to each other and they depend on the input and output voltages of the switcher, as well as the current rating. Choosing a high inductor-ripple current also impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current.

The TPS54120 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of 4.7 µF on each input voltage rail. In some applications, additional bulk capacitance may also be required for the PVIN input. The voltage rating of the input capacitor must be greater than the maximum input voltage.

The internal LDO of the TPS54120 is designed to be stable with standard ceramic output capacitors with values of 4.7 µF or larger; higher values are recommended for better noise performance.

A 0.1-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10-V or higher voltage rating.

The output voltage of both the switcher and the LDO are adjustable using an external-resistor feedback network. Also, both the LDO and the switcher have a soft-start function that can be adjusted externally using the C_{SS} and C_{NR} capacitors, as shown in Figure 34.

There are several industry techniques used to compensate dc-dc regulators; refer to Application Report SLVA503 for more details about different compensation networks for the TPS54120.

SIMPLIFIED DESIGN METHODOLOGY

The TPS54120 has a low-noise output voltage range of 0.8 V to 6.0 V with an output current of up to 1 A. To simplify design efforts using the TPS54120, the typical designs for common applications are listed in Table 1. For designs using ceramic output capacitors, proper derating of ceramic output capacitance is recommended when doing the stability analysis because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. To execute a complete application design, refer to Application Report SLVA506, *Design Procedures for the TPS54120*.

Table 1. Simplified Design Table

VIN (V)	DC-DC_OUT (V)	VOUT (V)	I_{OUT} (max) (A)	f_{SW} (kHz)	L_1 (µH)	C_{DC-DC_OUT} (µF)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	R_4 (kΩ)	R_5 (kΩ)	R_{RT} (kΩ)	C_1 (µF)	C_2 (pF)	C_{OUT} (µF)	C_{11} (pF)	C_{FF} (µF)	RMS NOISE 100 Hz TO 100 kHz AT 100 mA (µVrms)	EFFICIENCY (%)
5	3	1.8	1.0	480	18	47	27.4	10	1.58	12.4	10	100	0.047	330	100	270	0.1	7.32	56.35
7	2.5	1.8	0.25	300	100	47	21.5	10	0.887	12.4	10	165	0.220	1000	100	499	0.1	7.83	67.35
8	2.5	1.8	1.0	480	15	47	21.5	10	1.33	12.4	10	100	0.047	330	100	330	0.1	7.22	66.25
12	3.7	3.0	1.0	480	20	47	36.5	10	1.96	27.4	10	100	0.047	330	100	200	0.1	8.27	75.42
12	4.1	3.3	0.5	480	43	47	41.2	10	2.2	30.9	10	100	0.100	330	100	180	0.1	8.3	73.38
12	4.1	3.3	1.0	480	22	47	41.2	10	2.2	30.9	10	100	0.047	330	100	180	0.1	7.52	74.67
12	5.5	5.0	1.0	480	27	47	59.0	10	2.94	52.3	10	100	0.047	330	100	120	0.1	10.61	80.95
12	6	5.0	0.5	1000	27	47	64.9	10	7.15	52.3	10	47.5	0.033	33	100	51	0.1	10.71	73.33
12	6	5.5	1.0	480	27	47	64.9	10	3.16	59.0	10	100	0.047	330	100	110	0.1	11.47	83.91
16	6	5.0	1.0	480	27	47	64.9	10	3.16	52.3	10	100	0.047	330	100	110	0.1	10.69	74.59
17	6	5.0	0.2	480	130	47	64.9	10	3.16	52.3	10	100	0.220	330	100	110	0.1	10.81	76.84

PCB LAYOUT GUIDELINES

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS54120 are available at the end of this product datasheet and at www.ti.com.

BOARD LAYOUT RECOMMENDATIONS FOR HIGH-PSR AND LOW-NOISE PERFORMANCE

Correct printed circuit board (PCB) layout is a critical portion of good power-supply design and is a particularly important for the high PSR and low-noise performance of the TPS54120. The following general guidelines are provided; for a more detailed description, refer to the TPS54120EVM User Guide, SLVU641.

- The inductor, the boot capacitor, and the output cap of the dc-dc converter should be placed on layers of the board that help minimize the spread of the switching noise into the LDO area on the board, such as the bottom layer.
- The boot cap and inductor L1 should be connected as close as possible to the PH pin to reduce parasitic inductance of long traces.
- To help shield the compensation components, the soft-start capacitors, CLK/RT resistor, and dc-dc feedback resistors from noise, these components should be grounded to a power ground that is shielded from the high-current ground plane. This shielding can be achieved by using a separate trace to the PGND pin.
- The RT/CLK pin is sensitive to noise, so the RT resistor should be located as close as possible to the device and routed with a short connection.
- The noise-reduction capacitor should be placed as close as possible to the device to avoid noise pickup into the LDO reference.
- The ground planes on the input and the output should be isolated from each other and connected through a separate trace route that parallels the power-loop routing from the dc-dc output to the LDO input.
- The low-noise analog ground of the LDO circuits (such as the voltage set point divider, the LDO input, and output caps) should be terminated to ground using a wide ground trace separate from the power ground plane.
- The LDO input capacitor and output capacitor should be as close to the device as possible.
- The VIN and PVIN pins must be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric and placed as close as possible to the VIN, PVIN, and PGND pins.
- For operation at full-rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipation.
- PCB conductor planes should be minimized to prevent excessive capacitive coupling.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2012) to Revision C **Page**

- Added capacitor to Figure 28 12
- Changed Equation 3 13
- Added two new columns to Table 1 22

Changes from Revision A (January 2012) to Revision B **Page**

- Deleted device name from Figure 30, Figure 31, and Figure 32 (typo) 18

Changes from Original (January 2012) to Revision A **Page**

- Changed from product preview to production data 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS54120RGYR	ACTIVE	VQFN	RGY	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS54120	Samples
TPS54120RGYT	ACTIVE	VQFN	RGY	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS54120	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

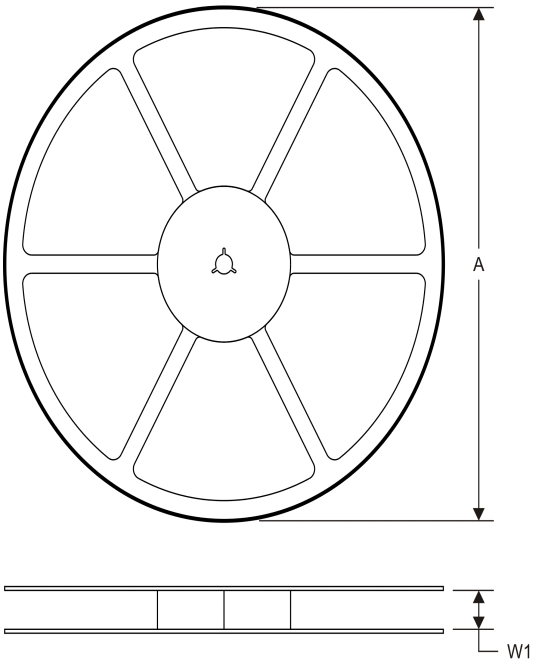
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

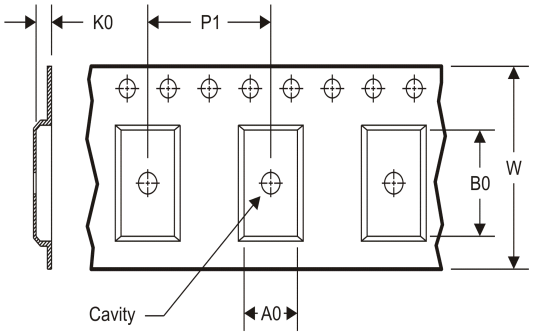
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

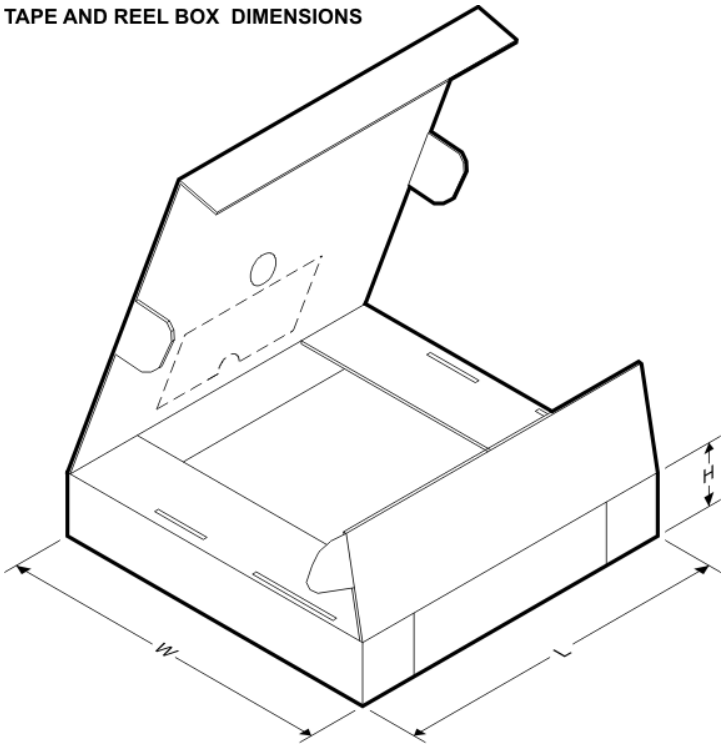
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54120RGYR	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
TPS54120RGYT	VQFN	RGY	24	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

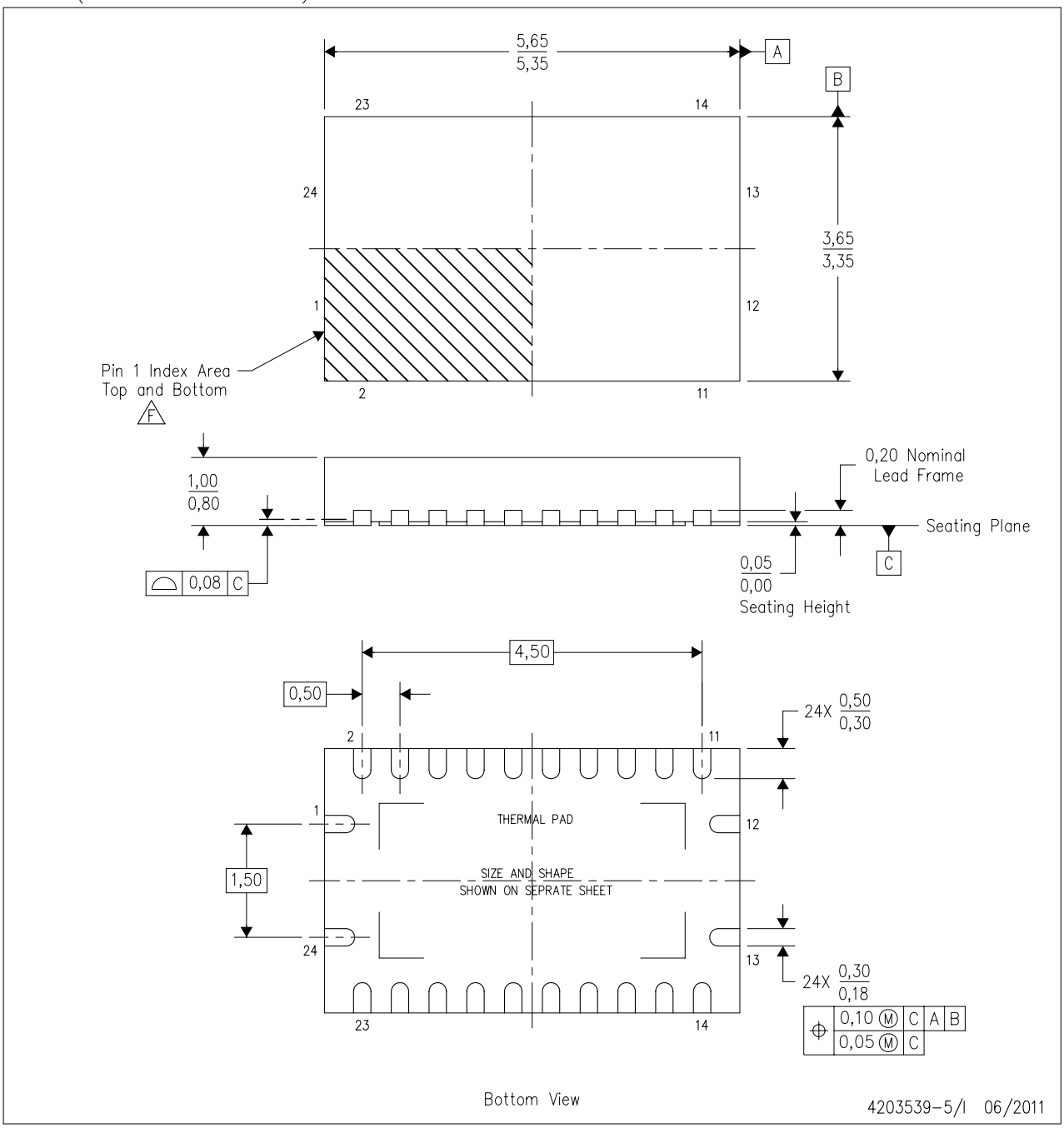


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54120RGYR	VQFN	RGY	24	3000	367.0	367.0	35.0
TPS54120RGYT	VQFN	RGY	24	250	210.0	185.0	35.0

MECHANICAL DATA

RGY (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

THERMAL PAD MECHANICAL DATA

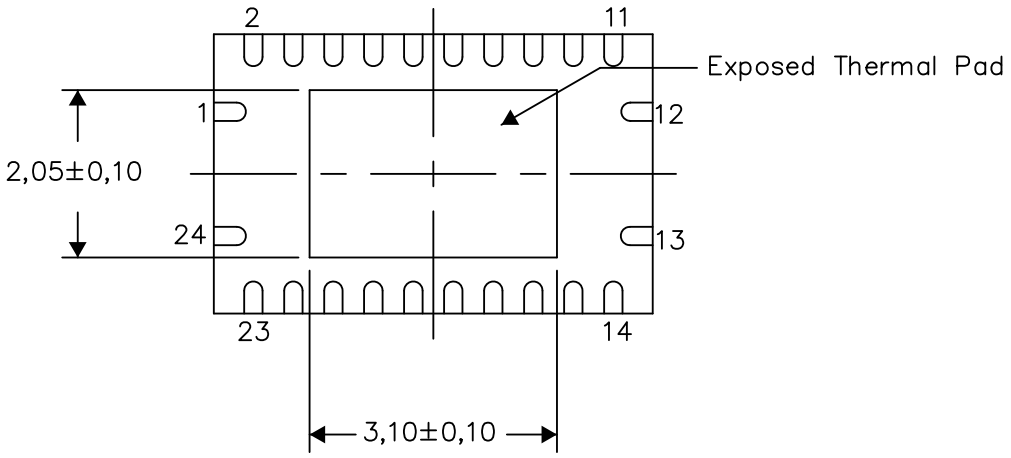
RGY (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

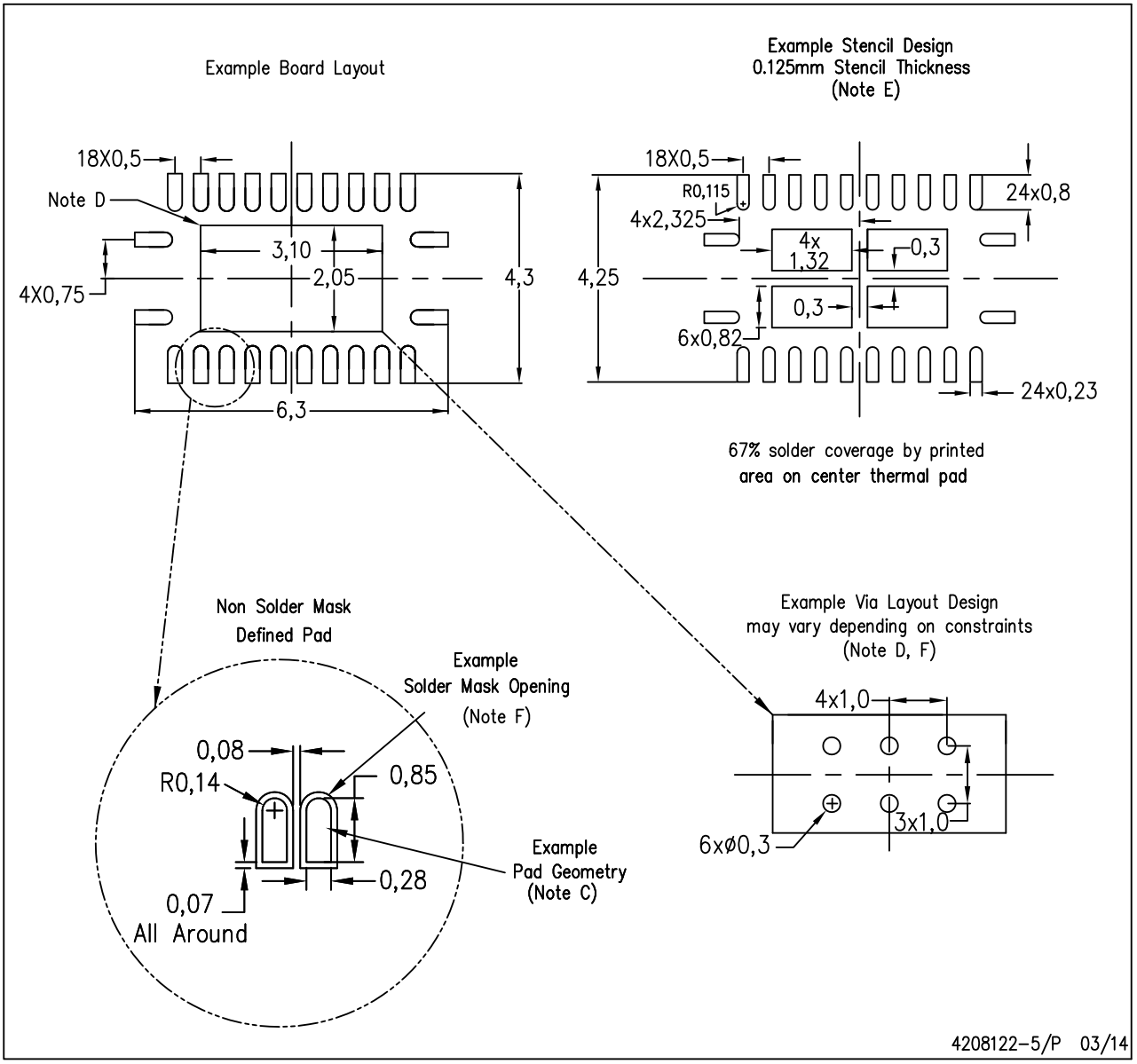
Exposed Thermal Pad Dimensions

4206353–6/P 03/14

NOTE: All linear dimensions are in millimeters

LAND PATTERN DATA

RGY (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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