

# **Excellent Integrated System Limited**

Stocking Distributor

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<u>Vishay Semiconductor/Diodes Division</u> <u>VBUS05L1-DD1-G-08</u>

For any questions, you can email us directly: <a href="mailto:sales@integrated-circuit.com">sales@integrated-circuit.com</a>

### Distributor of Vishay Semiconductor/Diodes Division: Excellent Integrated System Limite

Datasheet of VBUS05L1-DD1-G-08 - TVS DIODE 5.5VWM 17VC LLP1006

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### VBUS05L1-DD1

RoHS

COMPLIANT

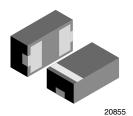
**HALOGEN** FREE

GREEN

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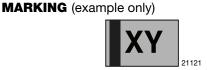
# Bidirectional Symmetrical (BiSy) Low Capacitance, Single-Line ESD-Protection Diode in LLP1006-2M





- Ultra compact LLP1006-2M package
- Low package height < 0.4 mm
- 1-line ESD-protection
- Working range ± 5.5 V
- Low leakage current I<sub>R</sub> < 0.1 μA</li>
- Very low load capacitance C<sub>D</sub> = 0.3 pF
- ESD-protection acc. IEC 61000-4-2 ± 15 kV contact discharge
  - ± 16 kV air discharge
- Soldering can be checked by standard vision inspection; no X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- e4 precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





Bar = pin 1 marking

X = date code

Y = type code (see table below)

ORDERING INFORMATION				
DEVICE NAME ORDERING CODE		TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY	
VBUS05L1-DD1	VBUS05L1-DD1-G-08	8000	8000	

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS05L1-DD1	LLP1006-2M	R	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS VBUS05L1-DD1						
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT		
Peak pulse current	Acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot	I <sub>PPM</sub>	2	Α		
Peak pulse power	Pin 1 to pin 2, acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot	$P_{PP}$	34	W		
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	M	± 15	kV		
	Air discharge acc. IEC 61000-4-2; 10 pulses	$V_{ESD}$	± 16	kV		
Operating temperature	Junction temperature	TJ	-40 to +125	°C		
Storage temperature		T <sub>STG</sub>	-40 to +150	°C		

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and International patents.

Rev. 1.5, 08-Jun-16 Document Number: 81188

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Datasheet of VBUS05L1-DD1-G-08 - TVS DIODE 5.5VWM 17VC LLP1006

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### VBUS05L1-DD1

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<b>ELECTRICAL CHARACTERISTICS VBUS05L1-DD1</b> (T <sub>amb</sub> = 25 °C, unless otherwise specified)						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	N <sub>channel</sub>	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	5.5	V
Reverse voltage	at I <sub>R</sub> = 0.05 μA	$V_R$	5.5	-	-	V
Reverse current	at V <sub>RWM</sub> = 5.5 V	I <sub>R</sub>	-	-	0.05	μA
Reverse breakdown voltage	at I <sub>R</sub> = 1 mA	$V_{BR}$	7	8.4	9.5	V
Reverse clamping voltage	at I <sub>PP</sub> 1 A	V <sub>C</sub>	-	11.5	14	V
	at I <sub>PP</sub> = I <sub>PPM</sub> = 2 A	V <sub>C</sub>	-	14	17	V
Capacitance	at V <sub>R</sub> = 0 V, f = 1 MHz	C <sub>D</sub>	-	0.33	0.4	pF
	at V <sub>R</sub> = 2.5 V, f = 1 MHz	C <sub>D</sub>	-	0.34	-	pF

#### **VBUS05L1-DD1: ESD PROTECTION WITH LOWEST LOAD CAPACITANCE**

The VBUS05L1-DD1 is a bidirectional and symmetrical (BiSy) ESD-protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VBUS05L1-DD1 offers a high isolation (low leakage current, lowest capacitance) within the specified working range. Due to the short leads and small package size of the tiny LLP1006-2M package the line inductance is very low, so that fast transients like an ESD-strike can be clamped with minimal over- or undershoots.

### TYPICAL CHARACTERISTICS (T<sub>amb</sub> = 25 °C, unless otherwise specified)

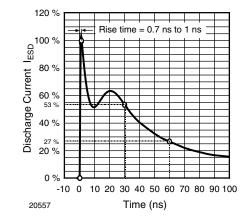


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

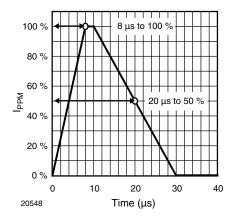
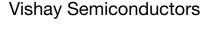


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

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# VBUS05L1-DD1

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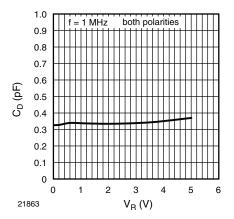


Fig. 3 - Typical Capacitance  $C_D$  vs. Reverse Voltage  $V_R$ 

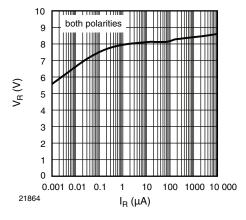


Fig. 4 - Typical Reverse Voltage  $V_{\text{R}}$  vs. Reverse Current  $I_{\text{R}}$ 

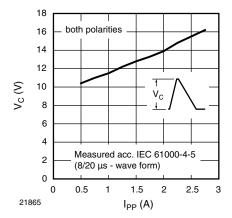


Fig. 5 - Typical Peak Clamping Voltage V<sub>C</sub> vs. Peak Pulse Current IPP

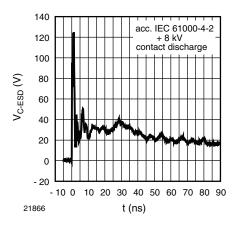


Fig. 6 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

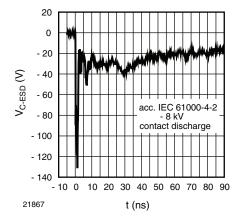


Fig. 7 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

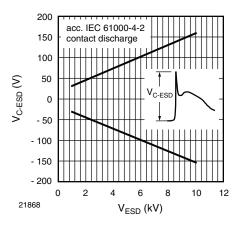


Fig. 8 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

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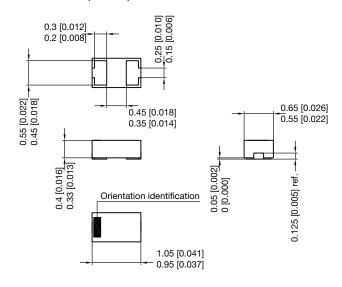
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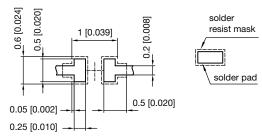
### VBUS05L1-DD1

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#### PACKAGE DIMENSIONS in millimeters (inches): LLP1006-2M

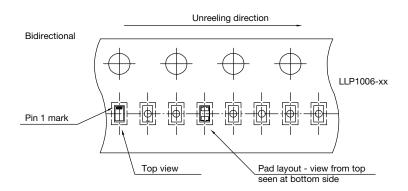


Foot print recommendation:



Pad Design Patented: (P)US 9.018.537 B2)

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