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AOD4136

N-Channel SDMOS™ POWER Transistor

General Description

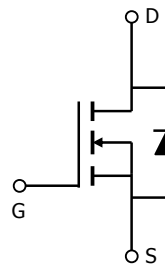
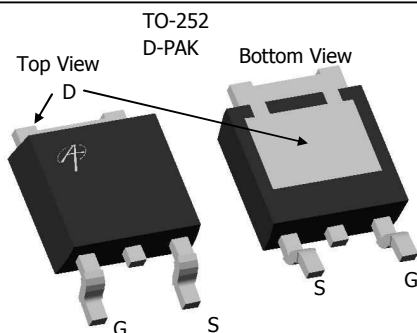
The AOD4136 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for both DC-DC and load switch applications.

- RoHS Compliant
- Halogen Free*

Features

V_{DS} (V) = 25V
 I_D = 25A (V_{GS} = 10V)
 $R_{DS(ON)} < 11m\Omega$ (V_{GS} = 10V)
 $R_{DS(ON)} < 19m\Omega$ (V_{GS} = 4.5V)

100% UIS Tested!
100% Rg Tested!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{B,H}	I_D	$T_C=25^\circ\text{C}$	25
		$T_C=100^\circ\text{C}$	20
Pulsed Drain Current ^C	I_{DM}	100	A
Avalanche Current ^C	I_{AR}	17	
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	15	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	30
		$T_C=100^\circ\text{C}$	15
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	2.1
		$T_A=70^\circ\text{C}$	1.3
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{A,G}	$R_{\theta JA}$	17.4	25	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient ^{A,G}	$R_{\theta JC}$	4	5	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case ^F				

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	25			V
I _D DSS	Zero Gate Voltage Drain Current	V _{DS} =25V, V _{GS} =0V T _J =55°C			10 100	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.5	1.9	2.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	100			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		9 13	11 16	mΩ
		V _{GS} =4.5V, I _D =15A		15	19	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		32		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.71	1	V
I _S	Maximum Body-Diode Continuous Current				20	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =12.5V, f=1MHz		734		pF
C _{oss}	Output Capacitance			174		pF
C _{rss}	Reverse Transfer Capacitance			97		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	2.4	3.6	5.4	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =12.5V, I _D =20A		12.9	16.8	nC
Q _g (4.5V)	Total Gate Charge			6.2	8.1	nC
Q _{gs}	Gate Source Charge			2.2		nC
Q _{gd}	Gate Drain Charge			4		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =12.5V, R _L =0.5Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			11.2		ns
t _{D(off)}	Turn-Off DelayTime			19.6		ns
t _f	Turn-Off Fall Time			9.6		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=300A/μs		12	16	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=300A/μs		11		nC

A: The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C. The power dissipation P_D and current rating I_D are based on T_{J(MAX)}=150°C, using t ≤ 10s junction-to-ambient thermal resistance.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

G: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

H: The maximum current rating is limited by bond-wires.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev1: Oct 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

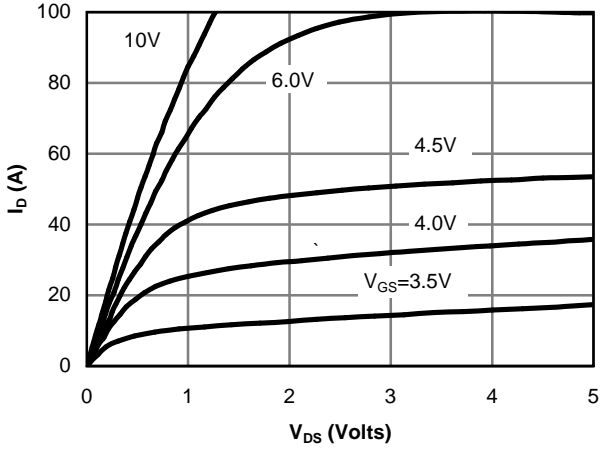


Figure 1: On-Region Characteristics

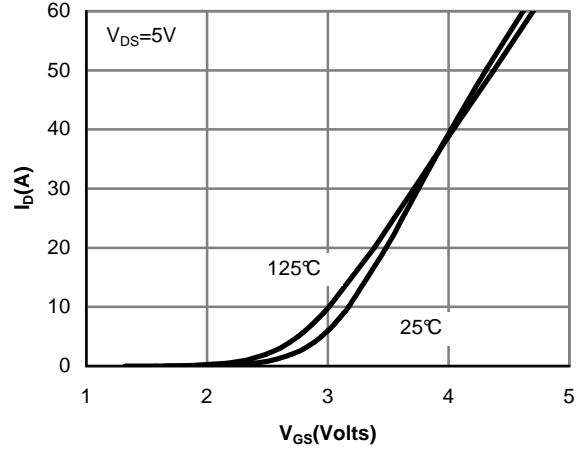


Figure 2: Transfer Characteristics

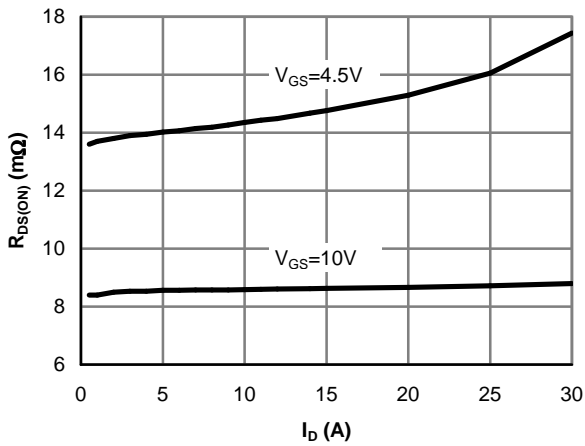


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

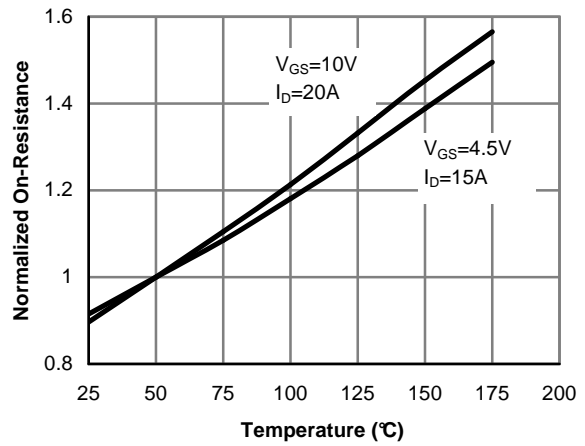


Figure 4: On-Resistance vs. Junction Temperature

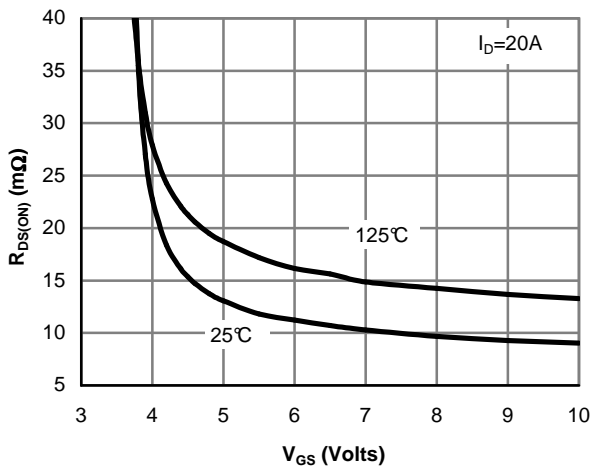


Figure 5: On-Resistance vs. Gate-Source Voltage

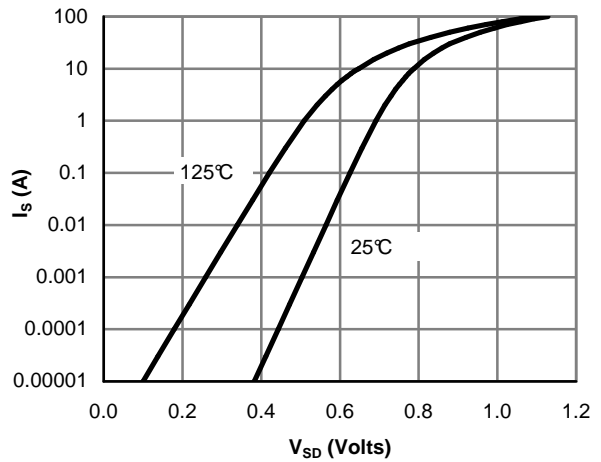


Figure 6: Body-Diode Characteristics

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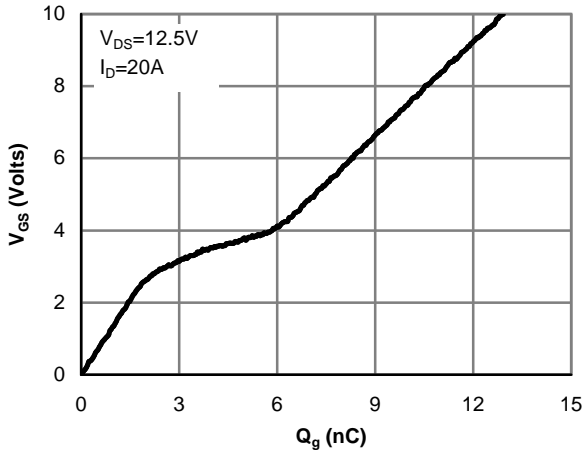


Figure 7: Gate-Charge Characteristics

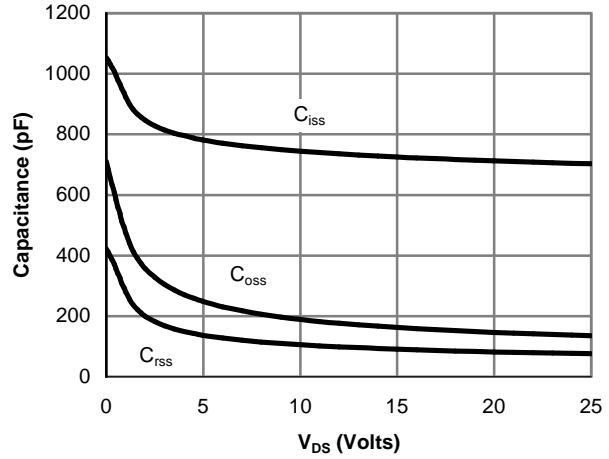


Figure 8: Capacitance Characteristics

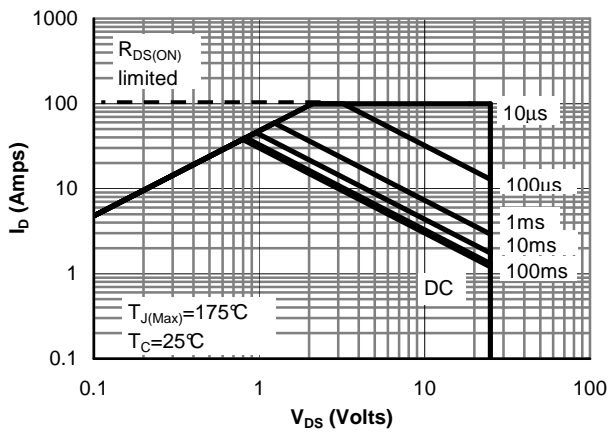


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

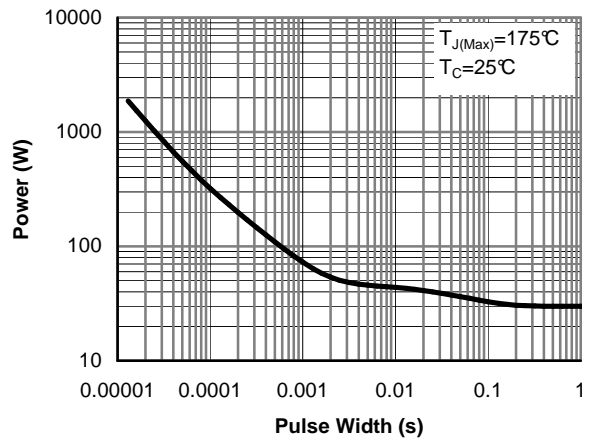


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

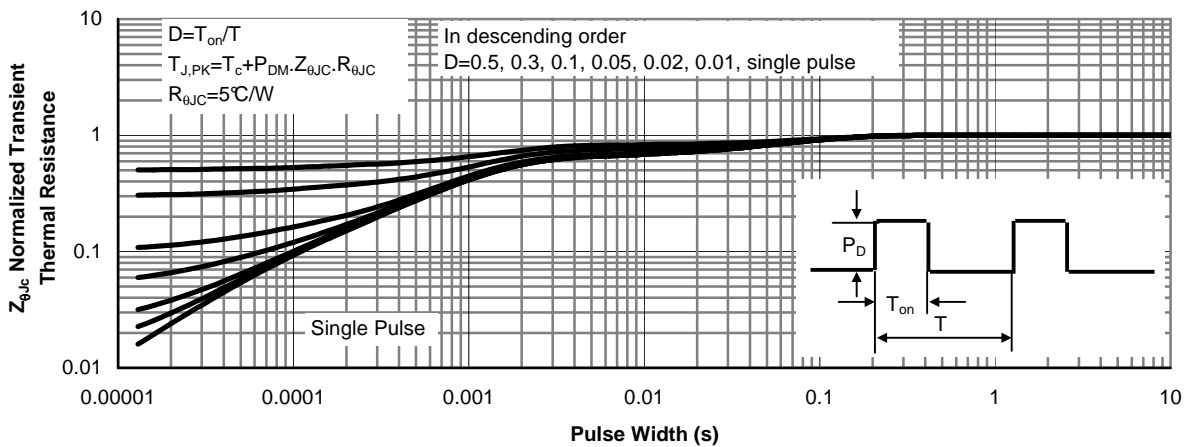


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

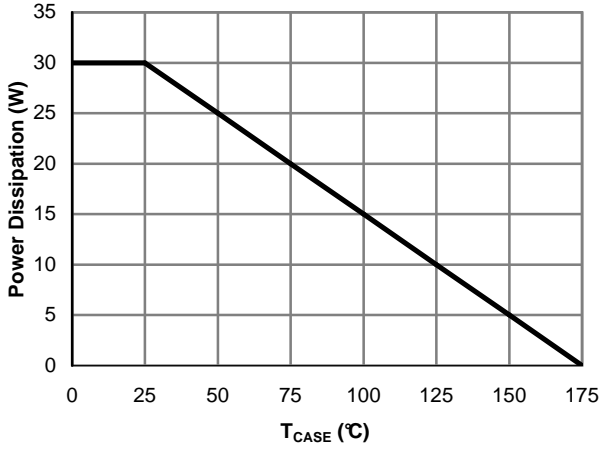


Figure 12: Power De-rating (Note B)

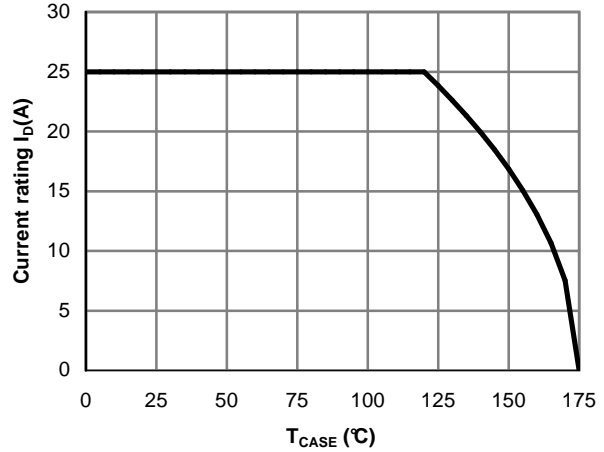


Figure 13: Current De-rating (Note B)

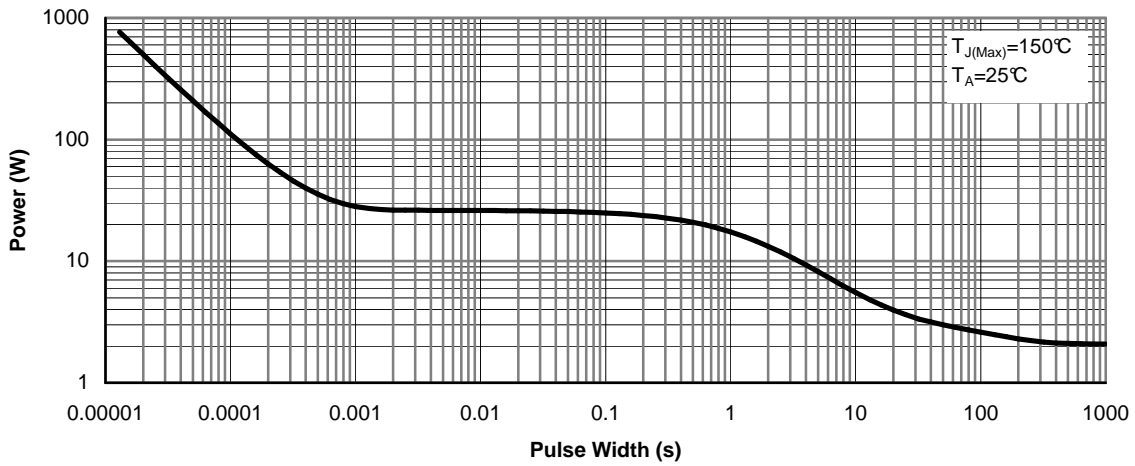


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

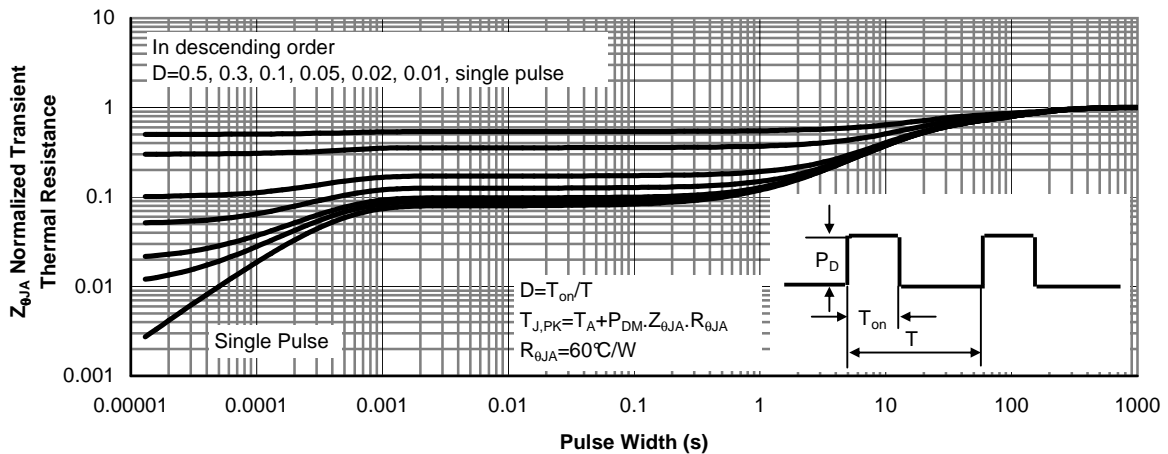
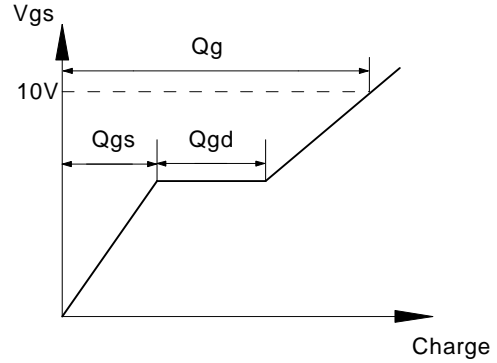
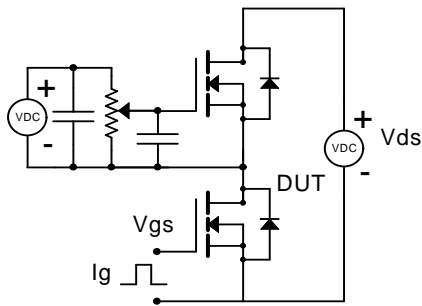


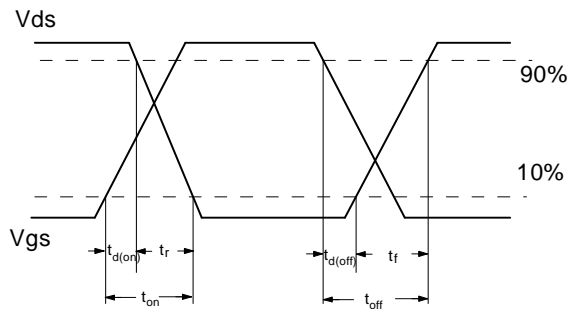
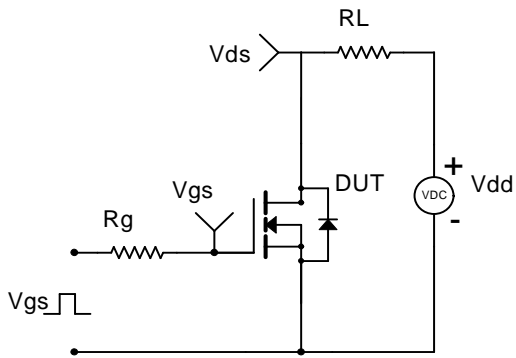
Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

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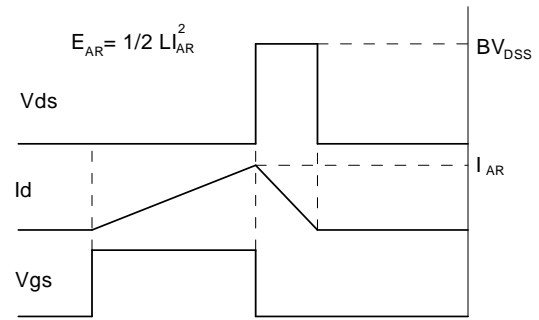
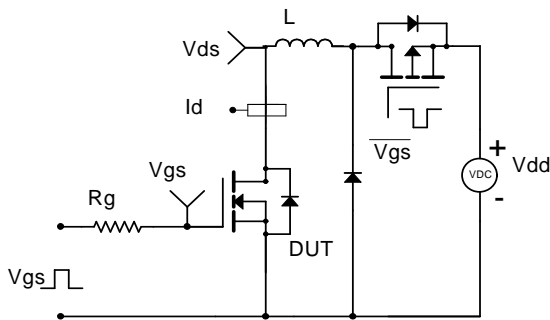
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

