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AOT482L/AOB482L

80V N-Channel MOSFET

SDMOS™

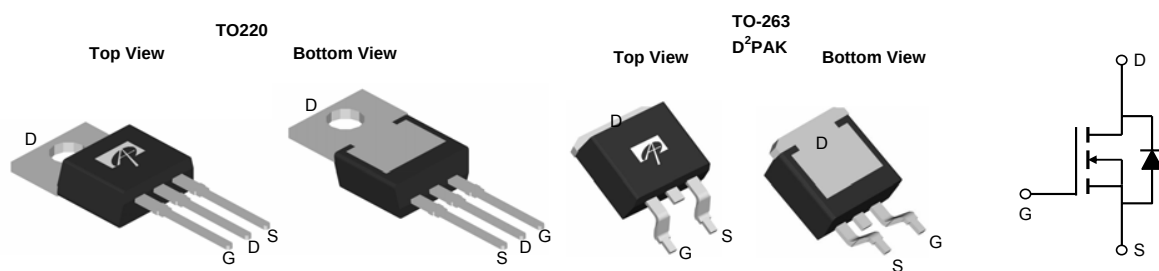
General Description

The AOT482L/AOB482L is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge and low Q_{rr} . The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

Product Summary

V_{DS}	80V
I_D (at $V_{GS}=10V$)	105A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 7.2mΩ
$R_{DS(ON)}$ (at $V_{GS} = 7V$)	< 9mΩ

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	±25	V
Continuous Drain Current ^G	I_D	105	A
$T_C=25^\circ\text{C}$		82	
$T_C=100^\circ\text{C}$			
Pulsed Drain Current ^C	I_{DM}	330	
Continuous Drain Current	I_{DSM}	11	A
$T_A=25^\circ\text{C}$		9	
$T_A=70^\circ\text{C}$			
Avalanche Current ^C	I_{AS}, I_{AR}	82	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	336	mJ
Power Dissipation ^B	P_D	333	W
$T_C=25^\circ\text{C}$		167	
$T_C=100^\circ\text{C}$			
Power Dissipation ^A	P_{DSM}	2.1	W
$T_A=25^\circ\text{C}$		1.3	
$T_A=70^\circ\text{C}$			
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	11	15	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient ^{A D}		47	60	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case	$R_{\theta JC}$	0.36	0.45	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	80			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			10 50	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 25\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.5	3.1	3.7	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	330			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$ TO220 $T_J=125^{\circ}\text{C}$		5.9 11	7.2 13	$\text{m}\Omega$
		$V_{GS}=7\text{V}$, $I_D=20\text{A}$ TO220		6.8	9	$\text{m}\Omega$
		$V_{GS}=10\text{V}$, $I_D=20\text{A}$ TO263		5.6	6.9	$\text{m}\Omega$
		$V_{GS}=7\text{V}$, $I_D=20\text{A}$ TO263		6.5	8.7	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		50		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.64	1	V
I_S	Maximum Body-Diode Continuous Current ^E				105	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=40\text{V}$, $f=1\text{MHz}$	3240	4054	4870	pF
C_{oss}	Output Capacitance		320	458	600	pF
C_{rss}	Reverse Transfer Capacitance		95	160	225	pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	0.2	0.45	0.7	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=40\text{V}$, $I_D=20\text{A}$	53	66.8	81	nC
Q_{gs}	Gate Source Charge		16	20.8	25	nC
Q_{gd}	Gate Drain Charge		12	20.2	30	nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=40\text{V}$, $R_L=2\Omega$, $R_{GEN}=3\Omega$		26		ns
t_r	Turn-On Rise Time			18		ns
$t_{D(off)}$	Turn-Off DelayTime			48		ns
t_f	Turn-Off Fall Time			21		ns
t_{rr}	Body Diode Reverse Recovery Time		18	26	34	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$	75	108	140	nC

- A. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
- B. The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
- D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^{\circ}\text{C}$. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

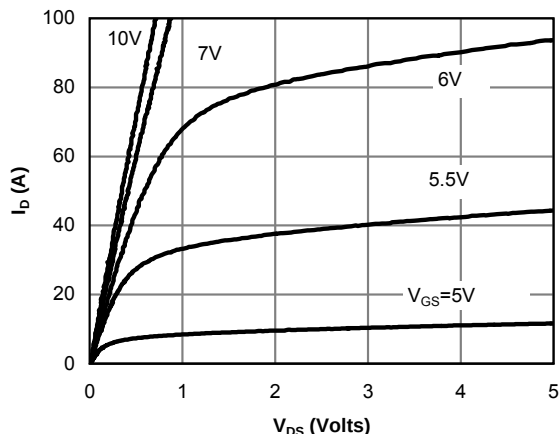


Fig 1: On-Region Characteristics (Note E)

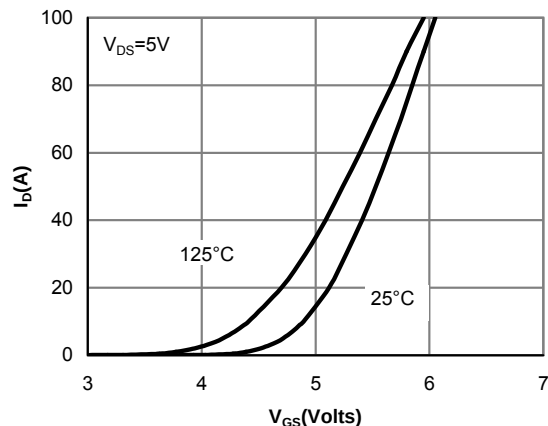


Figure 2: Transfer Characteristics (Note E)

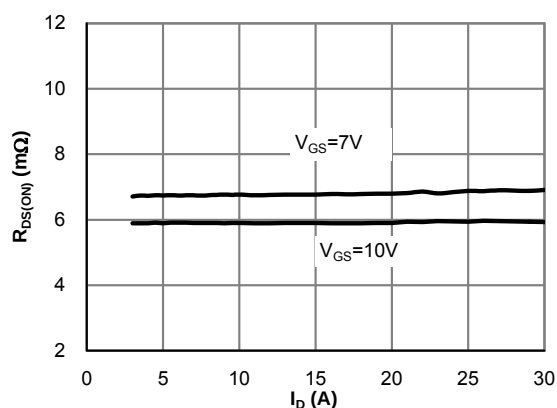


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

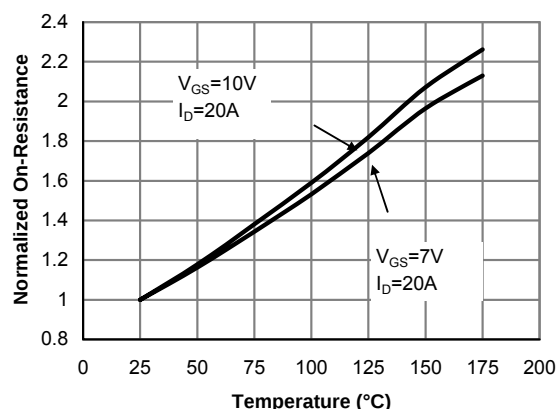


Figure 4: On-Resistance vs. Junction Temperature (Note E)

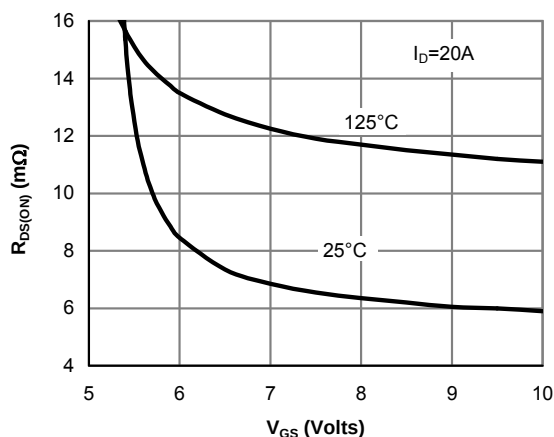


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

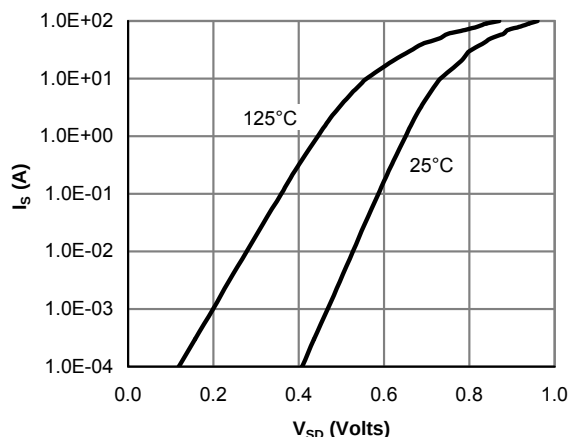


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

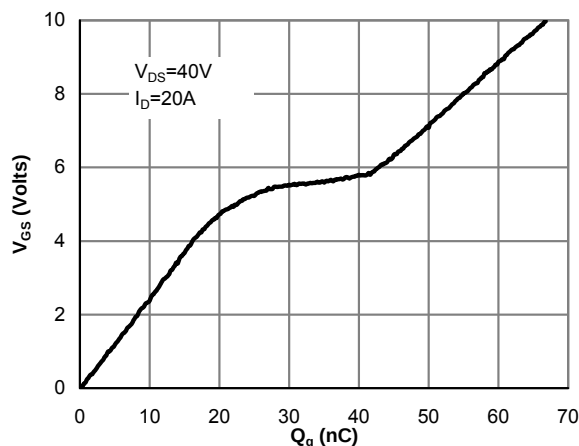


Figure 7: Gate-Charge Characteristics

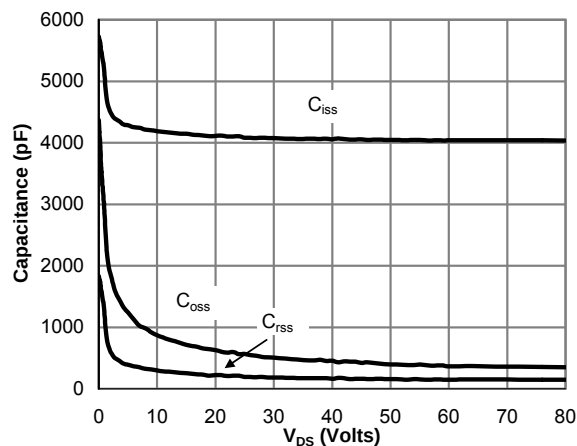


Figure 8: Capacitance Characteristics

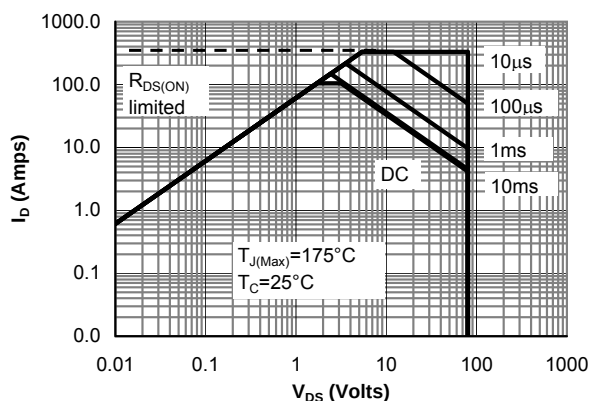


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

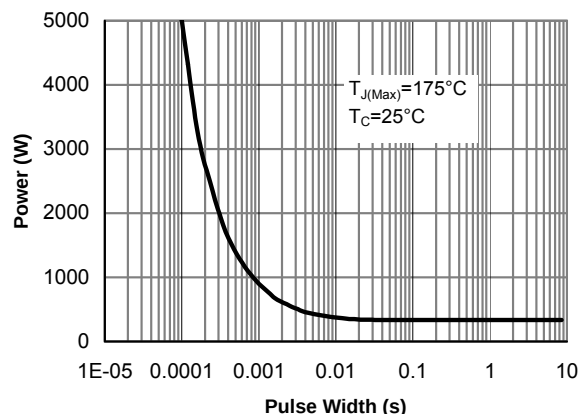


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

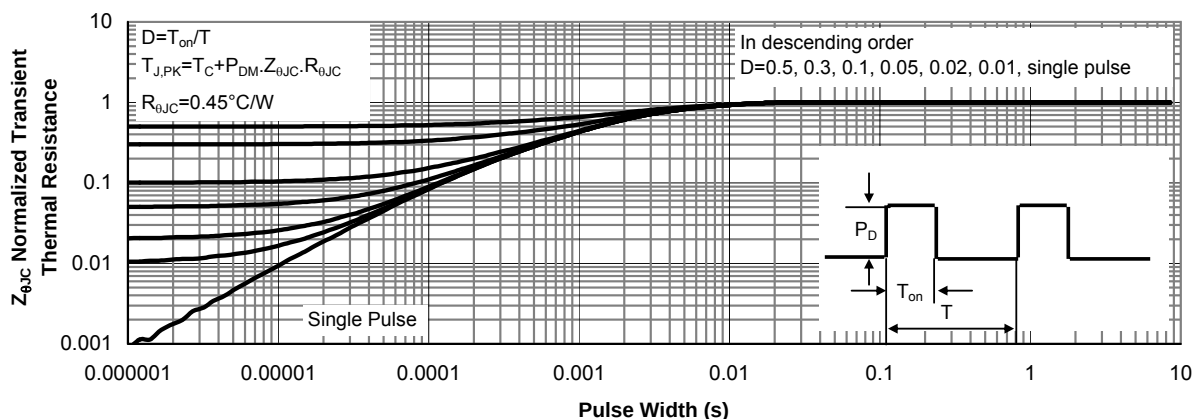


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

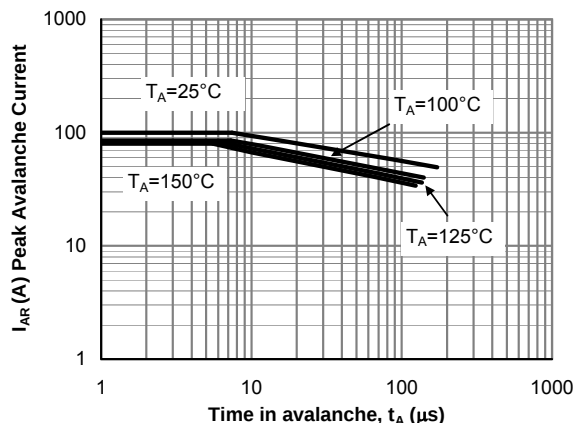


Figure 12: Single Pulse Avalanche capability (Note C)

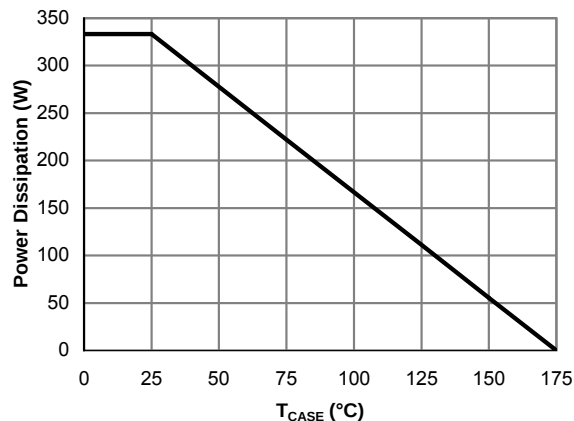


Figure 13: Power De-rating (Note F)

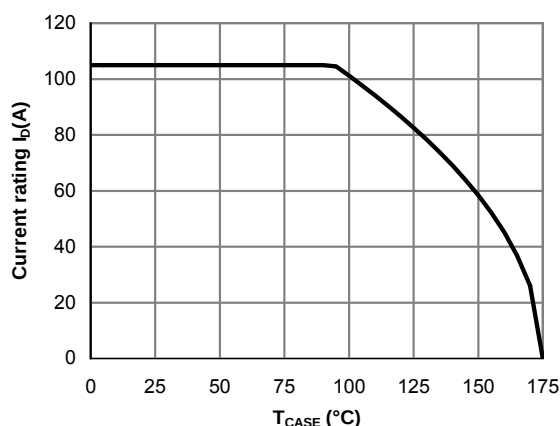


Figure 14: Current De-rating (Note F)

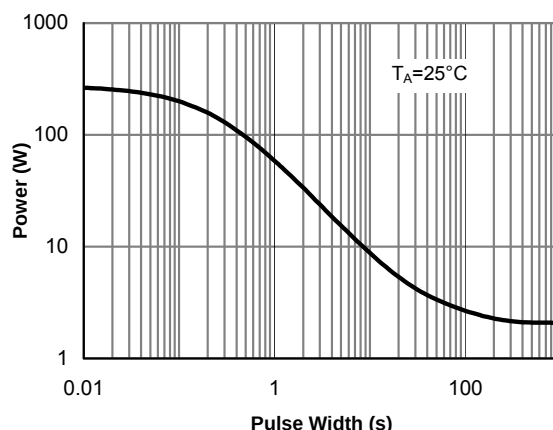


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

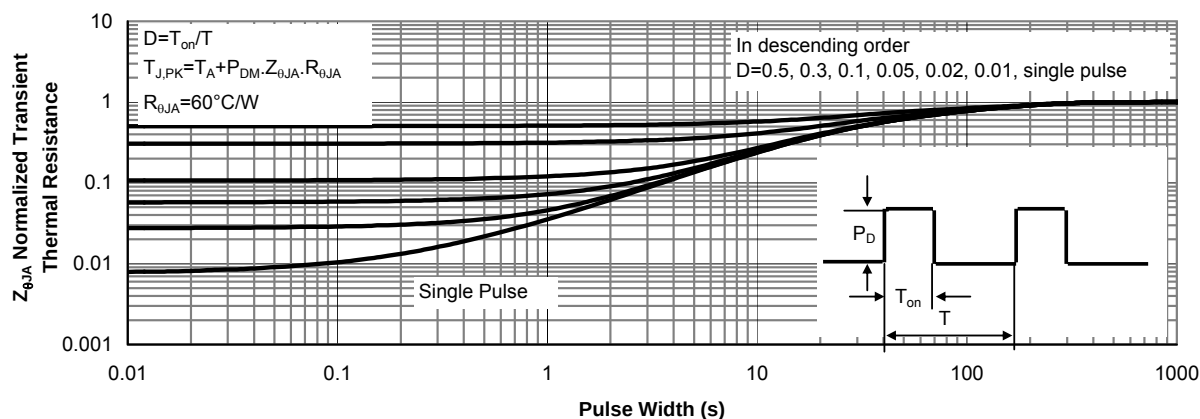


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

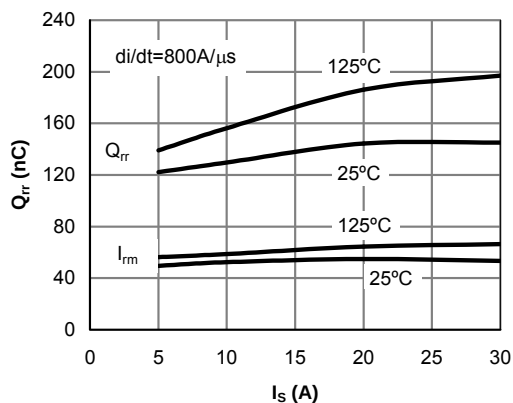


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

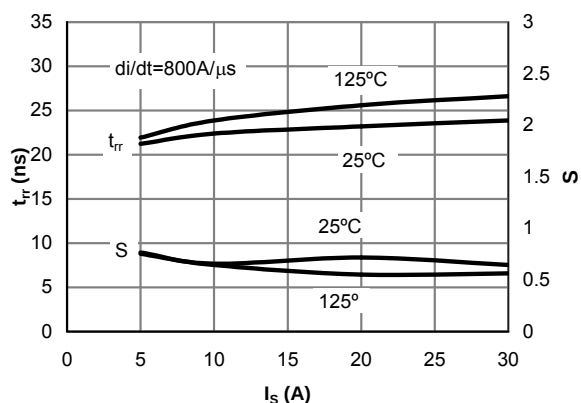


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

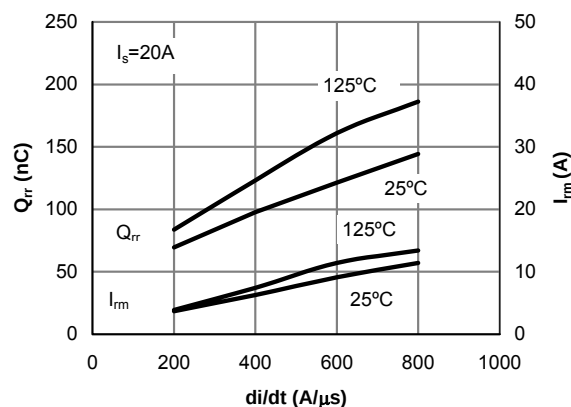


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

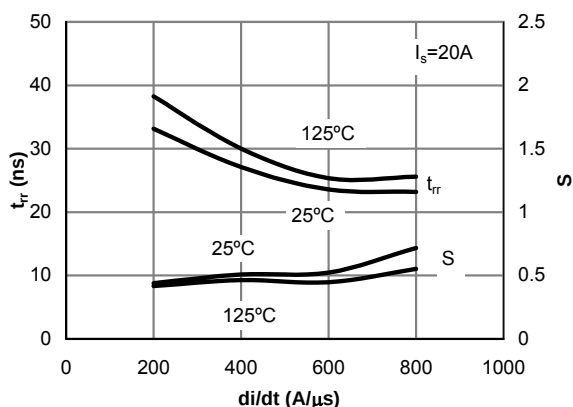
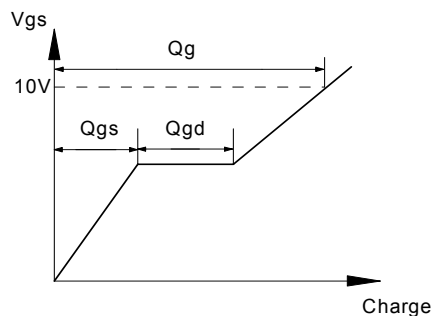
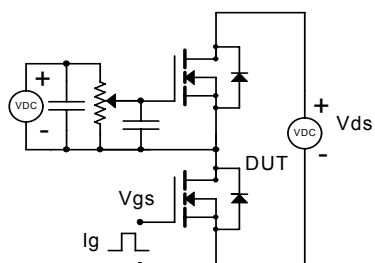
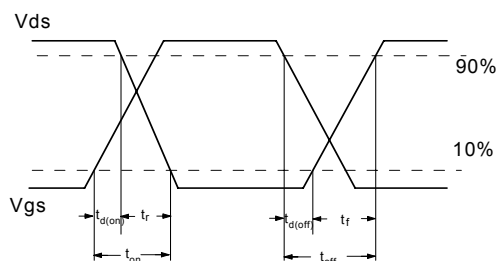
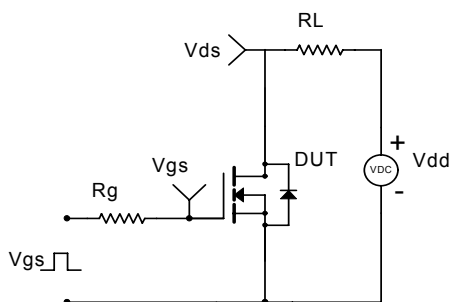


Figure 20: Diode Reverse Recovery Time and Softness Factor vs. di/dt

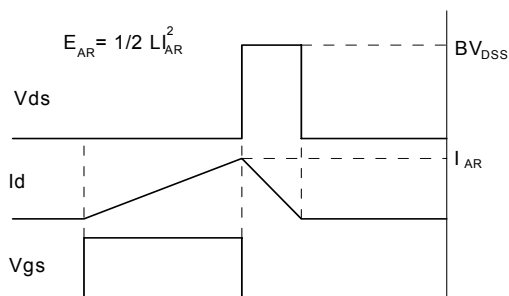
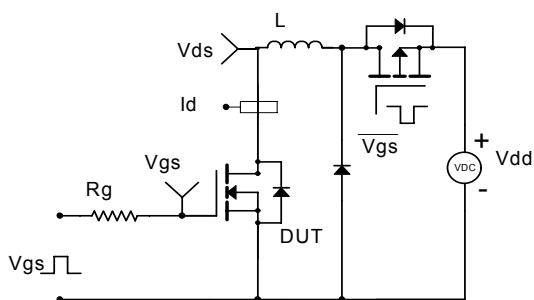
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

