# **Excellent Integrated System Limited**

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<u>Fairchild Semiconductor</u> <u>MM74C154N</u>

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October 1987 Revised January 2004

### MM74C154

### 4-Line to 16-Line Decoder/Demultiplexer

### **General Description**

The MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

#### **Features**

■ Supply voltage range: 3V to 15V

■ Tenth power TTL compatible: Drive 2 LPTTL loads

■ High noise margin: 1V guaranteed■ High noise immunity: 0.45 V<sub>CC</sub> (typ.)

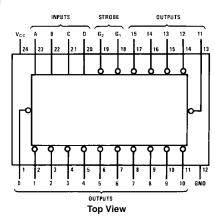
#### **Applications**

- Automotive
- · Data terminals
- · Instrumentation
- Medical electronics
- · Alarm systems
- · Industrial electronics
- · Remote metering
- Computers

### **Ordering Code:**

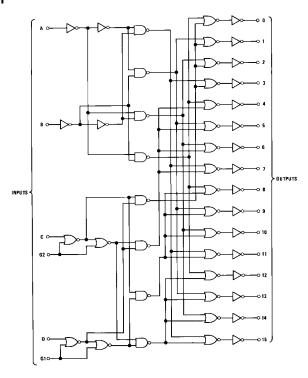
Order Number	Package Number	Package Description
MM74C154N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600" Wide

### **Connection Diagram**



MM74C154

# Logic Diagram



### **Truth Table**

Inputs							Outputs														
G1	G2	D	С	В	Α	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н
L	L	Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	L	Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
L	L	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	Х	Χ	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	Х	Χ	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	Н	Х	Х	Χ	Х	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
X = "Dor	't Care"	Condi	tion																		

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### **Absolute Maximum Ratings**(Note 1)

Voltage at Any Pin -0.3V to  $V_{CC} + 0.3V$ Operating Temperature Range -55°C to +125°C Storage Temperature Range  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 18V  ${\it Maximum} \ {\it V}_{\it CC} \ {\it Voltage}$ Power Dissipation

Dual-In-Line 700 mW Small Outline 500 mW

Operating  $V_{\rm CC}$  Range 3V to 15V

Lead Temperature

(Soldering, 10 seconds) 260°C Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

### **DC Electrical Characteristics**

Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units		
CMOS TO	CMOS	•		U	l .			
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 5.0V	3.5			V		
		V <sub>CC</sub> = 10V	8.0			v		
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 5.0V			1.5 V			
		V <sub>CC</sub> = 10V			2.0	v		
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	$V_{CC} = 5.0V, I_{O} = -10\mu A$			V			
		$V_{CC} = 10V, I_{O} = -10 \mu A$	9.0			v		
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	$V_{CC} = 5.0V, I_{O} = 10\mu A$			0.5	V		
		$V_{CC} = 10V$ , $I_{O} = 10 \mu A$			1.0	v		
I <sub>IN(1)</sub>	Logical "1" Input Current	V <sub>CC</sub> = 15V, V <sub>IN</sub> = 15V		0.005	1.0	μΑ		
I <sub>IN(0)</sub>	Logical "0" Input Current	V <sub>CC</sub> = 15V, V <sub>IN</sub> = 0V	-1.0	-0.005		μΑ		
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = 15V		0.05	300	μΑ		
CMOS TO	LPTTL INTERFACE	·			•			
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 4.75V	V <sub>CC</sub> - 1.5			V		
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 4.75V			0.8	V		
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_{O} = -100 \mu A$	2.4			V		
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V		
	RIVE (See Family Characteristics	Data Sheet) (Short Circuit Current)			•			
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 5.0V, V_{IN(0)} = 0V$	-1.75			mA		
		$T_A = 25$ °C, $V_{OUT} = 0V$						
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$	-8.0			mA		
		$T_A = 25^{\circ}C$ , $V_{OUT} = 0V$						
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 5.0V, V_{IN(1)} = 5.0V$	1.75			mA		
		$T_A = 25^{\circ}C$ , $V_{OUT} = V_{CC}$						
I <sub>SINK</sub>	Output Sink Current	V <sub>CC</sub> = 10V, V <sub>IN(1)</sub> = 10V	8.0			mA		
		$T_A = 25$ °C, $V_{OUT} = V_{CC}$						

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MM74C154

### AC Electrical Characteristics (Note 2)

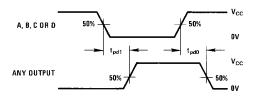
Symbol	Parameter	Conditions	Min	Тур	Max	Units			
t <sub>pd0</sub>	Propagation Delay to a Logical	V <sub>CC</sub> = 5.0V		275	400	ns			
	"0" from Any Input to Any Output	V <sub>CC</sub> = 10V		100	200	IIS			
t <sub>pd0</sub>	Propagation Delay to a Logical	V <sub>CC</sub> = 5.0V		275	400	no			
	"0" from G1 or G2 to Any Output	V <sub>CC</sub> = 10V		100	200	ns			
t <sub>pd0</sub>	Propagation Delay to a Logical	V <sub>CC</sub> = 5.0V		265	400	ns			
	"0" from Any Input to Any Output	V <sub>CC</sub> = 10V		100	200	115			
t <sub>pd1</sub>	Propagation Delay to a Logical	V <sub>CC</sub> = 5.0V		265	400	ns			
	"1" from G1 or G2 to Any Output	V <sub>CC</sub> = 10V		100	200	115			
C <sub>IN</sub>	Input Capacitance	(Note 3)		5.0		pF			
C <sub>PD</sub>	Power Dissipation Capacitance	(Note 4)		60		pF			

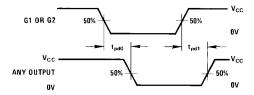
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C<sub>PD</sub> determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note

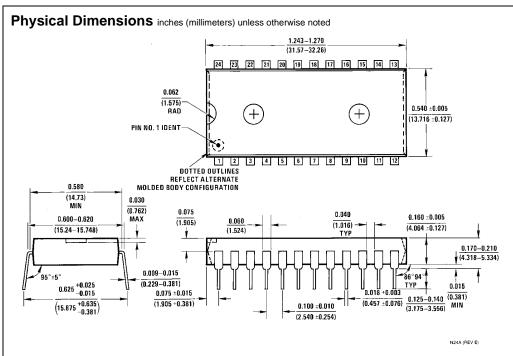
### **Switching Time Waveforms**





 $t_{\text{r}}=t_{\text{f}}=20~\text{ns}$ 





24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600" Wide Package Number N24A

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