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<u>Fairchild Semiconductor</u> <u>MM74C74N</u>

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FAIRCHILD SEMICONDUCTOR TM October 1987 Revised May 2002

MM74C74 **Dual D-Type Flip-Flop**

General Description

The MM74C74 dual D-type flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip-flop has independent data, preset, clear and clock inputs and Q and \overline{Q} outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear

Features

■ Supply voltage range: 3V to 15V

■ Tenth power TTL compatible: Drive 2 LPT²L loads

■ High noise immunity: 0.45 V_{CC} (typ.)

■ Low power: 50 nW (typ.)

■ Medium speed operation: 10 MHz (typ.) with 10V supply

Applications

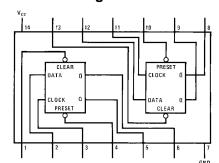
- Automotive
- Data terminals
- Instrumentation
- · Medical electronics
- Alarm system
- Industrial electronics
- · Remote metering
- · Computers

Ordering Code:

Order Number	Package Number	Package Description		
MM74C74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow		
MM74C74N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide		

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

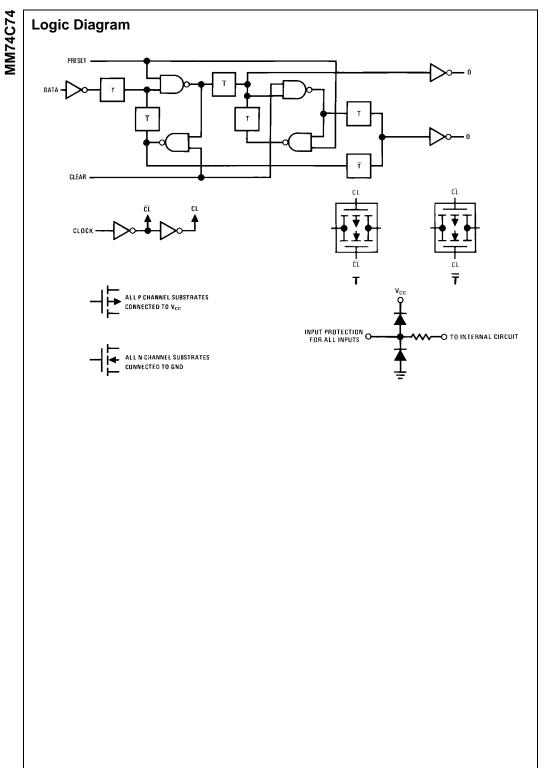


Note: A logic "0" on clear sets Q to logic "0".
A logic "0" on preset sets Q to logic "1". **Top View**

Truth Table

Preset	Clear	Q _n	$\overline{\mathbf{Q}}_{\mathbf{n}}$		
0	0	0	0		
0	1	1	0		
1	0	0	1		
1	1	Q _n (Note 1)	\overline{Q}_{n} (Note 1)		

Note 1: No change in output from previous state.





Absolute Maximum Ratings(Note 2)

Power Dissipation

Dual-In-Line 700 mW

Small Outline 500 mW

Lead Temperature

 $\begin{tabular}{ll} \mbox{(Soldering, 10 seconds)} & 260 \mbox{°C} \\ \mbox{Operating V_{CC} Range} & 3V \mbox{ to 15V} \\ \end{tabular}$

V_{CC} (Max) 18V

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO	CMOS	•	'			
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 5V	3.5			V
		V _{CC} = 10V	80			
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5V			1.5	V
		V _{CC} = 10V			2.0	
V _{OUT(1)}	Logical "1" Output Voltage	V _{CC} = 5V	4.5			V
		V _{CC} = 10V	9.0			
V _{OUT(0)}	Logical "0" Output Voltage	V _{CC} = 5V			0.5	V
		V _{CC} = 10V			1.0	
I _{IN(1)}	Logical "1" Input Current	V _{CC} = 15V			1.0	μΑ
I _{IN(0)}	Logical "0" Input Current	V _{CC} = 15V	-1.0			μΑ
I _{CC}	Supply Current	V _{CC} = 15V		0.05	60	μА
CMOS/LPT	TL INTERFACE	•	'			
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 4.75V	V _{CC} - 1.5			
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 4.75V			0.8	V
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_D = -360 \mu A$	2.4			V
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_D = 360 \mu A$			0.4	V
	RIVE (See Family Characteristics	Data Sheet)			•	•
I _{SOURCE}	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$	-1.75			mA
		$T_A = 25^{\circ}C$, $V_{OUT} = 0V$	-1.75			IIIA
I _{SOURCE}	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$	-8.0			mA
		T _A = 25°C, V _{OUT} = 0V	-8.0			
I _{SINK}	Output Sink Current	V _{CC} = 5V, V _{IN(1)} = 5V	1.75			mA
		$T_A = 25^{\circ}C$, $V_{OUT} = V_{CC}$				
I _{SINK}	Output Sink Current	V _{CC} = 10V, V _{IN(1)} = 10V	8.0			mA
		$T_A = 25$ °C, $V_{OUT} = V_{CC}$	0.0			

Distributor of Fairchild Semiconductor: Excellent Integrated System Limited Datasheet of MM74C74N - IC D-TYPE POS TRG DUAL 14DIP

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MM74C74

 t_{S0}, t_{S1}

 t_{H0}, t_{H1}

t_{PW1}

t_{PW2}

t_r, t_f

 f_{MAX}

 C_{PD}

$T_A = 25^{\circ}C, \; C_L = 50 \; \text{pF}, \; \text{unless otherwise noted}$ Symbol Parameter Conditions Min Тур Max Units C_IN Input Capacitance Any Input (Note 4) рF 5.0 Propagation Delay Time to a $V_{CC} = 5V$ 180 300 t_{pd} ns $V_{CC} = 10V$ Logical "0" t_{pd0} or Logical "1" 70 110 t_{pd1} from Clock to Q or Q Propagation Delay Time to a $V_{CC} = 5V$ t_{pd} Logical "0" from Preset or Clear 110 $V_{CC} = 10V$ 70 Propagation Delay Time to a $V_{CC} = 5V$ 250 400 t_{pd} ns Logical "1" from Preset or Clear 150 $V_{CC} = 10V$ 100

50

20

-20

-8.0

100

40

100

40

3.5

8.0

40

0

250

100

160

70

40

15.0

5.0

2.0

5.0

ns

ns

ns

ns

μs

MHz

рF

 $V_{CC} = 5V$

 $V_{CC} = 10V$

 $V_{CC} = 5V$

 $V_{CC} = 10V$

 $V_{CC} = 5V$

V_{CC} = 10V

 $V_{CC} = 5V$

V_{CC} = 10V

 $V_{CC} = 5V$

 $V_{CC} = 10V$

 $V_{CC} = 5V$

 $V_{CC} = 10V$

(Note 5)

Note 3: AC Parameters are guaranteed by DC correlated testing

Maximum Clock Frequency

Power Dissipation Capacitance

AC Electrical Characteristics (Note 3)

Time Prior to Clock Pulse that

Data Must be Present t_{SETUP}

Time after Clock Pulse that

Data Must be Held

Width (t_{WL} = t_{WH})
Minimum Preset and

Clear Pulse Width

and Fall Time

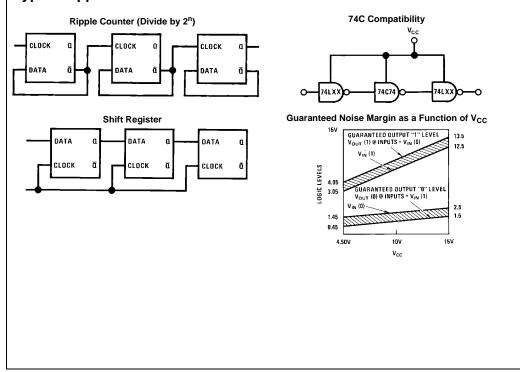
Maximum Clock Rise

Minimum Clock Pulse

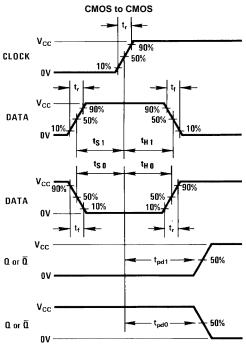
Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.

Typical Applications

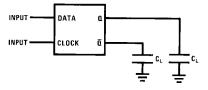


Switching Time Waveform

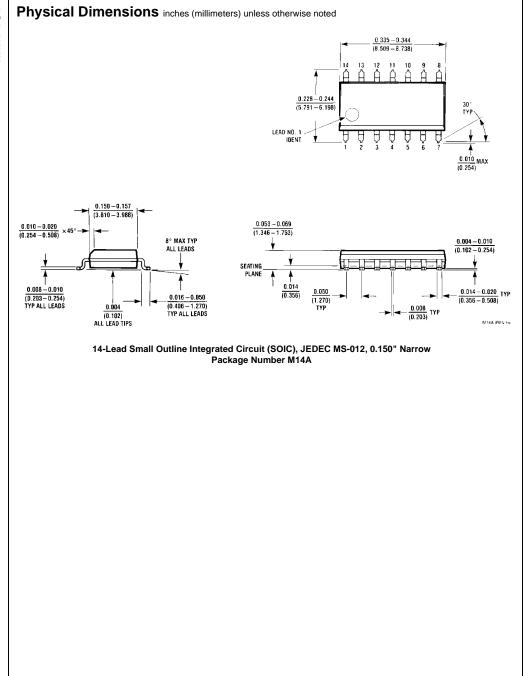


 $t_r = t_f = 20 \text{ ns}$

AC Test Circuit









Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 14 13 12 11 10 9 8 14 13 12 INDEX $\frac{0.250\pm0.010}{(6.350\pm0.254)}$ PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ $\frac{0.300 - 0.320}{(7.620 - 8.128)}$ 0.065 0.145 - 0.200(1.651) (3.683 - 5.080)<u></u> 0.008 - 0.016 (0.203 - 0.406) TYP 95°±5 (0.508) $\begin{array}{r} \hline 0.125 - 0.150 \\ \hline (3.175 - 3.810) \end{array}$ 0.280 (1.905 ± 0.381) 0.014-0.023 TYP (7.112)-MIN $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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N14A (REV.F)