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<u>Fairchild Semiconductor</u> <u>74F258APC</u>

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April 1988 Revised January 2004

74F258A

Quad 2-Input Multiplexer with 3-STATE Outputs

General Description

The 74F258A is a quad 2-input multiplexer with 3-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (OE) input, allowing the outputs to interface directly with bus-oriented systems.

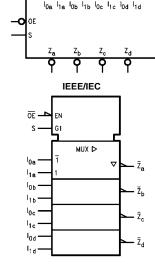
Features

- Multiplexer expansion by tying outputs together
- Inverting 3-STATE outputs

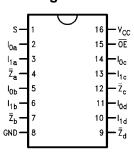
Ordering Code:

Order Number	Package Number	Package Description
74F258ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Dia Name	Donasistics.	U.L.	Input I _{IH} /I _{IL}		
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}		
S	Common Data Select Input	1.0/1.0	20 μA/–0.6 mA		
ŌĒ	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA		
I _{0a} –I _{0d}	Data Inputs from Source 0	1.0/1.0	20 μA/–0.6 mA		
I _{1a} –I _{1d}	Data Inputs from Source 1	1.0/1.0	20 μA/–0.6 mA		
$\overline{Z}_a - \overline{Z}_d$	3-STATE Inverting Data Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)		

Truth Table

Output Enable	Select Input	Data Inputs		Output
OE	s	I ₀	l ₁	z
Н	Х	Х	Х	Z
L	Н	X	L	Н
L	Н	X	Н	L
L	L	L	Χ	Н
L	L	Н	Х	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial Z = High Impedance

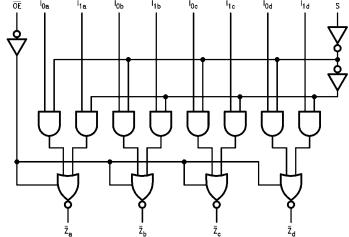
Functional Description

The 74F258A is a quad 2-input multiplexer with 3-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the l_{0x} inputs are selected and when Select is HIGH, the l_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 74F258A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equation for the outputs is shown below:

$$\overline{Z}_n = \overline{OE} \bullet (I_{1n} \bullet S + I_{0n} \bullet \overline{S})$$

When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-STATE devices whose outputs are tied together are designed so there is no overlap.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays



Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

Storage Temperature Ambient Temperature under Bias -55°C to +125°C Junction Temperature under Bias -55°C to +150°C

V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V Input Voltage (Note 2) -0.5V to +7.0V Input Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to $V_{\mbox{\footnotesize CC}}$ 3-STATE Output -0.5V to +5.5V

in LOW State (Max) twice the rated I_{OL} (mA) ESD Last Passing Voltage (Min) 4000V

Current Applied to Output

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions	
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH	10% V _{CC}	2.5					I _{OH} = -1 mA	
	Voltage	10% V _{CC}	2.4			V	Min	$I_{OH} = -3 \text{ mA}$	
		5% V _{CC}	2.7			V	IVIII	$I_{OH} = -1 \text{ mA}$	
		5% V _{CC}	2.7					$I_{OH} = -3 \text{ mA}$	
V _{OL}	Output LOW Voltage	10% V _{CC}			0.5	V	Min	I _{OL} = 24 mA	
I _{IH}	Input HIGH				5.0	^	Mau	\/ 0.7\/	
	Current				5.0	μΑ	Max	V _{IN} = 2.7V	
I _{BVI}	Input HIGH Current Breakdown Test				7.0	μА	Max	V _{IN} = 7.0V	
					7.0				
I _{CEX}	Output HIGH				50	μА	Max		
	Leakage Current				50	μΑ	IVIAX	$V_{OUT} = V_{CC}$	
V_{ID}	Input Leakage		4.75			V	0.0	I _{ID} = 1.9 μA	
	Test		4.75			V	0.0	All Other Pins Grounded	
I _{OD}	Output Leakage				3.75	μА	0.0	V _{IOD} = 150 mV	
	Circuit Current			3.75	μА	0.0	All Other Pins Grounded		
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V	
I _{OZH}	Output Leakage Current				50	μΑ	Max	V _{OUT} = 2.7V	
I _{OZL}	Output Leakage Current				-50	μΑ	Max	V _{OUT} = 0.5V	
Ios	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V	
I _{ZZ}	Bus Drainage Test				500	μΑ	0.0V	$V_{OUT} = V_{CC}$	
I _{CCH}	Power Supply Current			6.2	9.5	mA	Max	V _O = HIGH	
I _{CCL}	Power Supply Current			15.1	23	mA	Max	$V_O = LOW$	
I _{CCZ}	Power Supply Current			11.3	17	mA	Max	V _O = HIGH Z	



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74F258A

AC Electrical Characteristics

Symbol	nbol Parameter		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_{A} = -5^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V$ $C_{L} = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = 5.0V$ $C_L = 50 \text{ pF}$		
		Min	Тур	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay	2.5		5.3	2.0	7.5	2.0	6.0	ns	
t _{PHL}	I_n to \overline{Z}_n	1.0		4.0	1.0	6.0	1.0	5.0		
t _{PLH}	Propagation Delay	3.0		7.5	3.0	9.5	3.0	8.5	ns	
t _{PHL}	S to \overline{Z}_n	2.5		7.0	2.5	9.0	2.5	8.0		
t _{PZH}	Output Enable Time	2.0		6.0	2.0	8.0	2.0	7.0		
t _{PZL}		2.5		7.0	2.5	9.0	2.5	8.0		
t _{PHZ}	Output Disable Time	2.0		6.0	1.5	7.0	2.0	7.0	ns	
t _{PLZ}		2.0		6.0	2.0	8.5	2.0	7.0		

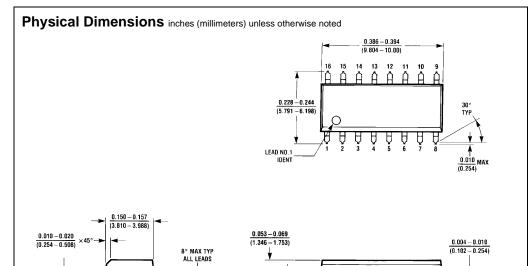
SEATING PLANE - 0.020 TYP - 0.508)

M16A (REV H)

0.014

0.008 (0.203) TYP





16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

0.016 - 0.050

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LIFE SUPPORT POLICY

0.008 - 0.010

(0.203 - 0.254) TYP ALL LEADS

0.004 (0.102) ALL LEAD TIPS

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