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Fairchild Semiconductor
74F323PC

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FAIRCHILD SEMICONDUCTOR™

April 1988
Revised August 1999

74F323

Octal Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

General Description

The 74F323 is an 8-bit universal shift/storage register with 3-STATE outputs. Its function is similar to the 74F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

Features

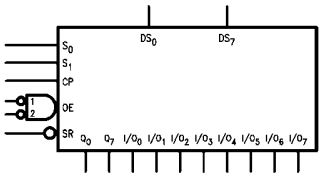
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- 3-STATE outputs for bus-oriented applications

Ordering Code:

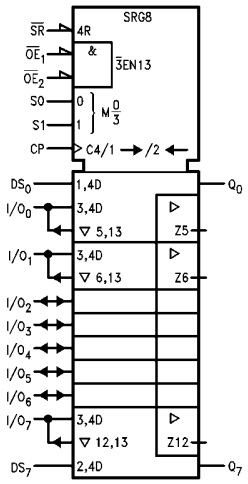
Order Number	Package Number	Package Description
74F323SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F323PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

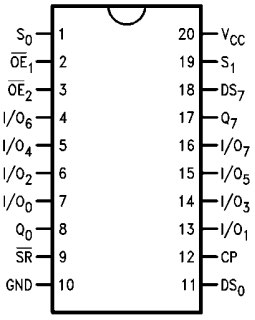
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
DS_0	Serial Data Input for Right Shift	1.0/1.0	20 µA/–0.6 mA
DS_7	Serial Data Input for Left Shift	1.0/1.0	20 µA/–0.6 mA
S_0, S_1	Mode Select Inputs	1.0/2.0	20 µA/–1.2 mA
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 µA/–0.6 mA
I/O_0–I/O_7	Multiplexed Parallel Data Inputs	3.5/1.083	70 µA/–0.65 mA
	3-STATE Parallel Data Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)
Q_0, Q_7	Serial Outputs	50/33.3	–1 mA/20 mA

Functional Description

The 74F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

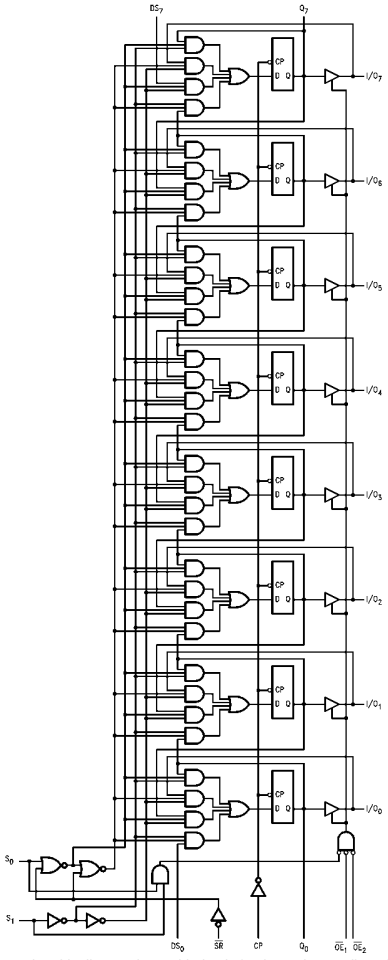
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The 3-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
SR	S_1	S_0	CP	
L	X	X	⌐	Synchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (Q_0, Q_7)
		10% V_{CC}	2.4					I_{OH} = −3 mA (I/O_n)
		5% V_{CC}	2.7					I_{OH} = −1 mA (Q_0, Q_7)
		5% V_{CC}	2.7					I_{OH} = −3 mA (I/O_n)
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (Q_0, Q_7)
		10% V_{CC}			0.5			I_{OL} = 24 mA (I/O_n)
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V (Non I/O Inputs)
I_{BVIT}	Input HIGH Current Breakdown (I/O)				0.5	mA	Max	V_{IN} = 5.5V (I/O Inputs)
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (CP, DS_0, DS_7, $\overline{SR}$, $\overline{OE_1}$, $\overline{OE_2}$)
					−1.2	mA	Max	V_{IN} = 0.5V (S_0, S_1)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			68	95	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			68	95	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			68	95	mA	Max	V_O = HIGH Z

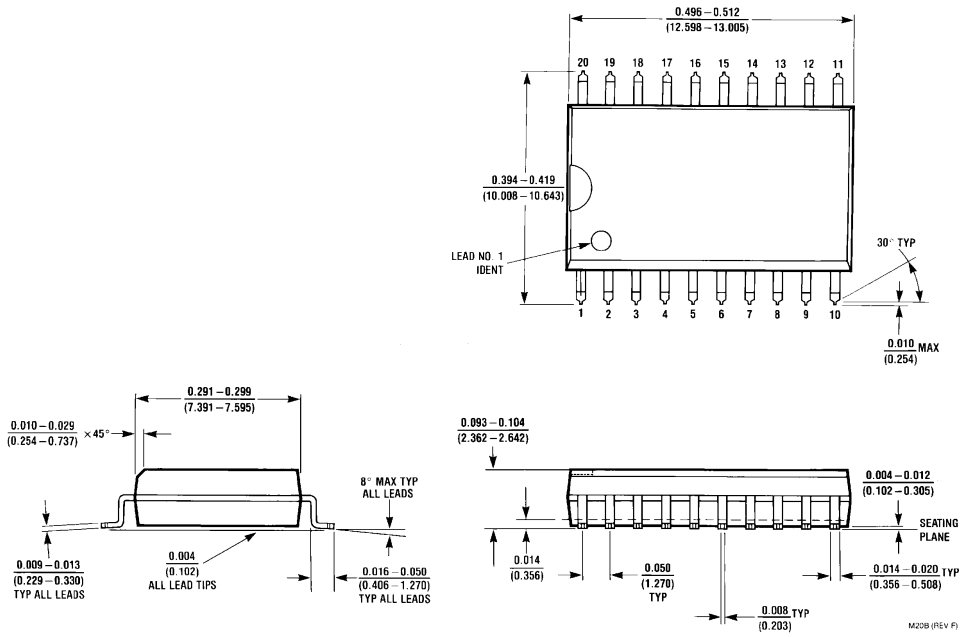
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Input Frequency	70	100		70		MHz
t_{PLH}	Propagation Delay	4.0	7.0	8.0	4.0	8.5	ns
t_{PHL}	CP to Q_0 or Q_7	4.5	6.5	8.0	4.5	8.5	
t_{PLH}	Propagation Delay	3.5	7.0	9.0	3.5	10.0	
t_{PHL}	CP to I/O_n	4.0	8.5	9.0	4.0	10.0	
t_{PZH}	Output Enable Time	3.5	6.0	8.0	3.5	9.0	ns
t_{PZL}		4.0	7.0	10.0	4.0	11.0	
t_{PHZ}	Output Disable Time	2.0	4.5	6.0	2.0	7.0	
t_{PLZ}		1.0	4.0	5.5	1.0	6.5	
t_{PZH}	Output Enable Time	3.5		9.0	3.5	10.0	ns
t_{PZL}	S_n to I/O_n	4.0		10.0	4.0	11.0	
t_{PHZ}	Output Disable Time	2.5		6.0	2.5	7.0	ns
t_{PLZ}	S_n to I/O_n	1.0		5.5	1.5	6.5	

AC Operating Requirements

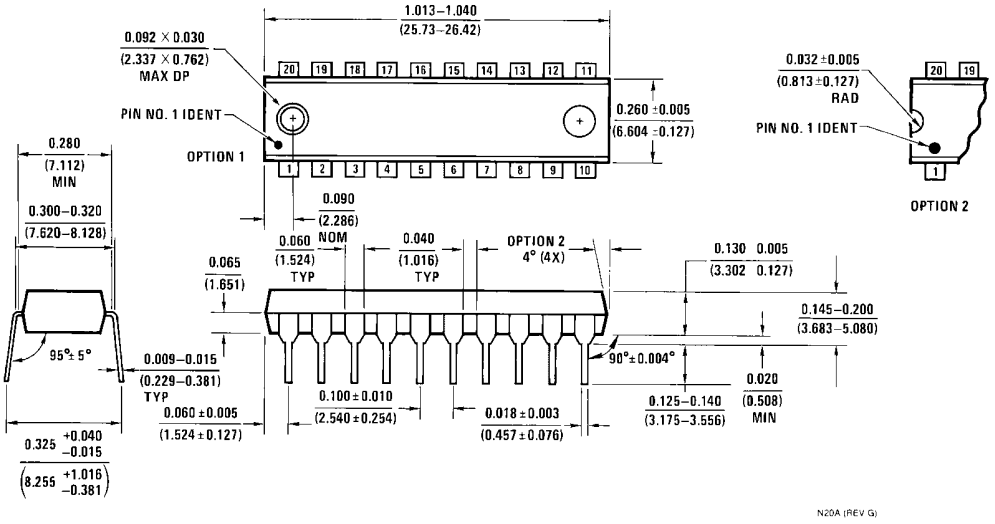
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	8.5		8.5		ns
$t_S(L)$	S_0 or S_1 to CP	8.5		8.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	S_0 or S_1 to CP	0		0		
$t_S(H)$	Setup Time, HIGH or LOW	5.0		5.0		ns
$t_S(L)$	I/O_n, DS_0, DS_7 to CP	5.0		5.0		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		
$t_H(L)$	I/O_n, DS_0, DS_7 to CP	2.0		2.0		
$t_S(H)$	Setup Time, HIGH or LOW	10.0		10.0		ns
$t_S(L)$	$\overline{SR}$ to CP	10.0		10.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	$\overline{SR}$ to CP	0		0		
$t_W(H)$	CP Pulse Width	5.0		5.0		ns
$t_W(L)$	HIGH or LOW	5.0		5.0		

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A