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DRV2665RGPR

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DRV2665 Piezo Haptic Driver with Integrated Boost Converter and Digital Front End

1 Features

- Integrated Digital Front End
  - Up to 400-kHz I^2C Bus Control
  - 100-Byte Internal FIFO Interface
  - Immersion TS5000-Compliant
  - Optional Analog Inputs
- High Voltage Piezo-Haptic Driver
  - Drives up to 100 nF at 200 V_{PP} and 300 Hz
  - Drives up to 150 nF at 150 V_{PP} and 300 Hz
  - Drives up to 330 nF at 100 V_{PP} and 300 Hz
  - Drives up to 680 nF at 50 V_{PP} and 300 Hz
  - Differential Output
- 105-V Integrated Boost Converter
  - Adjustable Boost Voltage
  - Adjustable Boost Current Limit
  - Integrated Power FET and Diode
  - No Transformer Required
- 2-ms Fast Start Up Time
- 3- to 5.5-V Wide Supply Voltage Range
- 1.8-V Compatible, V_{DD} Tolerant Digital Pins

2 Applications

- Mobile Phones
- Tablets
- Portable Computers
- Keyboards and Mice
- Electronic Gaming
- Touch Enabled Devices

3 Description

The DRV2665 device is a piezo haptic driver with integrated 105-V boost switch, integrated power diode, integrated fully-differential amplifier, and integrated digital front end. This versatile device is capable of driving both high-voltage and low-voltage piezo haptic actuators. The input signal can be driven as haptic packets over the I^2C port or through the analog inputs.

The digital interface of the DRV2665 device is available through an I^2C compatible bus. A digital interface relieves the costly processor burden of the PWM generation or additional analog channel requirements in the host system. Any writes to the internal first-in, first-out buffer (FIFO) will automatically wake up the device and begin playing the waveform after the 2 ms internal start-up procedure. When the data flow stops or the FIFO under-runs, the DRV2665 device will automatically enter a pop-less shutdown procedure.

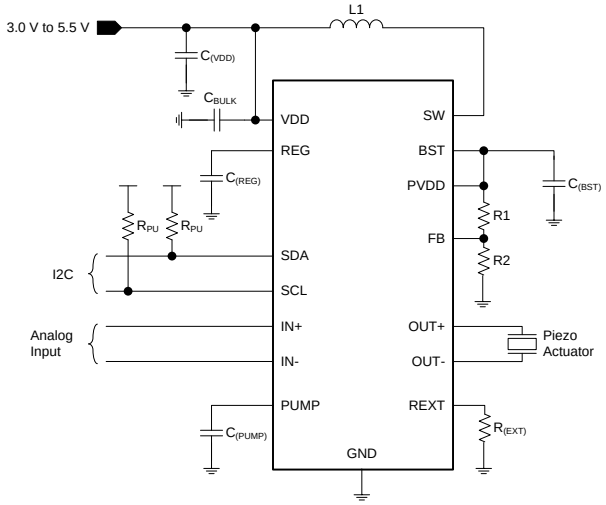
The boost voltage is set using two external resistors, and the boost current limit is programmable through the R_{EXT} resistor. A typical start-up time of 2 ms makes the DRV2665 device an ideal piezo driver for fast haptic responses. Thermal overload protection prevents the device from being damaged when overdriven.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
DRV2665	QFN (20)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2014) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added Exception description to *Brownout Protection* section ... 11

Changes from Original (May 2012) to Revision A — **Page**

- Changed from one-page data sheet to full data sheet in product folder ... 1

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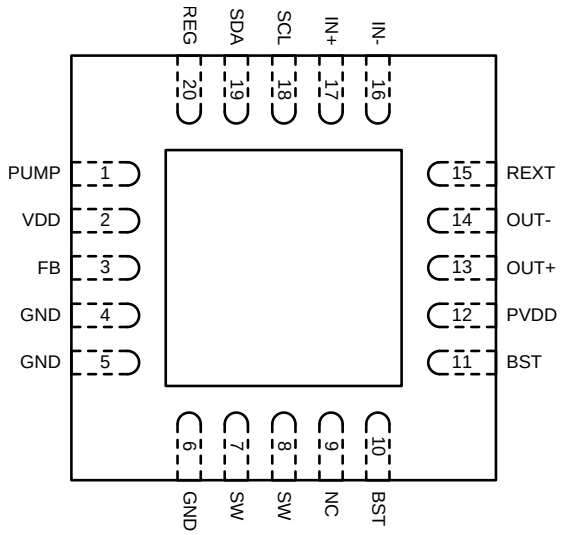
5 Pin Configuration and Functions

RGP Package
20-Pin QFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
PUMP	1	P	Internal charge pump voltage
VDD	2	P	3- to 5.5-V supply input. A 1 µF-capacitor is required.
FB	3	I	Boost feedback
GND	4, 5, 6	P	Supply ground
SW	7, 8	P	Internal boost switch pin
NC	9	—	No connect
BST	10, 11	P	Boost output voltage. A 0.1-µF capacitor is required.
PVDD	12	P	High-voltage amplifier input voltage
OUT+	13	O	Positive haptic driver differential output
OUT-	14	O	Negative haptic driver differential output
REXT	15	I	Sets boost current limit. Resistor to ground.
IN-	16	I	Negative analog input
IN+	17	I	Positive analog input
SCL	18	I	I^2C clock
SDA	19	I/O	I^2C data
REG	20	O	1.8-V regulator output. A 0.1-µF capacitor is required.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage, V_{DD}		–0.3	6	V
Input voltage, V_I	SDA, SCL, IN+, IN–, FB	–0.3	V_{DD} + 0.3	V
Boost voltage	BST, SW, OUT+, OUT–, PVDD	–0.3	120	V
Operating free-air temperature, T_A		–40	70	°C
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3		5.5	V
V_{BST}	Boost voltage		15		105	V
V_{IN}	Differential input voltage			1.8		V
C_L	Load capacitance	V_{BST} = 105 V, Frequency = 500 Hz, V_{OUT} = 200 V_{PP}			50	nF
		V_{BST} = 105 V, Frequency = 300 Hz, V_{OUT} = 200 V_{PP}			100	
		V_{BST} = 80 V, Frequency = 300 Hz, V_{OUT} = 150 V_{PP}			150	
		V_{BST} = 55 V, Frequency = 300 Hz, V_{OUT} = 100 V_{PP}			330	
		V_{BST} = 30 V, Frequency = 300 Hz, V_{OUT} = 50 V_{PP}			680	
		V_{BST} = 25 V, Frequency = 300 Hz, V_{OUT} = 40 V_{PP}			1000	
		V_{BST} = 15 V, Frequency = 300 Hz, V_{OUT} = 20 V_{PP}			3000	
R_{EXT}	Current limit control resistor		6		35	kΩ
L	Inductance for boost converter		3.3			µH

6.4 Thermal Information

THERMAL METRIC(1)		DRV2665 RGP (QFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

T_A = 25 °C, V_{DD} = 3.6 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG}	Voltage at the REG pin			1.6	1.75	1.9	V
I_{IL}	Digital low-level input current		SDA, SCL V_{DD} = 3.6 V, V_I = 0 V			1	µA
I_{IH}	Digital high-level input current		SDA, SCL V_{DD} = 3.6 V, V_I = V_{DD}			1	uA
V_{IL}	Digital low-level input voltage		SDA, SCL V_{DD} = 3.6 V			0.5	V
V_{IH}	Digital high-level input voltage		SDA, SCL V_{DD} = 3.6 V	1.4			V
V_{OL}	Digital low-level output voltage		SDA 3-mA sink current			0.4	V
I_{SD}	Shutdown current		V_{DD} = 3.6 V, STANDBY = 1		10		µA
I_Q	Quiescent current	Digital mode	V_{DD} = 3.6 V, STANDBY = 0		130	175	µA
		Analog mode	V_{DD} = 3.6 V, analog input mode, V_{BST} = 105 V		24		mA
			V_{DD} = 3.6 V, analog input mode, V_{BST} = 80 V		13		
			V_{DD} = 3.6 V, analog input mode, V_{BST} = 50 V		9		
			V_{DD} = 3.6 V, analog input mode, V_{BST} = 30 V		5		
R_{IN}	Input impedance		IN+, IN–; All gains		100		kΩ
$V_{OUT(FS)}$	Full-scale output voltage (digital mode)		GAIN[1:0] = 00	49	50	51	V_{PP}
			GAIN[1:0] = 01	98	100	102	
			GAIN[1:0] = 10	147	150	153	
			GAIN[1:0] = 01	196	200	204	
$V_{OUT(OS)}$	Output offset		All gains	–0.25		0.25	V
BW	Amplifier bandwidth		GAIN[1:0] = 00, V_{OUT} = 50 V_{PP}, no load		20		kHz
			GAIN[1:0] = 01, V_{OUT} = 100 V_{PP}, no load		10		
			GAIN[1:0] = 10, V_{OUT} = 150 V_{PP}, no load		7.5		
			GAIN[1:0] = 11, V_{OUT} = 200 V_{PP}, no load		5		
$I_{BAT, AVG}$	Average battery current during operation		C_L = 220 nF, f = 200 Hz, V_{BST} = 30 V, GAIN[1:0] = 00, V_{OUT} = 50 V_{PP}		69		mA
			C_L = 680 nF, f = 150 Hz, V_{BST} = 30 V, GAIN[1:0] = 00, V_{OUT} = 50 V_{PP}		75		
			C_L = 680 nF, f = 300 Hz, V_{BST} = 30 V, GAIN[1:0] = 00, V_{OUT} = 50 V_{PP}		115		
			C_L = 22 nF, f = 200 Hz, V_{BST} = 80 V, GAIN[1:0] = 10, V_{OUT} = 150 V_{PP}		67		
			C_L = 47 nF, f = 150 Hz, V_{BST} = 105 V, GAIN[1:0] = 11, V_{OUT} = 200 V_{PP}		210		
			C_L = 47 nF, f = 300 Hz, V_{BST} = 105 V, GAIN[1:0] = 11, V_{OUT} = 200 V_{PP}		400		
THD+N	Total harmonic distortion plus noise		f = 300 Hz, V_{OUT} = 200 V_{PP}		1%		
f_S	Output sample rate		Digital playback engine sample rate	7.8	8	8.05	kHz

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6.6 Timing Requirements

T_A = 25 °C, V_{DD} = 3.6 V (unless otherwise noted). For timing diagrams, see Figure 1 and Figure 2.

		MIN	NOM	MAX	UNIT
f_{SCL}	Frequency at the SCL pin with no wait states			400	kHz
$t_{w(H)}$	Pulse duration, SCL high	0.6			µs
$t_{w(L)}$	Pulse duration, SCL low	1.3			µs
$t_{su(1)}$	Setup time, SDA to SCL	100			ns
$t_{h(1)}$	Hold time, SCL to SDA	10			ns
t_{BUF}	Bus free time between stop and start condition	1.3			µs
$t_{su(2)}$	Setup time, SCL to start condition	0.6			µs
$t_{h(2)}$	Hold time, start condition to SCL	0.6			µs
$t_{su(3)}$	Setup time, SCL to stop condition	0.6			µs

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{start}	Start-up time	Time from I^2C write until boost and amplifier are fully enabled		2		ms

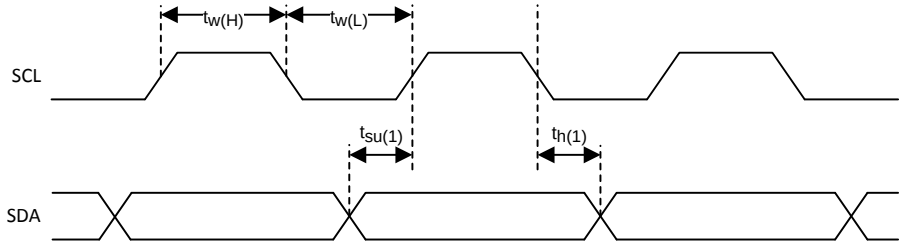

Figure 1. SCL and SDA Timing

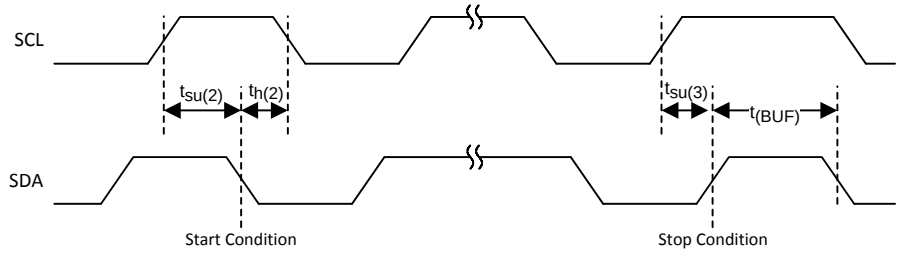

Figure 2. Timing for Start and Stop Conditions

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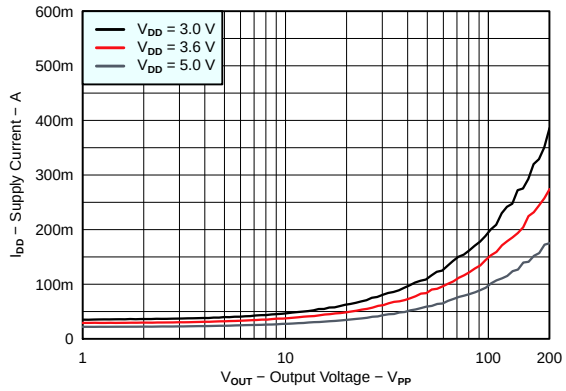
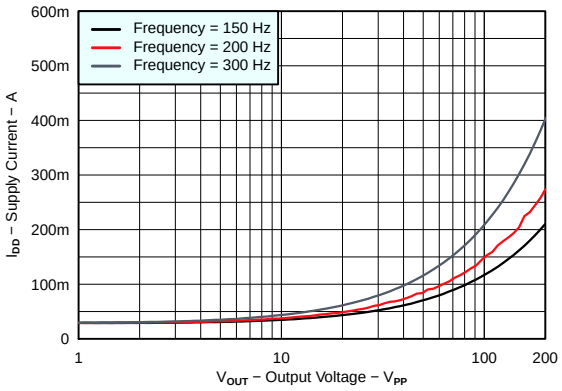
6.8 Typical Characteristics



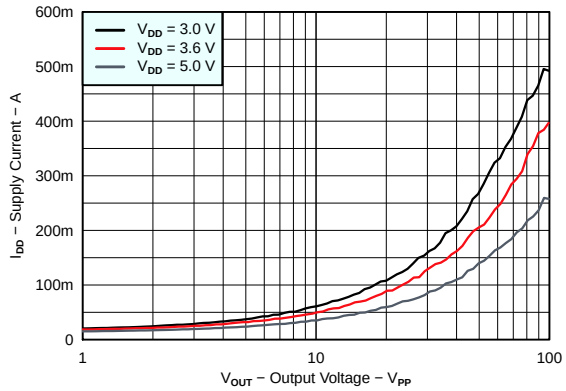
f = 200 Hz PVDD = 105 V
C_{LOAD} = 47 nF Gain = 40 dB

Figure 3. Supply Current vs Output Voltage



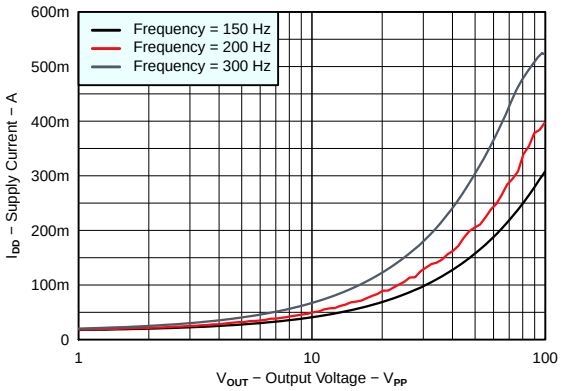
V_{DD} = 3.6 V PVDD = 105 V
C_{LOAD} = 47 nF Gain = 40 dB

Figure 4. Supply Current vs Output Voltage



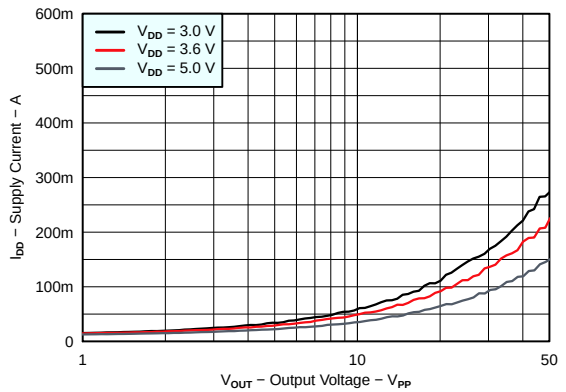
f = 200 Hz PVDD = 55 V
C_{LOAD} = 330 nF Gain = 34 dB

Figure 5. Supply Current vs Output Voltage



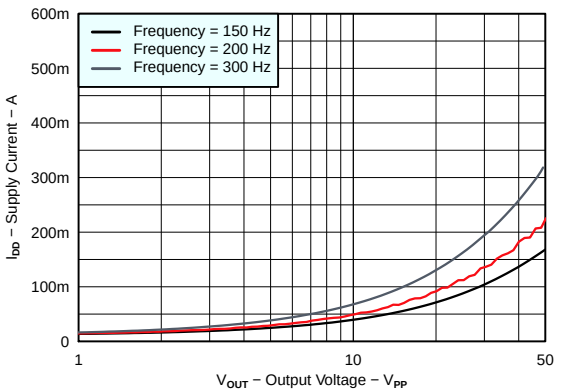
V_{DD} = 3.6 V PVDD = 55 V
C_{LOAD} = 330 nF Gain = 34 dB

Figure 6. Supply Current vs Output Voltage



f = 200 Hz PVDD = 30 V
C_{LOAD} = 680 nF Gain = 28 dB

Figure 7. Supply Current vs Output Voltage



V_{DD} = 3.6 V PVDD = 30 V
C_{LOAD} = 680 nF Gain = 28 dB

Figure 8. Supply Current vs Output Voltage

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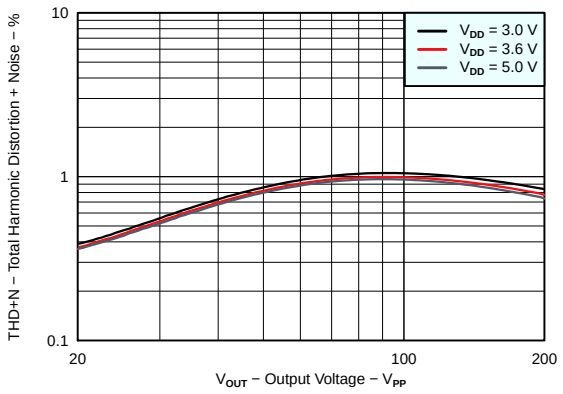
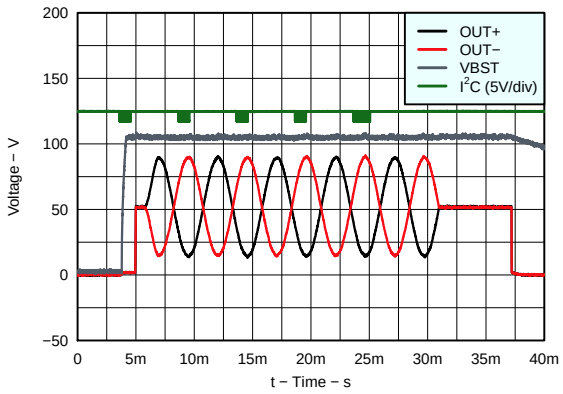
Typical Characteristics (continued)



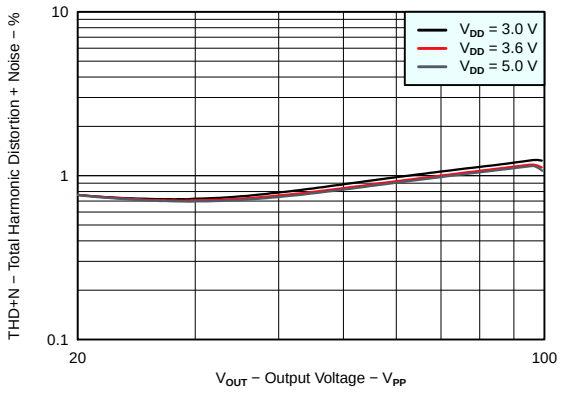
f = 200 Hz PVDD = 105 V
C_{LOAD} = 47 nF Gain = 40 dB

Figure 9. Total Harmonic Distortion + Noise vs Output Voltage



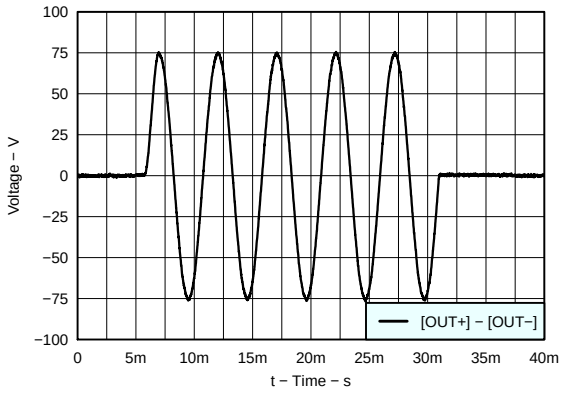
V_{DD} = 3.6 V PVDD = 105 V
C_{LOAD} = 47 nF Gain = 40 dB

Figure 10. Typical Waveform



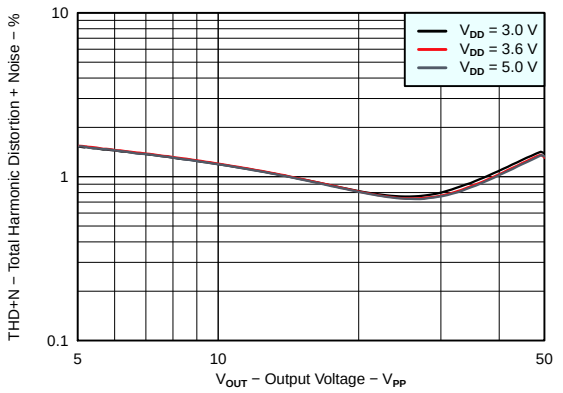
f = 200 Hz PVDD = 55 V
C_{LOAD} = 330 nF Gain = 34 dB

Figure 11. Total Harmonic Distortion + Noise vs Output Voltage



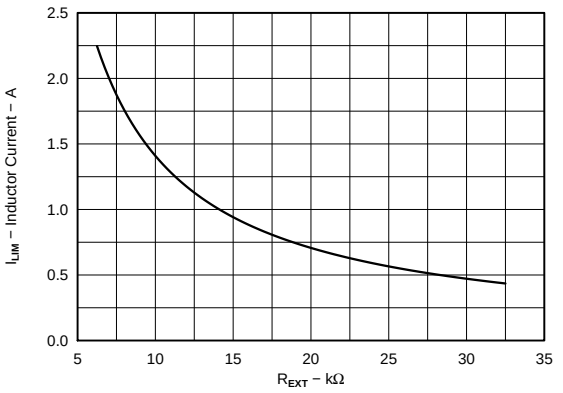
V_{DD} = 3.6 V PVDD = 55 V
C_{LOAD} = 330 nF Gain = 34 dB

Figure 12. Typical Waveform – Differential



f = 200 Hz PVDD = 30 V
C_{LOAD} = 680 nF Gain = 28 dB

Figure 13. Total Harmonic Distortion + Noise vs Output Voltage



V_{DD} = 3.6 V PVDD = 30 V
C_{LOAD} = 680 nF Gain = 28 dB

Figure 14. I_{LIM} vs $R_{(EXT)}$

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7 Detailed Description

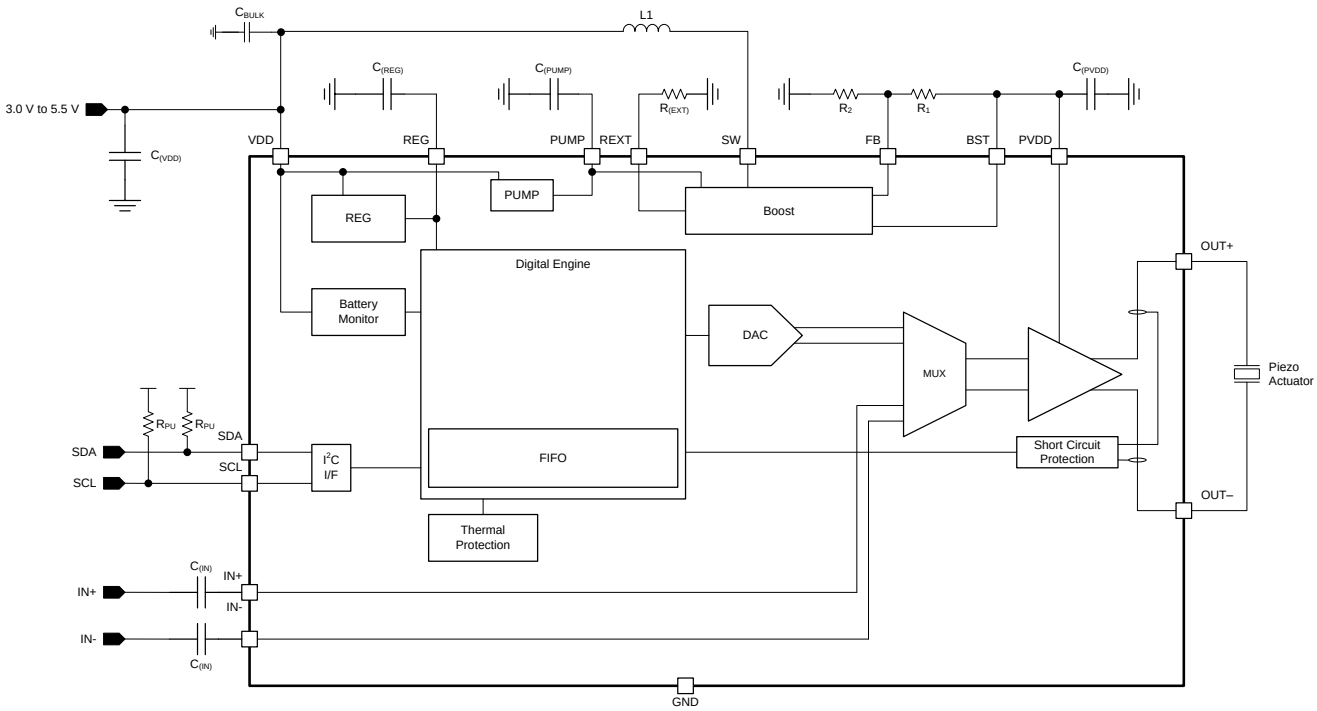
7.1 Overview

The DRV2665 device is a piezo haptic driver with integrated boost switch, integrated power diode, integrated fully-differential amplifier, and integrated digital front end. This versatile device is capable of driving both high-voltage and low-voltage piezo haptic actuators. The input signal can be driven over the I^2C port or the analog inputs.

The digital interface of the DRV2665 device is available through an I^2C compatible bus. A digital interface relieves the costly processor burden of PWM generation or additional analog channel requirements in the host system. Any writes to the internal FIFO automatically wakes up the device and begin playing the waveform after the 2 ms internal startup procedure. When the data flow stops or the FIFO under runs, the device automatically enters a pop-less shutdown procedure.

The boost voltage is set using two external resistors, and the boost current limit is programmable through the R_{EXT} resistor. A typical start-up time of 2 ms makes the DRV2665 an ideal piezo driver for fast haptic responses. Thermal overload protection prevents the device from being damaged when overdriven.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Support for Haptic Piezo Actuators

The DRV2665 device supports haptic piezo actuators of up to 200 V_{PP}.

7.3.2 Flexible Front End Interface

The DRV2665 device supports multiple approaches to launch and control haptic effects, that are detailed in *Device Functional Modes*.

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Feature Description (continued)

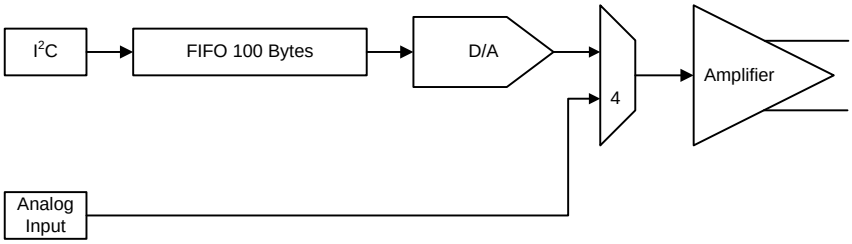

Figure 15. Front-End Interface

7.3.3 Ramp Down Behavior

If the user leaves the state of the DAC at any level other than mid-scale (0x00), the DAC automatically ramps down at a safe rate after the timeout period has expired. If the DRV2665 device is properly programmed, the ramp down sequence will never be used. This is a failsafe for any unavoidable interruptions to the playback process. Any writes to the FIFO during the ramp down period are discarded.

7.3.4 Low Latency Startup

The DRV2665 device features a fast startup time, that is essential for achieving low latency in haptic applications. When the STANDBY bit is transitioned from high to low, the device is ready for operation. The device logic automatically controls the internal boost converter and amplifier enable signals. The boost converter and amplifier are enabled only when needed and otherwise remain in a lower power idle state. When the device received a data byte through the FIFO interface, the boost converter and amplifier wake up and the internal logic sends the first sample through the internal DAC after the wake-up is completed. In the system application, the entire system latency must be kept to less than 30 ms total to be imperceptible to the end user. At a 2-ms wake-up time, the device is a small percentage of the total system latency.

If the EN_OVERRIDE bit is set, the device immediately enters the startup procedure and the boost converter and amplifier remain enabled, bypassing the internal controls. Subsequent transactions occur immediately with no wake-up overhead, but the boost converter and amplifier draw a quiescent current until the EN_OVERRIDE bit is cleared by the user.

7.3.5 Low Power Standby Mode

The DRV2665 device has a low-power standby mode through the I^2C interface that puts the device in its lowest power state. This mode is entered when the standby bit (STANDBY) is set from low to high. When the STANDBY bit is set high, no other mode of operation is enabled. When the STANDBY bit transitions from high to low, the device is readied for operation and may receive data.

7.3.6 Device Reset

The DRV2665 device has software-based reset functionality. When the DEV_RST bit is set, the device immediately stops any transaction in process, resets all of its internal registers to the default values, and enters standby mode.

7.3.7 Amplifier Gain

The amplifier gain determines the gain from IN+/IN– to OUT+/OUT– when using the analog playback mode. For digital playback, the gain is optimized for achieving approximately 50 V_{PP}, 100 V_{PP}, 150 V_{PP}, 200 V_{PP} without clipping. Note that clipping of the amplifier occurs if the expected peak voltage is greater than the boost converter output voltage (VBST)

The DRV2665 device gain is programmable according to Table 1.

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Feature Description (continued)

Table 1. Amplifier Gain Table

GAIN[1]	GAIN[0]	FULL SCALE PEAK VOLTAGE (V)	GAIN (dB) ANALOG MODE
0	0	25	28.8
0	1	50	34.8
1	0	75	38.4
1	1	100	40.7

7.3.8 Adjustable Boost Voltage

The output voltage of the integrated boost converter may be adjusted by a resistive feedback divider between the boost output voltage (VBST) and the feedback pin (FB). The boost voltage must be programmed to a value greater than the maximum peak signal voltage that the user expects to create with the device amplifier. Lower boost voltages achieve better system efficiency when lower amplitude signals are applied, thus the user must take care not to use a higher boost voltage than necessary. The maximum allowed boost voltage is 105 V.

7.3.9 Adjustable Current Limit

The current limit of the boost switch can be adjusted through a resistor to ground placed on the REXT pin. To avoid damage to both the inductor and the DRV2665 device, the programmed current limit must be less than the rated saturation limit of the inductor selected by the user. If the combination of the programmed limit and inductor saturation is not high enough, then the output current of the boost converter will not be high enough to regulate the boost output voltage under heavy load conditions. This then causes the boosted rail to sag, possibly causing distortion of the output waveform.

7.3.10 Internal Charge Pump

The DRV2665 device has an integrated charge pump to provide adequate gate drive for internal nodes. The output of this charge pump is placed on the PUMP pin. An X5R or X7R storage capacitor of 0.1 µF with a voltage rating of 10 V or greater must be placed at this pin.

7.3.11 Device Protection

7.3.11.1 Thermal Protection

The DRV2665 device contains an internal temperature sensor that shuts down both the boost converter and the high-voltage amplifier when the temperature threshold is exceeded. When the device temperature falls below the threshold, the device will restart operation automatically. Continuous operation of the device is not recommended. Most haptic use models only operate the device in short bursts. The thermal shutdown function protects the device from damage when overdriven, but usage models which drive the device into thermal shutdown must always be avoided.

7.3.11.2 Overcurrent Protection

If the load demands more current than what the DRV2665 device can supply, the device automatically clamps the output voltage to avoid damage.

7.3.11.3 Brownout Protection

The DRV2665 device has on-chip brownout protection. When activated, a reset signal is issued that returns the DRV2665 device to the initial default state. If the voltage regulator V_{REG} goes below the brownout protection threshold (V_{BOT}) the DRV2665 device automatically shuts down. When V_{REG} returns to the typical output voltage (1.75 V), the DRV2665 device returns to the initial device state. The brownout protection threshold, V_{BOT}, is typically at 0.84 V.

There is one exception to this behavior. The brownout circuit is designed to tolerate fast brownout conditions as shown by Case 1 in Figure 16. If the V_{DD} ramp-up rate is slower than 3.6 kV/s, then the device can fall into an unknown state. In such a situation, to return to the initial default state the device must be power-cycled with a V_{DD} ramp-up rate that is faster than 3.6 kV/s.

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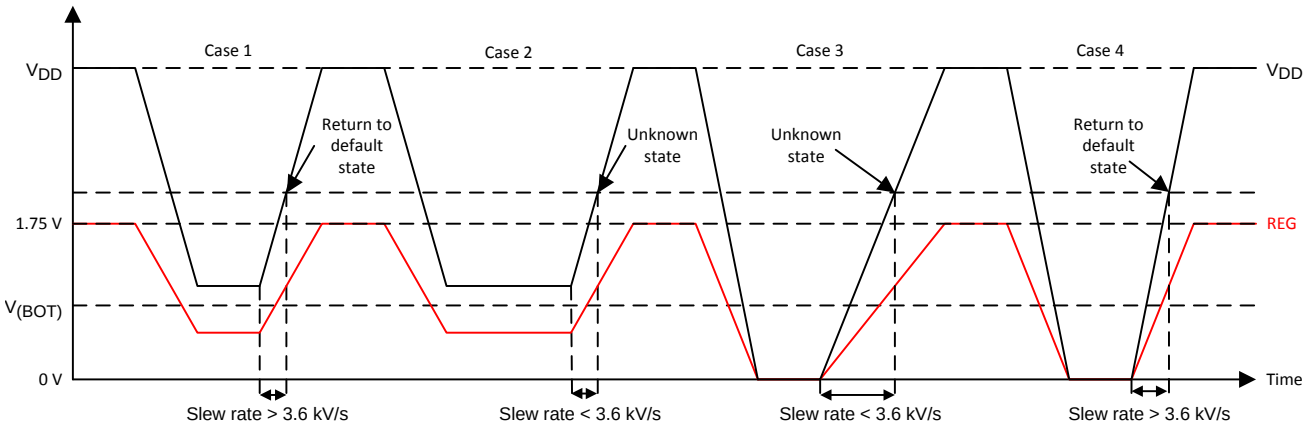

Figure 16. Brownout Behavior

7.4 Device Functional Modes

7.4.1 FIFO Mode

The DRV2665 device includes a 100-byte FIFO for real-time haptic waveform playback. The FIFO mode accepts 8-bit digital haptic waveform data over an I^2C compatible bus and writes it into an on-chip FIFO. The data is read out of the FIFO automatically at an 8-kHz sampling rate and fed into a digital-to-analog converter (DAC). The DAC then drives the high-voltage amplifier. This mode is utilized when the user writes directly to the I^2C FIFO entry address (0x0B). When the first data byte is written to the FIFO, the device goes through the proper start-up sequence and begins outputting the waveform automatically. An internal timing sequence waits approximately 2 ms before the first data is sent through the DAC and output by the device. It is important that the data values start and end at or near the mid-scale code (0x00) to avoid large steps at the beginning and end of the waveform. When the FIFO is empty, the device waits for the timeout period, and then enters into an idle state.

Because the speed of the serial interface could be faster than the read-out rate of the FIFO, the device does not acknowledge, or NAK, if the FIFO is full during a FIFO write transaction. If at any time the FIFO becomes completely full, the FIFO_FULL bit is set. When in this condition, the FIFO cannot accept more data without overwriting previous data that has not yet been played. If this occurs, the user must wait until data has had a chance to empty from the FIFO before sending more data. The data must be re-sent starting at the byte that received a NAK.

Any multi-byte I^2C write to the FIFO register is treated as a continuous write to the FIFO. Multi-byte writes are preferred for optimum performance. The FIFO interprets the incoming data as twos complement. This means the maximum full-scale code is 0x7F, the maximum negative voltage is 0x80, and the mid-scale is 0x00.

7.4.2 Analog Playback Mode

In analog playback mode the signal in the IN+/IN– inputs is amplified and played through the high-voltage amplifier. When the INPUT_MUX bit is set, the DRV2665 device switches the analog inputs (IN+/IN–) to the high-voltage amplifier. While in the analog mode, the gain is still register-selectable. Also, the high-voltage amplifier enable is controlled directly through the EN_OVERRIDE bit, so the EN_OVERRIDE bit must be set for the boost and amplifier to be active.

7.4.3 Low Voltage Operation Mode

The lowest gain setting is optimized for 50 V_{PP} with a boost voltage of 30 V. Some applications may not need 50 V_{PP}, so the user may elect to program the boost converter as low as 15 V to improve efficiency. When using boost voltages lower than 30 V, consider the following: First, to reduce boost ripple to an acceptable level, a 50-V rater, 0.22-µF boost capacitor is recommended. Second, the maximum code range of the digital interface is limited. For example, the user may elect to program the boost voltage to 25 V, and plan for a maximum drive signal of 40 V_{PP} at the actuator. Any digital code given to the FIFO that is greater than 20 V_P / 25 V_P x 127 = ±102 may induce clipping, so the user must only send digital codes between –102 and 102. Use of codes outside this range, for this example, may clip or drive the actuator beyond its rating.

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7.5 Programming

7.5.1 Programming the Boost Voltage

The boost output voltage is programmed through two external resistors as shown in Figure 17. The boost output voltage is given by Equation 1.

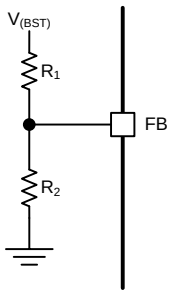

Figure 17. FB Network

$$V_{(BST)} = V_{(FB)} \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where

- $V_{(FB)}$ = 1.32 V

$V_{(BST)}$ must be programmed to a value of 5.0 V greater than the largest peak voltage expected in the system to allow adequate amplifier headroom. Because the programming range for the boost voltage extends to 105 V, the leakage current through the resistor divider can become significant. It is recommended that the sum of the resistances R_1 + R_2 be greater than 400 kΩ. When resistor values greater than 1 MΩ are used, PCB contamination may cause boost voltage inaccuracy. Exercise caution when soldering large resistances, and clean the area when finished for best results. Table 2 shows examples on how to configure the device for different output voltages.

Table 2. Boost Voltage Table

R_1	R_2	GAIN[1:0]	$V_{(BST)}$	FULL SCALE PEAK VOLTAGE (V)
402 kΩ	18.2 kΩ	00	30	25
392 kΩ	9.76 kΩ	01	55	50
768 kΩ	13 kΩ	10	80	75
768 kΩ	9.76 kΩ	11	105	100

7.5.2 Programming the Boost Current Limit

The peak current drawn from the supply through the inductor is set solely by the $R_{(EXT)}$ resistor. This peak current limit is independent of the inductance value chosen, but the inductor must be capable of handling this programmed limit. The relationship of $R_{(EXT)}$ and I_{LIM} is approximated by Equation 2.

$$R_{(EXT)} = \left(K \cdot \frac{V_{REF}}{I_{LIM}}\right) - R_{INT} \quad (2)$$

where

- K = 10500, , and
- V_{REF} = 1.35 V
- R_{INT} = 60 Ω
- I_{LIM} is the desired peak current limit through the inductor.

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7.5.3 I²C Interface

7.5.3.1 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The 8-bit address and data bytes are transferred with the most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on the SDA signal indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 18 shows a typical sequence. The master device generates the 7-bit slave address and the read-write (R/W) bit to start communication with a slave device. The master device then waits for an acknowledge condition. The slave device holds the SDA signal low during the acknowledge clock period to indicate acknowledgment. When this acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus a R/W bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection.

The number of bytes that can be transmitted between start and stop conditions is not limited. When the last word transfers, the master generates a stop condition to release the bus. Figure 18 shows a generic data-transfer sequence.

Use external pullup resistors for the SDA and SCL signals to set the logic-high level for the bus. Pullup resistors with values between 660 Ω and 4.7 kΩ are recommended. Do not allow the SDA and SCL voltages to exceed the DRV2665 supply voltage, V_{DD}.

The DRV2665 device operates as an I²C-slave with 1.8-V logic thresholds, but can operate up to the V_{DD} voltage.

NOTE

The slave address for the DRV2665 device is 0x59 (7-bit), or 1011001 in binary, which is equivalent to 0xB2 (8-bit) for writing and 0xB3 (8-bit) for reading.

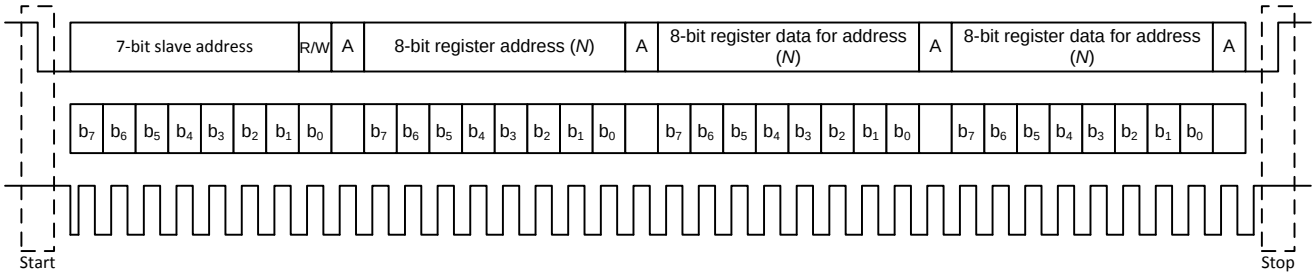

Figure 18. Typical I²C Sequence

7.5.3.2 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read-write operations for all registers.

During multi-byte transactions, the register address provided serves as the starting address. Subsequent data transfers automatically increment the register address accessed until a stop condition is reached.

7.5.3.3 Single-Byte Write

As shown in Figure 19, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read-write bit. The read-write bit determines the direction of the data transfer. For a write-data transfer, the read-write bit must be set to 0. After receiving the correct I²C device address and the read-write bit, the DRV2665 device responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the DRV2665 internal-memory address that is accessed. After receiving the register byte, the device responds again with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

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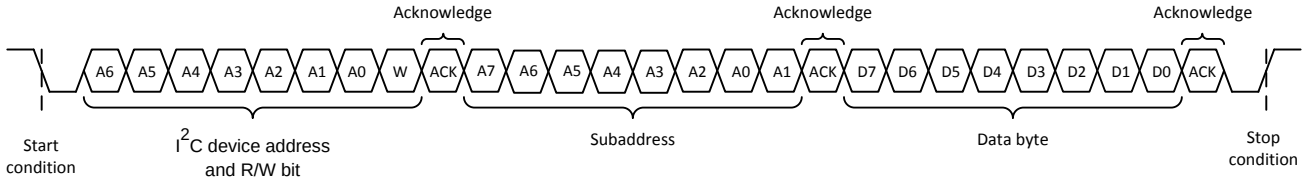

Figure 19. Single-Byte Write Transfer

7.5.3.4 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DRV2665 device. After receiving each data byte, the DRV2665 device responds with an acknowledge bit as shown in Figure 20.

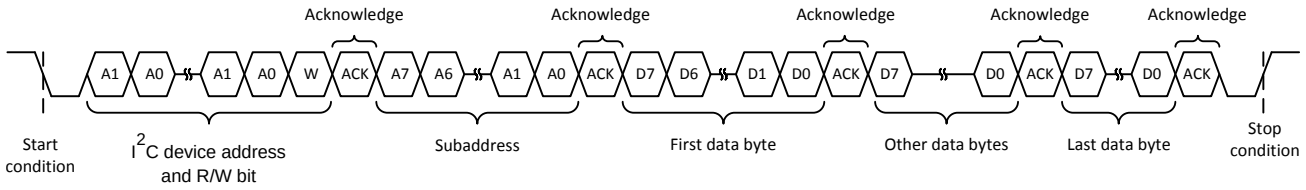

Figure 20. Multiple-Byte Write Transfer

7.5.3.5 Single-Byte Read

Figure 21 shows that a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read-write bit. For the data-read transfer, both a write followed by a read actually occur. Initially, a write occurs to transfer the address byte of the internal memory address to be read. As a result, the read-write bit is set to 0.

After receiving the DRV2665 address and the read-write bit, the DRV2665 device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the DRV2665 address and the read-write bit again. This time, the read-write bit is set to 1, indicating a read transfer. Next, the DRV2665 device transmits the data byte from the memory address that is read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer. See the note in the *General I^{2}C Operation* section for the device address.

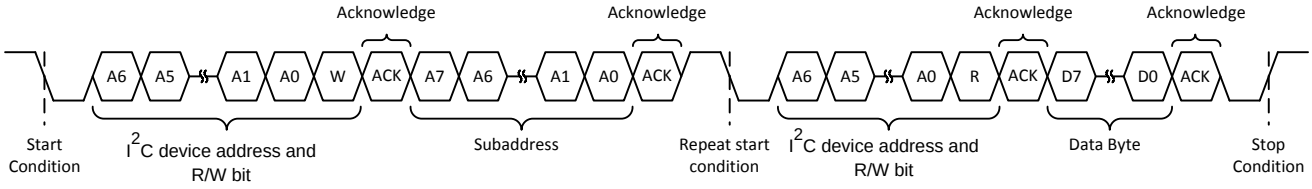

Figure 21. Single-Byte Read Transfer

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7.5.3.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the DRV2665 device to the master device as shown in Figure 22. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

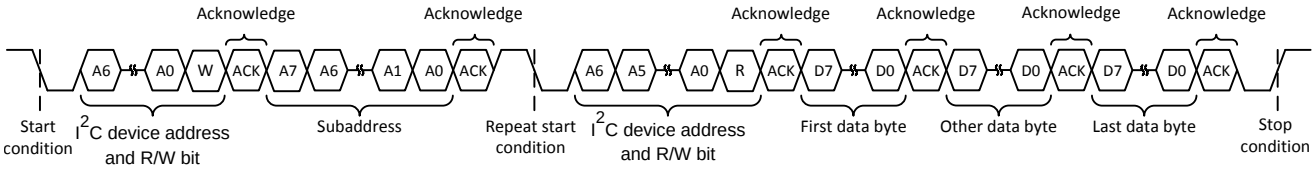

Figure 22. Multiple-Byte Read Transfer

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7.6 Register Map

Register Map Overview

REG NO.	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	0x02	Reserved						FIFO_EMPTY	FIFO_FULL
0x01	0x28	Reserved	CHIPID[3:0]				INPUT_MUX	GAIN[1:0]	
0x02	0x40	DEV_RST	STANDBY	Reserved		TIMEOUT[1:0]		EN_OVERRIDE	Reserved
0x0B	0x00	FIFO[7:0]							

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7.6.1 Address: 0x00

Figure 23. 0x00

7	6	5	4	3	2	1	0
Reserved						FIFO_EMPTY[0]	FIFO_FULL[0]
						RO-1	RO-0

Table 3. Address: 0x00

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-2	Reserved			
1	FIFO_EMPTY	RO	1	Indicates that the internal 100-byte FIFO is empty.
				0 FIFO is not empty.
				1 FIFO is empty.
0	FIFO_FULL	RO	0	Indicates that the internal100-byte FIFO is full and cannot accept data until another byte has played through the internal DAC.
				0 FIFO is not full.
				1 FIFO is full.

7.6.2 Address: 0x01

Figure 24. 0x01

7	6	5	4	3	2	1	0
Reserved	CHIPID[3:0]				INPUT_MUX[0]	GAIN[1:0]	
	RO-0	RO-1	RO-0	RO-1	R/W-0	R/W-0	R/W-0

Table 4. Address: 0x01

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	Reserved			
6-3	CHIPID[3:0]	RO	5	Identifies the device.
				0 DRV2660
				7 DRV2667
2	INPUT_MUX	R/W	0	Selects the source to be played.
				0 Digital input source
				1 Analog input source
1-0	GAIN[1:0]	R/W	0	Selects the gain for the amplifier.
				0 25 V (Digital) - 28.8 dB (Analog)
				1 50 V (Digital) - 34.8 dB (Analog)
				2 75 V (Digital) - 38.4 dB (Analog)
				3 100 V (Digital) - 40.7 dB (Analog)

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7.6.3 Address: 0x02

Figure 25. 0x02

7	6	5	4	3	2	1	0
DEV_RST[0]	STANDBY[0]	Reserved		TIMEOUT[1:0]		EN_OVERRIDE[0]	Reserved
R/W-0	R/W-1			R/W-0	R/W-0	R/W-0	

Table 5. Address: 0x02

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	DEV_RST	R/W	0	When asserted, the device will immediately stop any transaction in process, reset all of its internal register to their default values, and enters standby mode.
				0 Normal operation
				1 Reset device
6	STANDBY	R/W	1	Low-power standby
				0 Device is active and ready to receive a signal.
				1 Device is in low power standby mode.
5-4	Reserved			
3-2	TIMEOUT[1:0]	R/W	0	Time period when the FIFO runs empty and the device goes into idle mode, powering down the boost converter and amplifier.
				0 5 ms
				1 10 ms
				2 15 ms
				3 20 ms
1	EN_OVERRIDE	R/W	0	Override bit for the boost converter and amplifier enables.
				0 Boost converter and amplifier enables are controlled by device logic.
				1 Boost converter and amplifier are enabled indefinitely.
0--1	Reserved			

7.6.4 Address: 0x0B

Figure 26. 0x0B

7	6	5	4	3	2	1	0
FIFO[7:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 6. Address: 0x0B

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-0	FIFO[7:0]	R/W	0	Entry point for FIFO data. The user repeatedly writes this register with continuous haptic waveform data.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical application for a haptic driver is in a touch-enabled system that already has an application processor that makes the decision on when to execute haptic effects.

The DRV2665 device is configured and can be used fully with I^2C communication to stream or launch haptic effects. Additionally, the system designer may decide to use the analog input to stream the desired haptic effects.

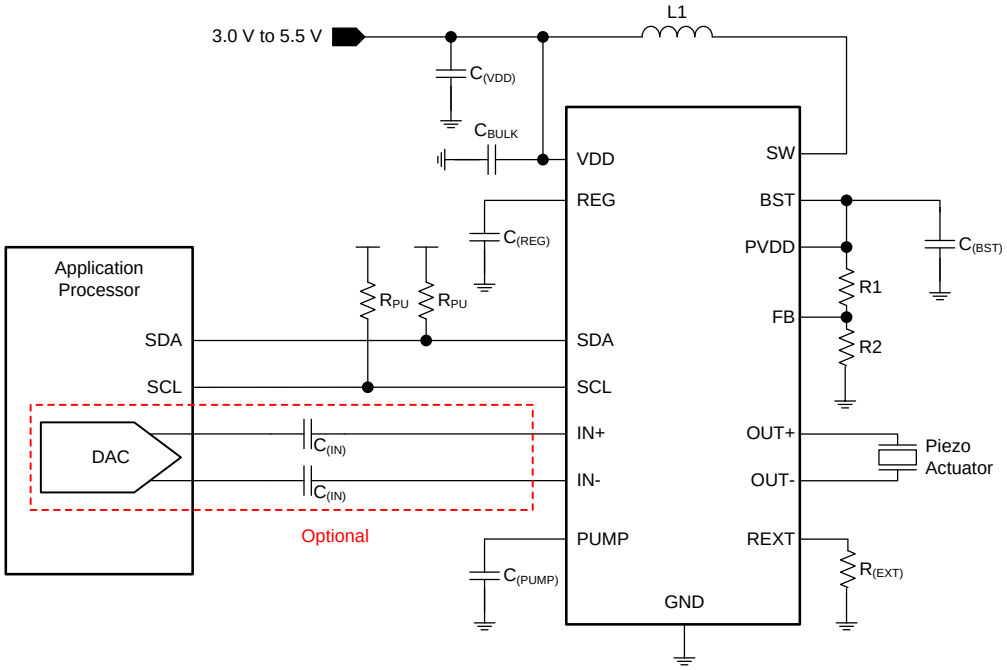

Figure 27. Typical Application Configuration

Table 7. Recommended External Components

COMPONENT	DESCRIPTION	SPECIFICATION	TYPICAL VALUE
$C_{(VDD)}$	Input capacitor	Capacitance	1 µF
$C_{(REG)}$	Regulator capacitor	Capacitance	0.1 µF
$C_{(BST)}$	Boost capacitor	Capacitance	0.1 µF
C_{BULK}	Bulk capacitor	Capacitance	10 µF
$C_{(PUMP)}$	Internal charge pump capacitor	Capacitance	0.1 µF
$C_{(IN)}$	AC coupling capacitor (optional)	Capacitance	1 µF
R_1	Boost feedback resistor (see *Programming the Boost Voltage*)	Resistance	768 kΩ
R_2	Boost feedback resistor (see *Programming the Boost Voltage*)	Resistance	9.76 kΩ
R_2	Current limit resistor (see *Programming the Boost Current Limit*)	Resistance	13 kΩ

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Application Information (continued)

Table 7. Recommended External Components (continued)

COMPONENT	DESCRIPTION	SPECIFICATION	TYPICAL VALUE
$R_{(PU)}$	Pullup resistor	Resistance	2.2 kΩ
L_1	Boost inductor	Inductance	3.3 µH

8.2 Typical Application

A typical application of the DRV2665 device is in a system that has external buttons which fire different haptic effects when pressed. Figure 28 shows a typical schematic of such a system. The buttons can be physical buttons, capacitive-touch buttons, or GPIO signals coming from the touch-screen system.

Effects in this type of system are programmable.

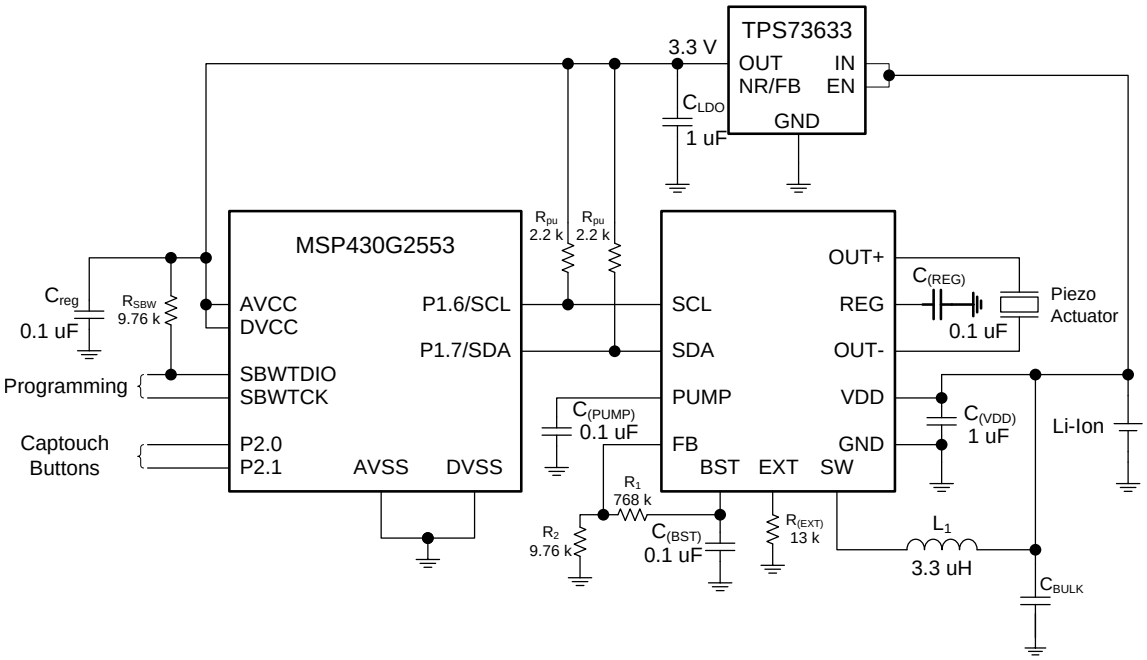

Figure 28. Example Application Schematic

8.2.1 Design Requirements

For this design example, use the values listed in Table 8 as the input parameters.

Table 8. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Actuator type	120 V_{PP}
Input power source	Li-ion / Li-polymer

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8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

Inductor selection plays a critical role in the performance of the DRV2665 device. The range of recommended inductances is from 3.3 µF to 22 µF. In general, higher inductances within an inductor series of a given manufacturer have lower saturation current limits, and vice-versa. When a larger inductance is chosen, the device boost converter automatically runs at a lower switching frequency and incurs less switching losses; however, larger values of inductance may have higher equivalent series resistance (ESR), that increases the parasitic inductor losses. Because lower values of inductance generally have higher saturation currents, they are a better choice when attempting to maximize the output current of the boost converter. Ensure that the saturation current of the inductor selected is higher than the programmed current limit for the device.

8.2.2.2 Piezo Actuator Selection

There are several key specifications to consider when choosing a piezo actuator for haptics, such as dimensions, blocking force, and displacement. However, the key electrical specifications from the driver perspective are voltage rating and capacitance.

At the maximum frequency of 500 Hz, the device is optimized to drive up to 50 nF at 200 V_{PP}, that is the highest voltage swing capability. It drives larger capacitances if the programmed boost voltage is lowered and/or the user limits the input frequency range to lower frequencies (e.g. 300 Hz).

8.2.2.3 Boost Capacitor Selection

The boost output voltage may be programmed as high as 105 V. A capacitor with a voltage rating of at least the boost output voltage must be selected. A 250-V rated 100-nF capacitor of the X5R or X7R type is recommended for the 105 V case because ceramic capacitors tend to come in ratings of 100 V or 250 V. The selected boost capacitor must have a minimum working capacitance of at least 50 nF. For boost voltages from 30 V to 80 V, a 100-V rated or 250-V rated, 100-nF capacitor is acceptable. For boost voltages less than 30 V, a 50-V, 0.22-µF capacitor is recommended.

8.2.2.4 Bulk Capacitor Selection

The use of a bulk capacitor placed next to the inductor is recommended due to the switch pin current requirements. A ceramic capacitors of the X5R or X7R type with capacitance of at least 1 µF is recommended.

8.2.3 Application Curves

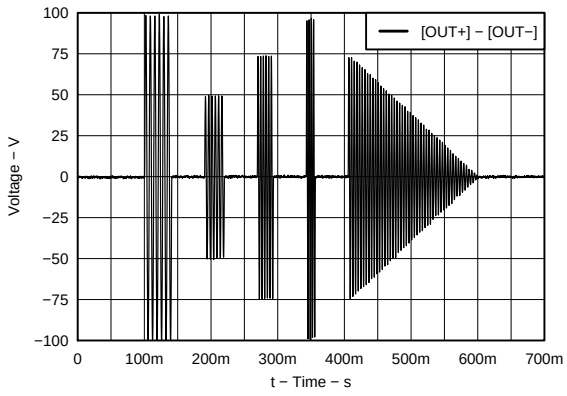

Figure 29. Example Waveform – Pinball Effect

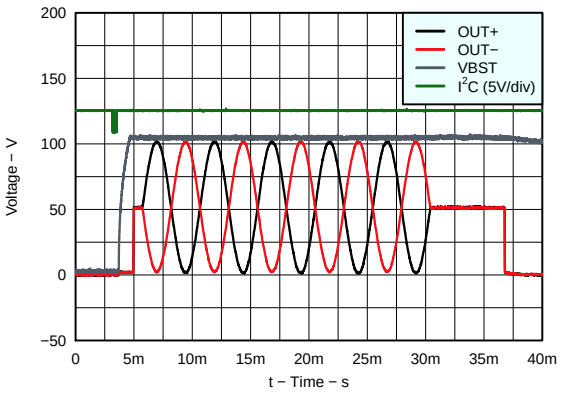

Figure 30. Typical Waveform

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8.3 Initialization Setup

The DRV2665 device features a simple initialization procedure:

8.3.1 Initialization Procedure

1. Apply power to the DRV2665 device.
2. Wait for 1 ms for the DRV2665 device to power-up before attempting an I^2C write.
3. Exit low-power standby mode by clearing the STANDBY bit in register 0x02, bit 6.
4. Choose the interface mode as analog or digital in register 0x01, bit 2.
5. Select the gain setting for your application in register 0x01, bits [1:0].
6. Choose the desired timeout period in register 0x02, bits[3:2].
7. If using the digital interface mode, the device is now ready to receive data. If using the analog input mode, set the EN_OVERRIDE bit in register 0x02, bit 1 to enable the boost and high-voltage amplifier and begin sourcing the waveform to the analog input.

9 Power Supply Recommendations

The DRV2665 device is designed to operate from an input-voltage supply range between 3 V and 5.5 V. The decoupling capacitor for the power supply must be placed as close to the device pin as possible.

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10 Layout

10.1 Layout Guidelines

Use the following guidelines for the DRV2665 device layout:

- The decoupling capacitor for the power supply (V_{DD}) must be placed close to the device pin.
- The filtering capacitor for the regulator (REG) must be placed close to the device pin.
- The boost inductor must be placed as close as possible to the SW pin.
- The bulk capacitor for the boost must be placed as close as possible to the inductor.
- The charge pump capacitor (PUMP) must be placed close to the device pin.

Use of the thermal footprint outlined by this datasheet is recommended to achieve optimum device performance. See land pattern diagram for exact dimensions.

The DRV2665 device power pad must be soldered directly to the thermal pad on the printed circuit board. The printed circuit board thermal pad must be connected to the ground net and thermal vias to any existing backside/internal copper ground planes. Connection to a ground plane on the top layer near the corners of the device is also recommended. Another key layout consideration is to keep the boost programming resistors (R1 and R2) as close as possible to the FB pin of the device. Care must be taken to avoid getting the FB trace near the SW trace.

10.2 Layout Example

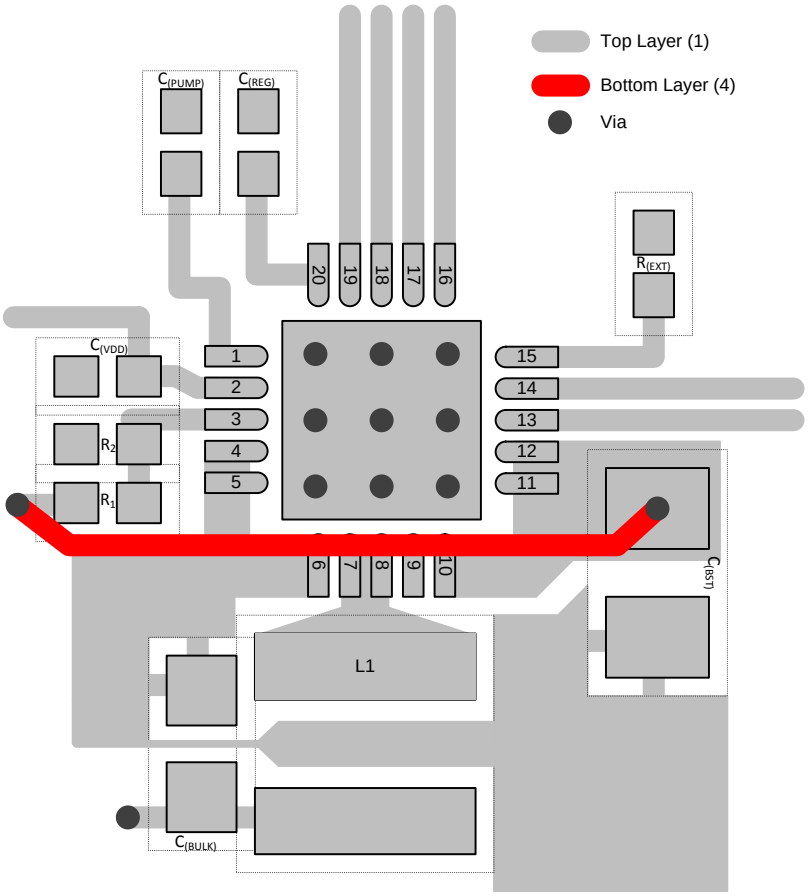

Figure 31. Layout Example with a 4-Layer Board

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11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV2665RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 70	2665	Samples
DRV2665RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 70	2665	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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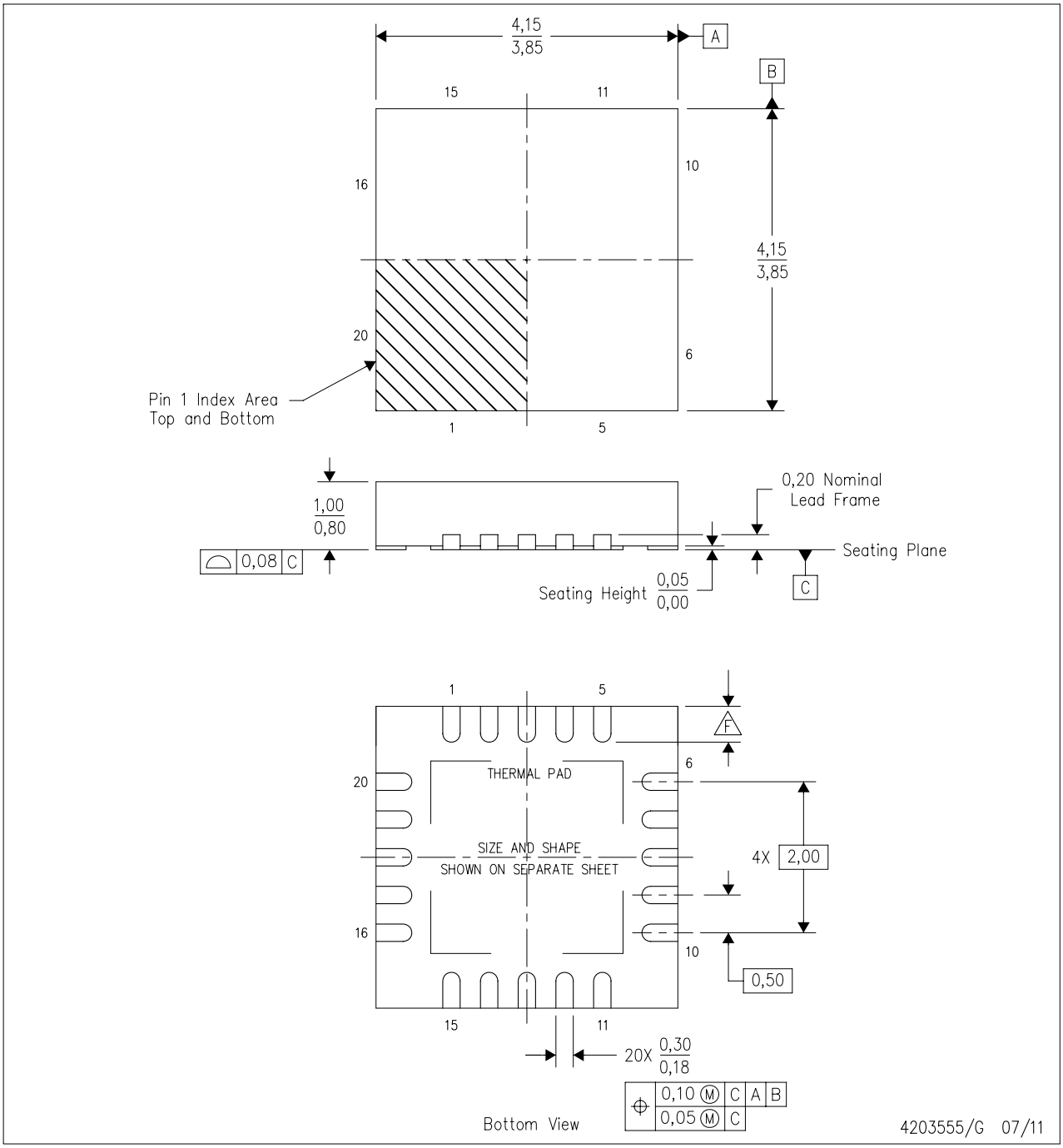
MECHANICAL DATA

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

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THERMAL PAD MECHANICAL DATA

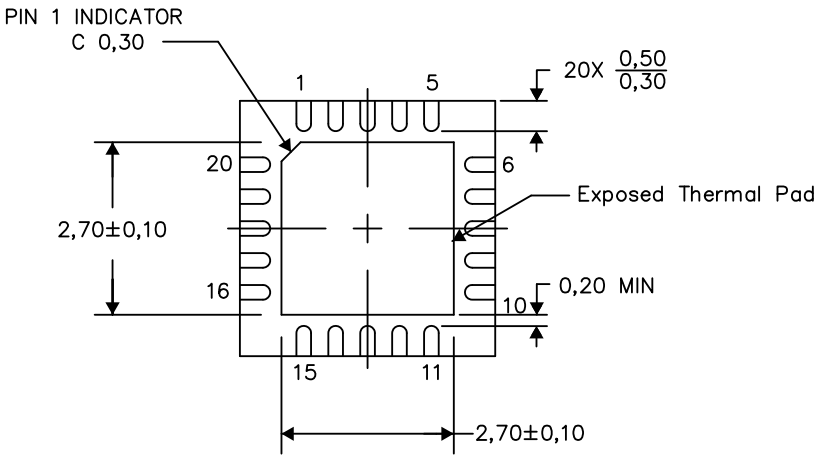
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

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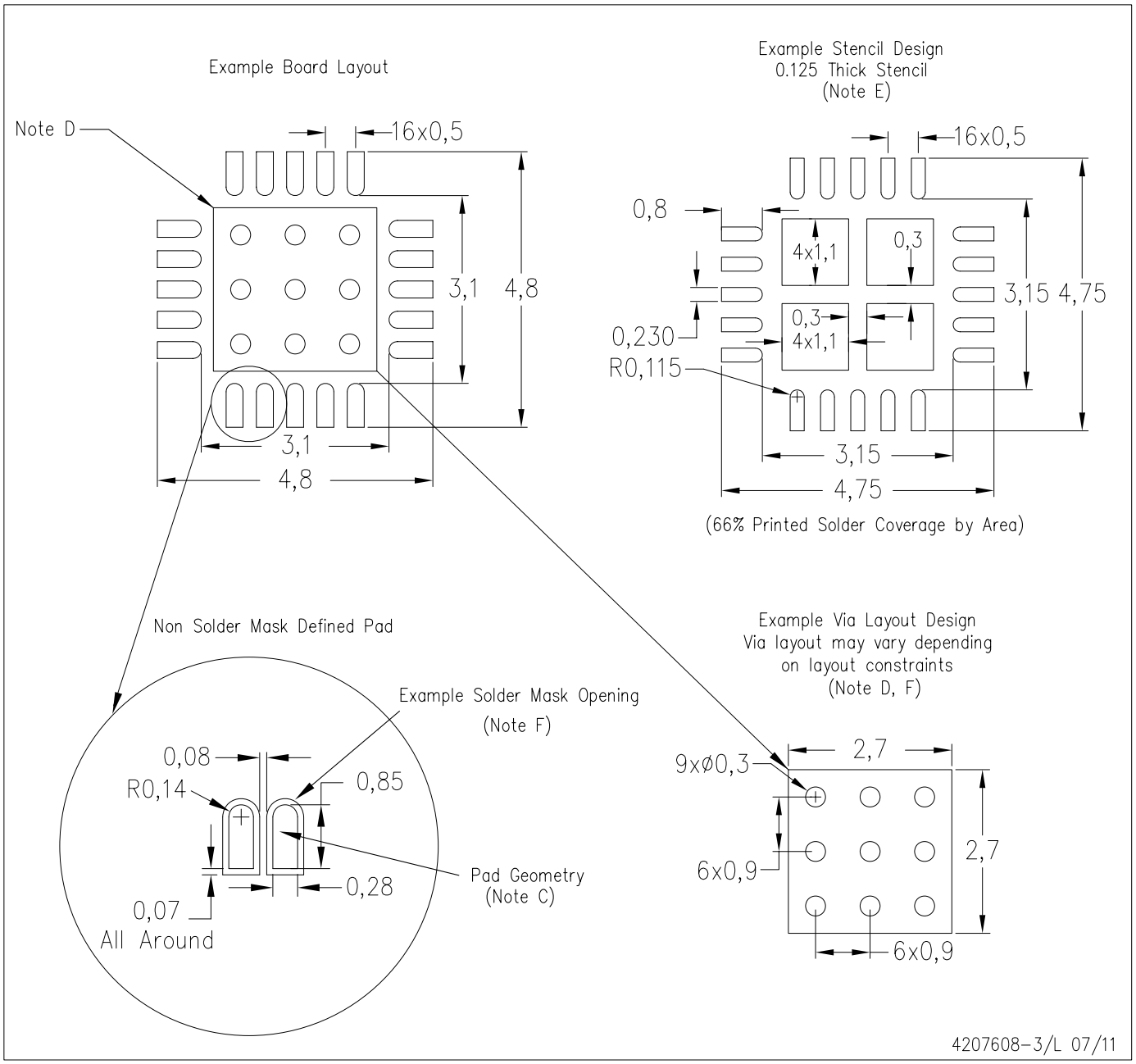
RGP (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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