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[SIHF10N40D-E3](#)

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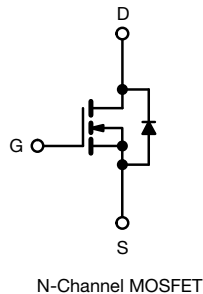
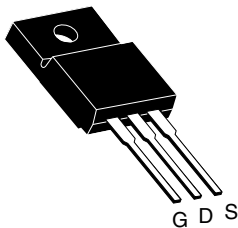
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**SiHF10N40D**  
 Vishay Siliconix

## D Series Power MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V) at T <sub>J</sub> max.	450
R <sub>DS(on)</sub> max. (Ω) at 25 °C	V <sub>GS</sub> = 10 V   0.6
Q <sub>g</sub> max. (nC)	30
Q <sub>gs</sub> (nC)	4
Q <sub>gd</sub> (nC)	7
Configuration	Single

TO-220 FULLPAK



### FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance (C<sub>iss</sub>)
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): R<sub>on</sub> x Q<sub>g</sub>
  - Fast switching
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS\*  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

### APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- Battery chargers

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF10N40D-E3


ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	400	V
Gate-Source Voltage	V <sub>GS</sub>	± 30	
Gate-Source Voltage AC (f > 1 Hz)		30	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>e</sup>	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	10
		T <sub>C</sub> = 100 °C	6
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	23	A
Linear Derating Factor		0.26	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	194	mJ
Maximum Power Dissipation	P <sub>D</sub>	33	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	T <sub>J</sub> = 125 °C	24
Reverse Diode dV/dt <sup>d</sup>		0.6	
Soldering Recommendations (Peak temperature) <sup>c</sup>	for 10 s	300	°C

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 2.3 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 13 A.
- 1.6 mm from case.
- I<sub>SD</sub> ≤ I<sub>D</sub>, starting T<sub>J</sub> = 25 °C.
- Limited by maximum junction temperature.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.8	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		400	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 250\text{ }\mu\text{A}$		-	0.53	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3	-	5	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 5\text{ A}$	-	0.5	0.6	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 5\text{ A}$		-	2.7	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$		-	526	-	pF
Output Capacitance	$C_{oss}$			-	59	-	
Reverse Transfer Capacitance	$C_{rss}$			-	9	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 320\text{ V}$		-	66	-	pF
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$			-	84	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 5\text{ A}, V_{DS} = 320\text{ V}$	-	15	30	nC
Gate-Source Charge	$Q_{gs}$			-	4	-	
Gate-Drain Charge	$Q_{gd}$			-	7	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 10\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	12	24	ns
Rise Time	$t_r$			-	18	36	
Turn-Off Delay Time	$t_{d(off)}$			-	18	36	
Fall Time	$t_f$			-	14	28	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$		0.9	1.8	3.6	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	10	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	40	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 5\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	230	-	ns
Reverse Recovery Charge	$Q_{rr}$			-	1.6	-	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	14	-	A

**Notes**

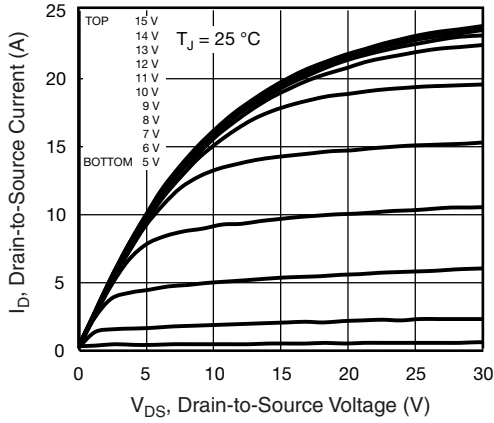
- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .  
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .



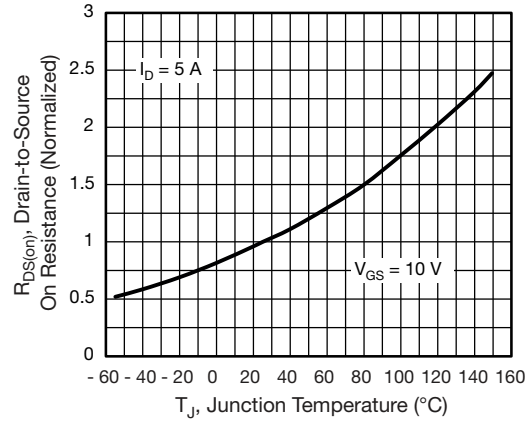
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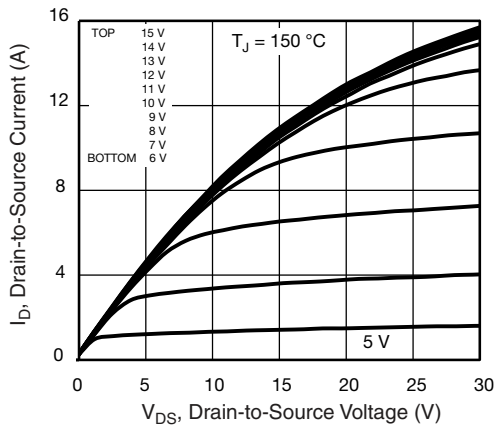
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



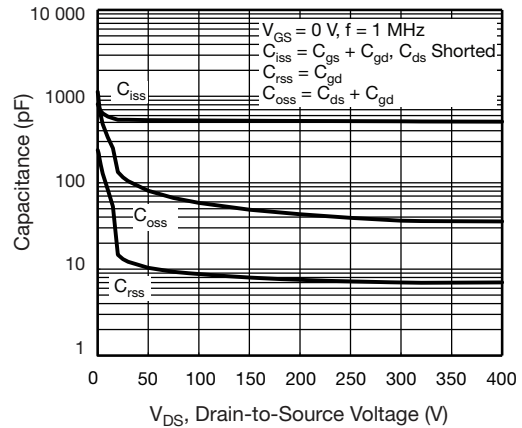
**Fig. 1 - Typical Output Characteristics**



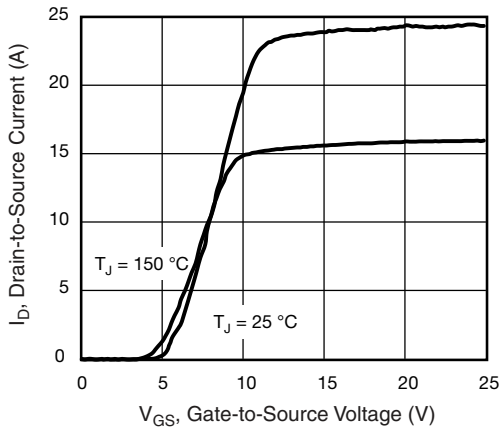
**Fig. 4 - Normalized On-Resistance vs. Temperature**



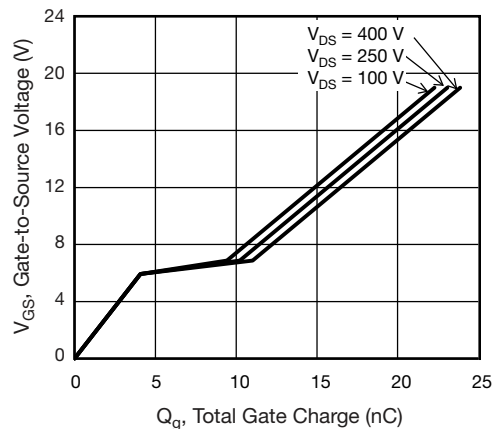
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



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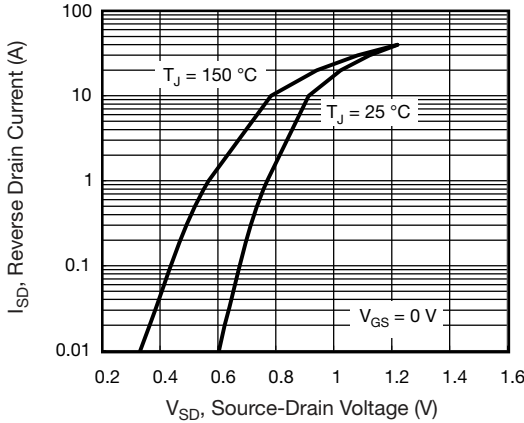


Fig. 7 - Typical Source-Drain Diode Forward Voltage

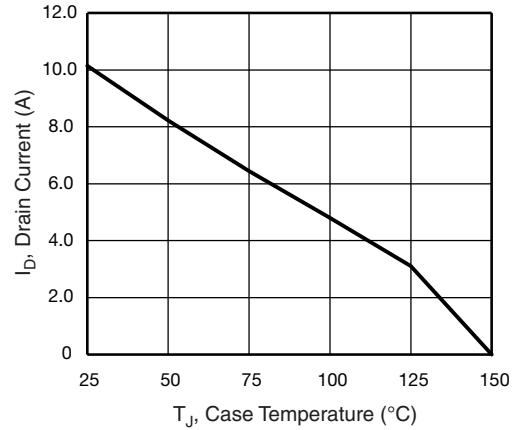


Fig. 9 - Maximum Drain Current vs. Case Temperature

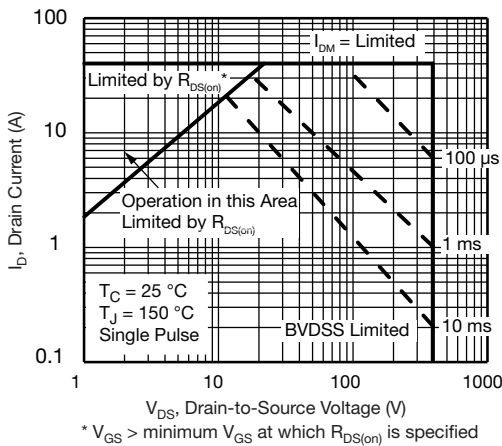


Fig. 8 - Maximum Safe Operating Area

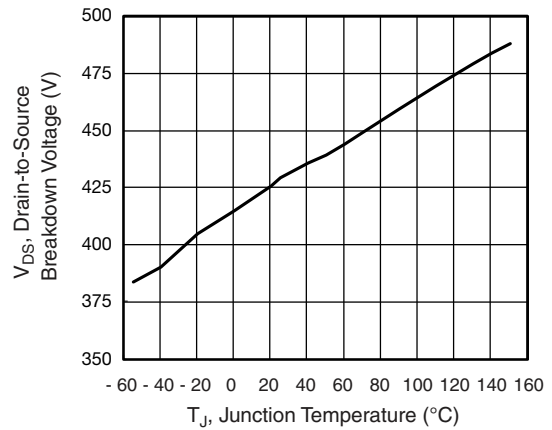


Fig. 10 - Temperature vs. Drain-to-Source Voltage

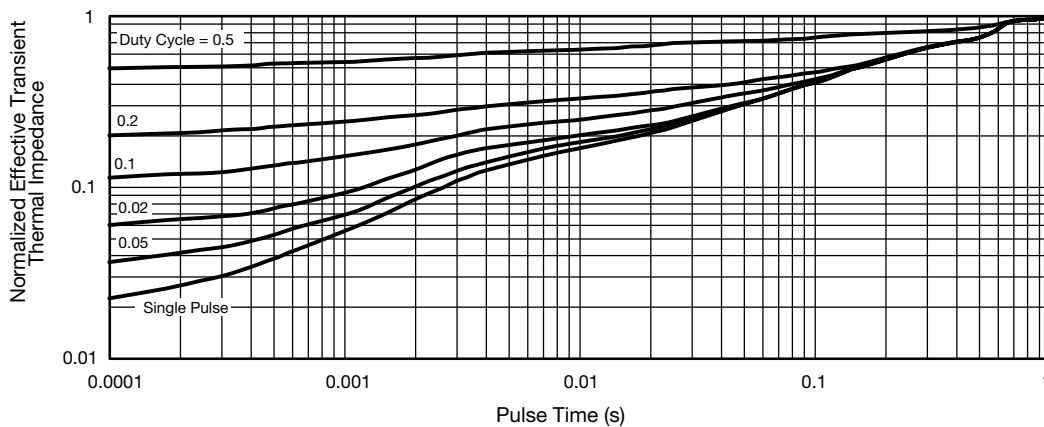
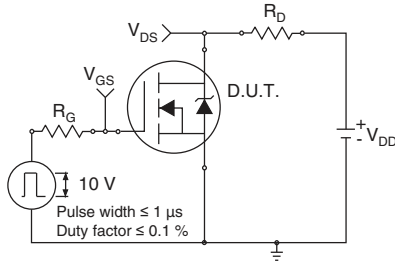


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

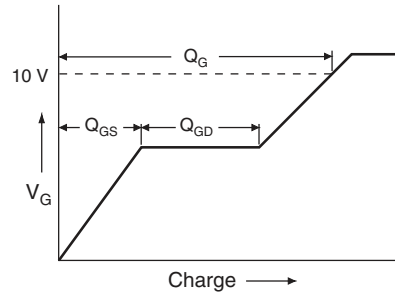


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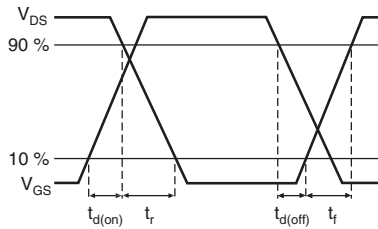
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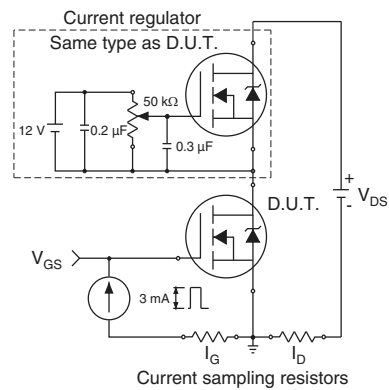
**Fig. 12 - Switching Time Test Circuit**



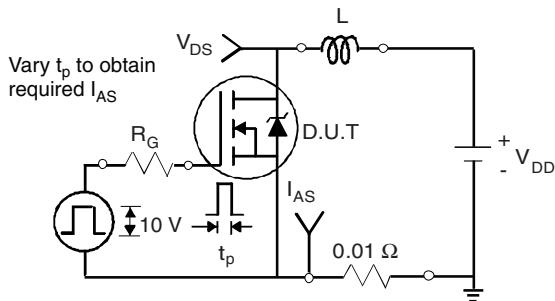
**Fig. 16 - Basic Gate Charge Waveform**



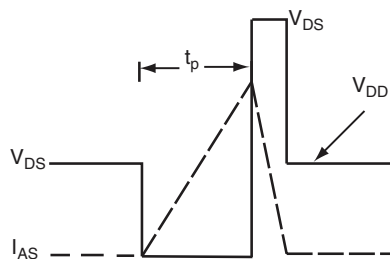
**Fig. 13 - Switching Time Waveforms**



**Fig. 17 - Gate Charge Test Circuit**

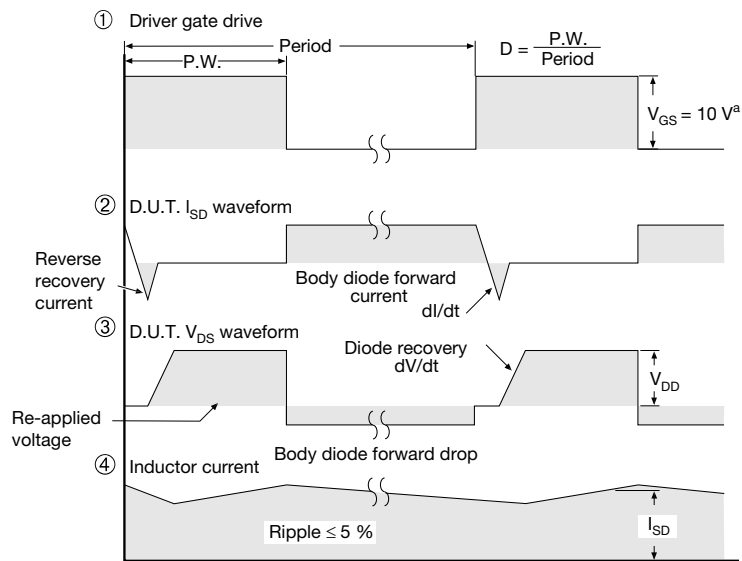
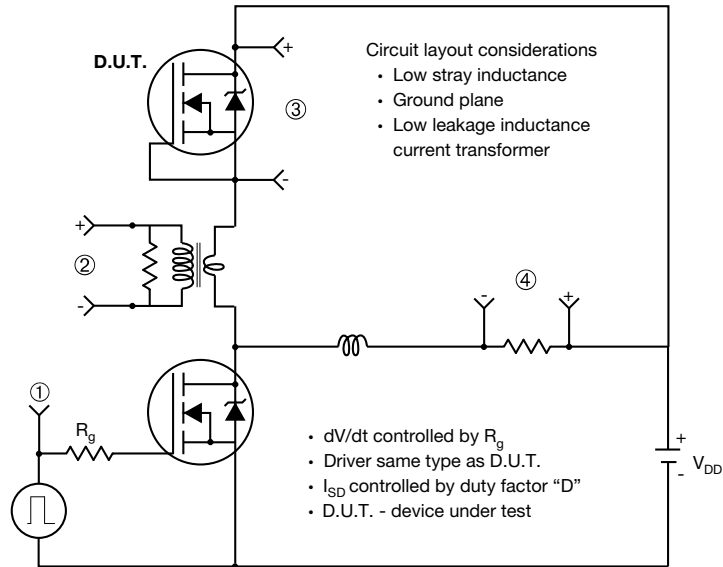


**Fig. 14 - Unclamped Inductive Test Circuit**



**Fig. 15 - Unclamped Inductive Waveforms**

**Peak Diode Recovery dV/dt Test Circuit**



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 18 - For N-Channel**

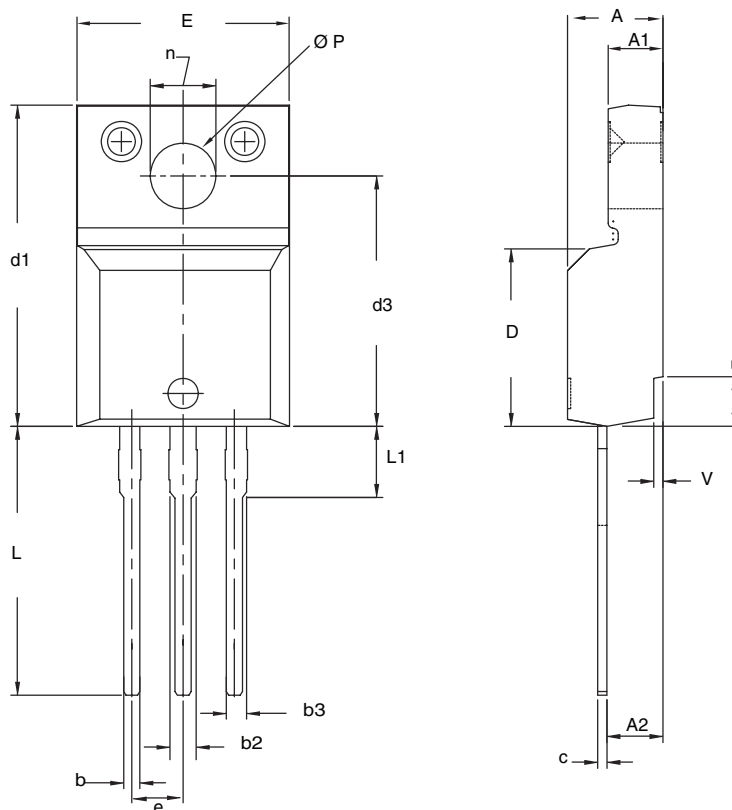
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## Package Information

Vishay Siliconix

### TO-220 FULLPAK (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
DWG: 5972

#### Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.





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