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Diodes Incorporated DMP2039UFDE4-7

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Datasheet of DMP2039UFDE4-7 - MOSFET P-CH 25V 7.3A 6DFN

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# DMP2039UFDE4

## 25V P-CHANNEL ENHANCEMENT MODE MOSFET

# **Product Summary**

V <sub>(BR)DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub> T <sub>A</sub> = 25°C
-25V	$26m\Omega$ @ $V_{GS} = -4.5V$	-7.3
-25V	40m $Ω$ @ V <sub>GS</sub> = -1.8V	-6.0

# **Description and Applications**

This new generation MOSFET has been designed to minimize the onstate resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Load Switching
- Battery Management Application
- Power Management Functions

## **Features and Benefits**

- Low R<sub>DS(ON)</sub> ensures on state losses are minimized
- 0.4mm profile ideal for low profile applications
- PCB footprint of 4mm<sup>2</sup>
- Low Input Capacitance
- ESD Protected Gate
- Lead, Halogen, and Antimony Free, RoHS Compliant (Note 1)
- "Green" Device (Note 2)
- Qualified to AEC-Q101 Standards for High Reliability

## **Mechanical Data**

- Case: X2-DFN2020-6
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.006 grams (approximate)

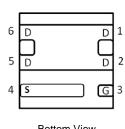
## X2-DFN2020-6

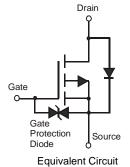




**Bottom View** 







Bottom View Internal Schematic

# Ordering Information (Note 3)

Part Number	Case	Packaging	
DMP2039UFDE4-7	X2-DFN2020-6	3,000/Tape & Reel	

Notes:

- 1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. No purposely added lead. Halogen and Antimony free.
- 2. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com.
- 3. For packaging details, go to our website at http://www.diodes.com.

## **Marking Information**



PD = Product Type Marking Code YM = Date Code Marking Y = Year (ex: Y = 2011) M = Month (ex: 9 = September) Dot Denotes Pin 1

## Date Code Key

Year	201	1	2012		2013	20	14	2015		2016	2	2017
Code	Υ		Z		Α		3	С		D		E
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	4	2	2	1		6	7	0	0		N	7

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DMP2039UFDE4

# Maximum Ratings @TA = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units		
Drain-Source Voltage			$V_{DSS}$	-25	V
Gate-Source Voltage			V <sub>GSS</sub>	±8	V
Continuous Durin Courset (Nata 5) V	Steady State	$T_A = 25$ °C $T_A = 70$ °C	I <sub>D</sub>	-7.3 -5.8	А
Continuous Drain Current (Note 5) V <sub>GS</sub> = -4.5V	t<5s	T <sub>A</sub> = 25°C T <sub>A</sub> = 70°C	I <sub>D</sub>	-9.2 -7.3	А
Continuous Dusin Courset (Note 5) \/ 4.0\/	Steady State	T <sub>A</sub> = 25°C T <sub>A</sub> = 70°C	I <sub>D</sub>	-6.0 -4.7	А
Continuous Drain Current (Note 5) V <sub>GS</sub> = -1.8V	t<5s	$T_A = 25$ °C $T_A = 70$ °C	I <sub>D</sub>	-7.6 -6.0	А
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I <sub>DM</sub>	-60	Α		
Continuous Source-Drain Diode Current	I <sub>S</sub>	-2.0	Α		

# Thermal Characteristics @TA = 25°C unless otherwise specified

Characteristic		Symbol	Value	Units	
Total Power Dissipation (Note 4)	T <sub>A</sub> = 25°C	Р	0.69	W	
Total Power Dissipation (Note 4)	T <sub>A</sub> = 70°C	$P_{D}$	0.44	VV	
Thermal Resistance, Junction to Ambient (Note 4)	Steady state	р	182	°C/W	
Thermal Resistance, Junction to Ambient (Note 4)	t<5s	$R_{\theta JA}$	113		
Total Power Dissipation (Note 5)	$T_A = 25^{\circ}C$	D	2.4	W	
Total Fower Dissipation (Note 5)	T <sub>A</sub> = 70°C	$P_{D}$	1.5		
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	D	52	°C/W	
Thermal Resistance, Junction to Ambient (Note 5)	t<5s	$R_{ hetaJA}$	33	C/VV	
Thermal Resistance, Junction to Case (Note 5)	Steady state	$R_{ heta JC}$	9.1	°C/W	
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C	

# **Electrical Characteristics** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition		
OFF CHARACTERISTICS (Note 6)								
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-25	_	_	V	$V_{GS} = 0V, I_D = -250\mu A$		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		_	-1	μΑ	$V_{DS} = -25V, V_{GS} = 0V$		
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±10	μΑ	$V_{GS} = \pm 8.0 V, V_{DS} = 0 V$		
ON CHARACTERISTICS (Note 6)								
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.4	_	-1.0	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$		
			19	26		$V_{GS} = -4.5V, I_D = -6.4A$		
Static Drain-Source On-Resistance	_	_	24	33	0	$V_{GS} = -2.5V, I_D = -4.8A$		
Static Drain-Source On-Resistance	R <sub>DS</sub> (ON)	_	29	40	mΩ	$V_{GS} = -1.8V, I_D = -2.5A$		
		_	35	70		$V_{GS} = -1.5V, I_D = -1.5A$		
Forward Transfer Admittance	Y <sub>fs</sub>	_	14	_	mS	$V_{DS} = -5V, I_{D} = -4A$		
Diode Forward Voltage (Note 5)	$V_{SD}$	_	-0.7	-1.0	V	$V_{GS} = 0V, I_{S} = -1A$		
DYNAMIC CHARACTERISTICS (Note 7)								
Input Capacitance	C <sub>iss</sub>		2530	_	pF	45)/ )/ 0)/		
Output Capacitance	Coss	1	203	_	pF	$V_{DS} = -15V, V_{GS} = 0V$ - f = 1.0MHz		
Reverse Transfer Capacitance	C <sub>rss</sub>	_	177	_	pF	1 = 1.0MHZ		
Gate Resistance	Rq	_	9.1	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$		
Total Gate Charge	Qg	_	28.2	_				
Gate-Source Charge	Q <sub>qs</sub>	_	48.7	_	nC	$V_{DS} = -15V, I_{D} = -4.0A$		
Gate-Drain Charge	Q <sub>qd</sub>	_	3.2	_				
Turn-On Delay Time	t <sub>D(on)</sub>	_	5.0	_				
Turn-On Rise Time	t <sub>r</sub>	_	15.1	_	nS	$V_{DD} = -15V, V_{GS} = -4.5V, R_{G} = 1\Omega,$		
Turn-Off Delay Time	t <sub>D(off)</sub>	_	23.5	_	115	$I_D = -4.0A$		
Turn-Off Fall Time	t <sub>f</sub>	_	137.6					

Notes:

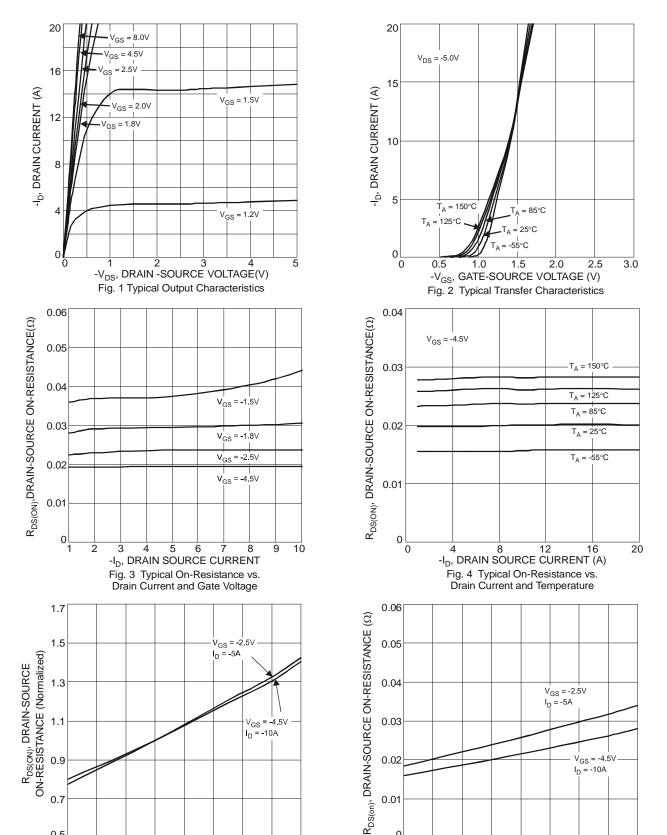
- 4. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
- 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate
- Short duration pulse test used to minimize self-heating effect
   Guaranteed by design. Not subject to production testing.

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# DMP2039UFDE4



25

50

T<sub>.I</sub>, JUNCTION TEMPERATURE (°C)

Fig. 5 On-Resistance Variation with Temperature

75

100

0.5

0 -50

25

50 75

T<sub>.I</sub>, JUNCTION TEMPERATURE (°C)

Fig. 6 On-Resistance Variation with Temperature

100 125

# **DIODES**

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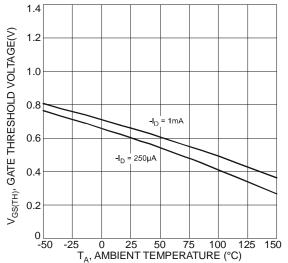
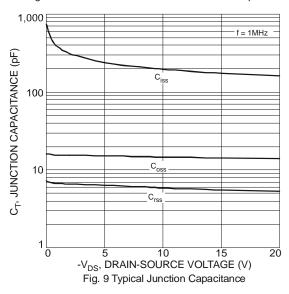
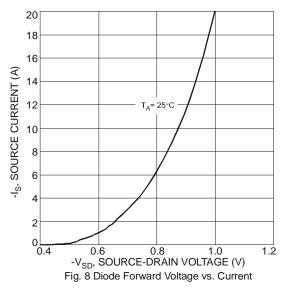


Fig. 7 Gate Threshold Variation vs. Ambient Temperature





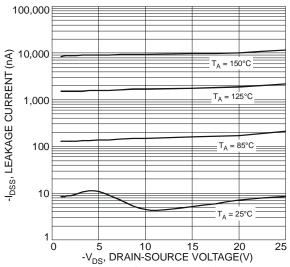
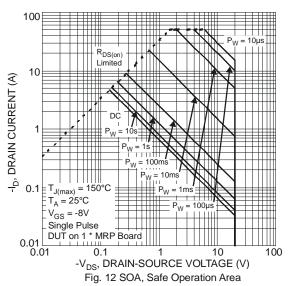


Fig. 10 Typical Drain-Source Leakage Current vs. Voltage

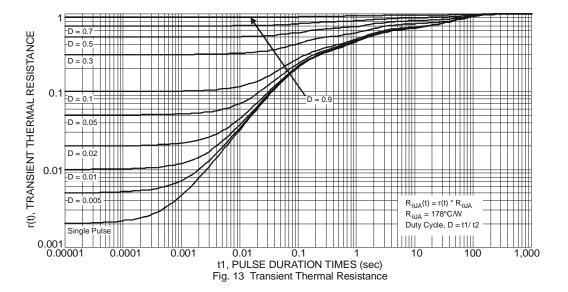


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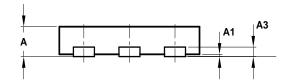
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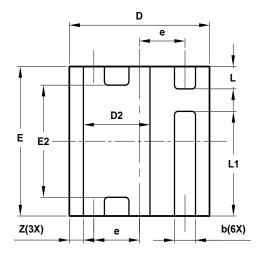


# DMP2039UFDE4



# **Package Outline Dimensions**





X2-DFN2020-6							
Dim	Dim Min Max						
Α	_	0.40	Тур _				
A1	0	0.05	0.03				
A3	-	_	0.13				
b	0.25	0.35	0.30				
D	1.95	2.05	2.00				
D2	0.85	1.05	0.95				
Е	1.95	2.05	2.00				
E2	1.40	1.60	1.50				
е	-	_	0.65				
L	0.25	0.35	0.30				
L1	1.35	1.45	1.40				
Z	-	-	0.20				
All	All Dimensions in mm						

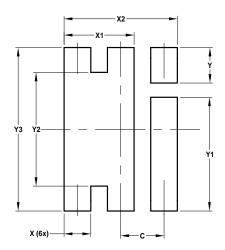
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## Suggested Pad Layout



Dimensions	Value (in mm)		
С	0.650		
Х	0.400		
X1	1.050		
X2	1.700		
Υ	0.500		
Y1	1.600		
Y2	1.600		
Y3	2.300		

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