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Texas Instruments
CDCS503TPWRQ1

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Clock Buffer/Clock Multiplier With Optional SSC

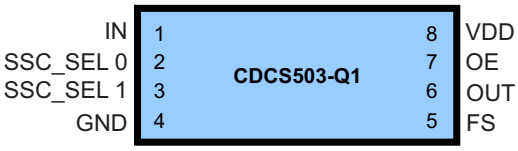
Check for Samples: CDCS503-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Test Guidance With the Following Results:**
  - **Device Temperature Grade 2**
  - **-40°C to 105°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **Part of a Family of Easy to Use Clock Generator Devices With Optional Spread Spectrum Clocking (SSC)**
- **Clock Multiplier With Selectable Output Frequency and Selectable SSC**
- **SSC Controllable Through Two External Pins**
  - **±0%, ±0.5%, ±1%, ±2% Center Spread**
- **Frequency Multiplication Selectable Between x1 or x4 With One External Control Pin**
- **Output Disable Through Control Pin**
- **Single 3.3 V Device Power Supply**
- **Wide Temperature Range –40°C to 105°C**
- **Low Space Consumption 8-Pin TSSOP Package**

APPLICATIONS

- **Automotive Applications Requiring EMI Reduction Through SSC and/or Clock Multiplication**



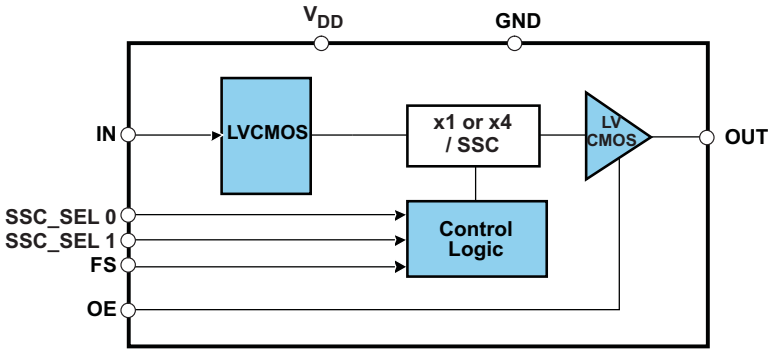


Figure 1. BLOCK DIAGRAM

DESCRIPTION

The CDCS503-Q1 device is a spread spectrum capable, LVCMOS input clock buffer with selectable frequency multiplication.

It shares major functionality with the CDCS502 but uses a LVCMOS input stage instead of the crystal input stage of the CDCS502, and the CDCS503-Q1 has an output enable pin.

The device accepts a 3.3-V LVCMOS signal at the input.

The input signal is processed by a phased-locked loop (PLL), whose output frequency is either equal to the input frequency or multiplied by the factor of four.

The PLL is also able to spread the clock signal by ±0%, ±0.5%, ±1% or ±2% centered around the output clock frequency with a triangular modulation.

By this, the device can generate output frequencies between 8 MHz and 108 MHz with or without SSC.

A separate control pin can be used to enable or disable the output. The CDCS503-Q1 device operates in a 3.3-V environment.

It is characterized for operation from –40°C to 105°C, and available in an 8-pin TSSOP package.

Table 1. FUNCTION TABLE

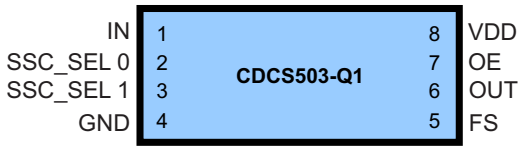
OE	FS	SSC_SEL 0	SSC_SEL 1	SSC AMOUNT	f_{OUT}/f_{IN}	f_{OUT} at f_{in} = 27 MHz
0	x	x	x	x	x	3-state
1	0	0	0	±0.00%	1	27 MHz
1	0	0	1	±0.50%	1	27 MHz
1	0	1	0	±1.00%	1	27 MHz
1	0	1	1	±2.00%	1	27 MHz
1	1	0	0	±0.00%	4	108 MHz
1	1	0	1	±0.50%	4	108 MHz
1	1	1	0	±1.00%	4	108 MHz
1	1	1	1	±2.00%	4	108 MHz

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

PACKAGE



PIN FUNCTIONS

SIGNAL	PIN	TYPE	DESCRIPTION
IN	1	I	LVCMOS clock input
OUT	6	O	LVCMOS clock output
SSC_SEL 0, 1	2, 3	I	Spread selection pins, internal pullup
OE	7	I	Output enable, internal pullup
FS	5	I	Frequency multiplication selection, internal pullup
VDD	8	Power	3.3-V power supply
GND	4	Ground	Ground

ORDERING INFORMATION

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	TSSOP	2000	CDCS503TPWRQ1	CS503Q

PACKAGE THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE

over operating free-air temperature range (unless otherwise noted)(1)

PW 8-PIN TSSOP			THERMAL AIRFLOW (CFM)				UNIT
			0	150	250	500	
$R_{\theta JA}$	High K		149	142	138	132	°C/W
	Low K		230	185	170	150	
$R_{\theta JC}$	High K	65					°C/W
	Low K	69					

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

THERMAL INFORMATION

THERMAL METRIC(1)		CDCS503TPWRQ1	UNIT
		PW (8 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	179.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	64.9	
θ_{JB}	Junction-to-board thermal resistance	108.7	
ψ_{JT}	Junction-to-top characterization parameter	9	
ψ_{JB}	Junction-to-board characterization parameter	107	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 4.6	V
V_{IN}	Input voltage range	–0.5 to 4.6	V
V_{out}	Output voltage range	–0.5 to 4.6	V
I_{IN}	Input current ($V_I < 0$, $V_I > V_{DD}$)	20	mA
I_{out}	Continuous output current	50	mA
T_{ST}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	125	°C
ESD Rating	Human-body model (HBM) AEC-Q100 classification level H2	1.5	kV
	Charged-device model (CDM) AEC-Q100 classification level C3B	750	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3		3.6	V
f_{IN}	Input frequency	FS = 0	8		32	MHz
		FS = 1	8		27	
V_{IL}	Low-level input voltage LVCMOS				0.3 V_{DD}	V
V_{IH}	High-level input voltage LVCMOS		0.7 V_{DD}			V
V_I	Input voltage threshold LVCMOS			0.5 V_{DD}		V
C_L	Output load test LVCMOS				15	pF
I_{OH}/I_{OL}	Output current				±12	mA
T_A	Operating free-air temperature		–40		105	°C

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Device supply current	f_{out} = 20 MHz; FS = 0, no SSC		19		mA
		f_{out} = 70 MHz; FS = 1, SSC = 2%		22		
f_{OUT}	Output frequency	FS = 0	8		32	MHz
		FS = 1	32		108	
I_{IH}	LVCMOS input current	$V_I = V_{DD}$; V_{DD} = 3.6 V			10	µA
I_{IL}	LVCMOS input current	V_I = 0 V; V_{DD} = 3.6 V			–10	µA
V_{OH}	LVCMOS high-level output voltage	I_{OH} = - 0.1 mA	2.9			V
		I_{OH} = - 8 mA	2.4			
		I_{OH} = - 12 mA	2.2			
V_{OL}	LVCMOS low-level output voltage	I_{OL} = 0.1 mA			0.1	V
		I_{OL} = 8 mA			0.5	
		I_{OL} = 12 mA			0.8	
I_{OZ}	High-impedance-state output current	OE = Low	–2		2	µA
$t_{JIT(C-C)}$	Cycle to cycle jitter(1)	f_{out} = 108 MHz; FS = 1, SSC = 1%, 10000 Cycles		110		ps
t_r/t_f	Rise and fall time(1)	20%–80%		0.75		ns
O_{dc}	Output duty cycle(2)		45%		55%	
f_{MOD}	Modulation frequency			30		kHz

(1) Measured with Test Load, see Figure 3.
(2) Not production tested.

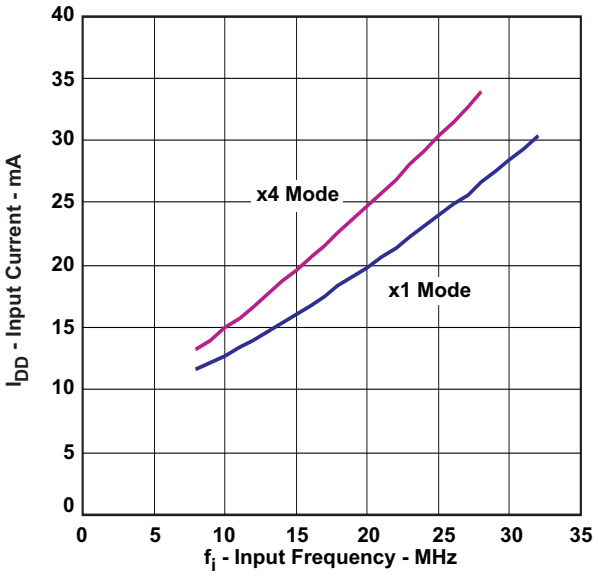


Figure 2. I_{DD} vs Input Frequency, V_{CC} = 3.3 V, SSC = 2%, Output Loaded With Test Load

APPLICATION INFORMATION

SSC MODULATION

The exact implementation of the SSC modulation plays a vital role for the EMI reduction. The CDCS503-Q1 device uses a triangular modulation scheme implemented in a way that the modulation frequency depends on the VCO frequency of the internal PLL and the spread amount is independent from the VCO frequency.

The modulation frequency can be calculated by using one of the below formulas chosen by frequency multiplication mode.

FS = 0: $f_{mod} = f_{IN} / 708$
FS = 1: $f_{mod} = f_{IN} / 620$

PARAMETER MEASUREMENT INFORMATION

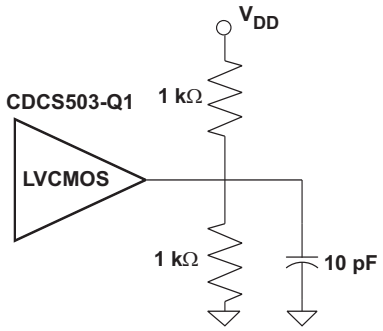


Figure 3. Test Load

PARAMETER MEASUREMENT INFORMATION (continued)

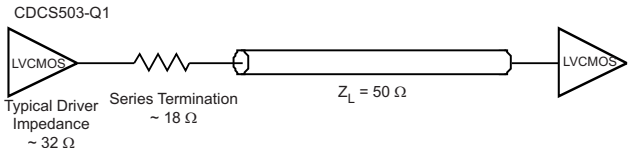


Figure 4. Load for 50-Ω Board Environment

REVISION HISTORY

Changes from Revision A (June 2012) to Revision B	Page
• Changed AEC Q100 Qualified to AEC Q100 Test Guidance in FAD.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCS503TPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	CS503Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF CDCS503-Q1 :

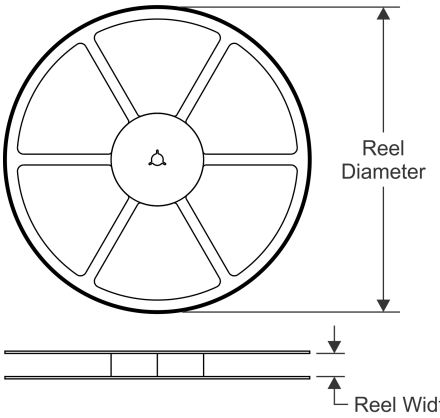
- Catalog: CDCS503

NOTE: Qualified Version Definitions:

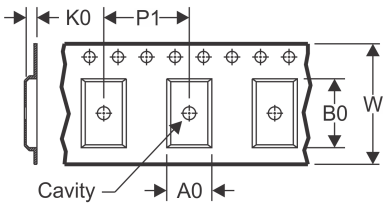
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

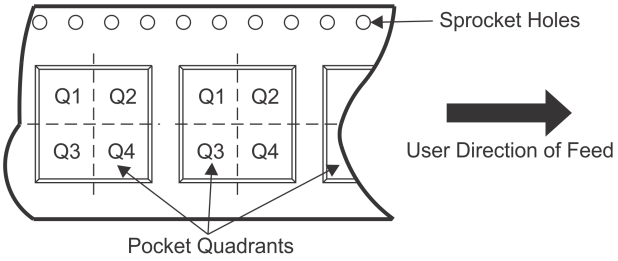


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

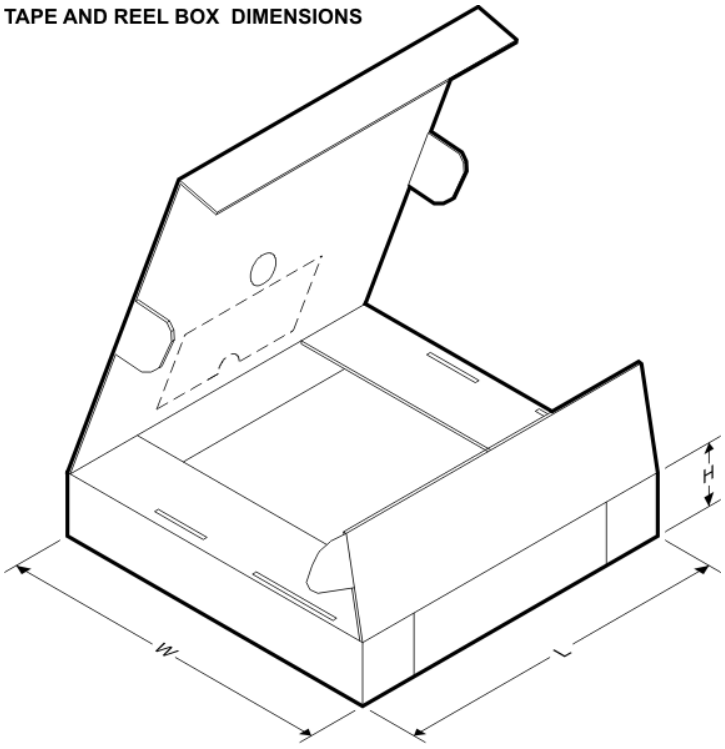


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCS503TPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

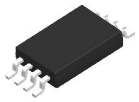
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCS503TPWRQ1	TSSOP	PW	8	2000	367.0	367.0	35.0

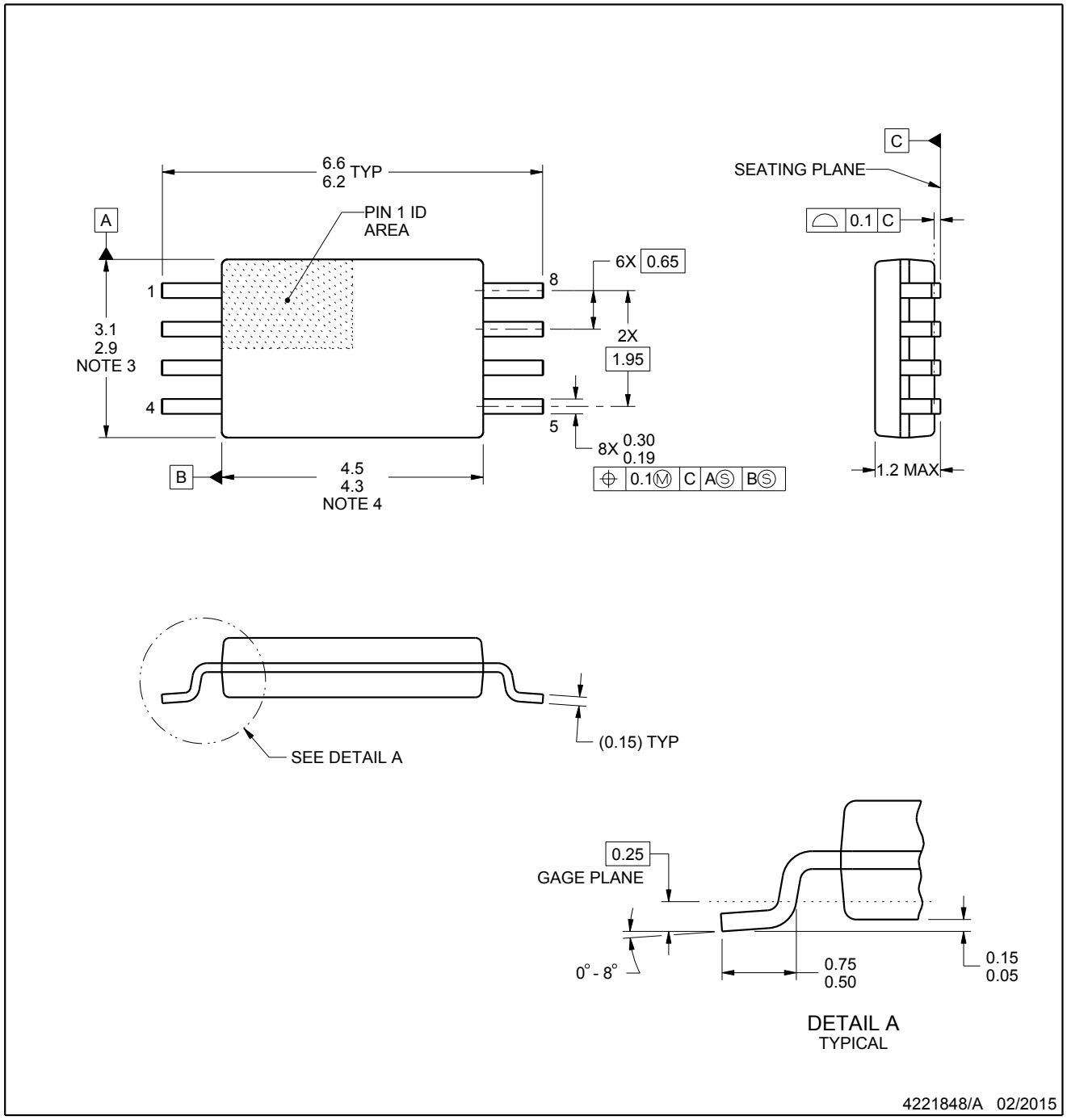
PACKAGE OUTLINE



PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

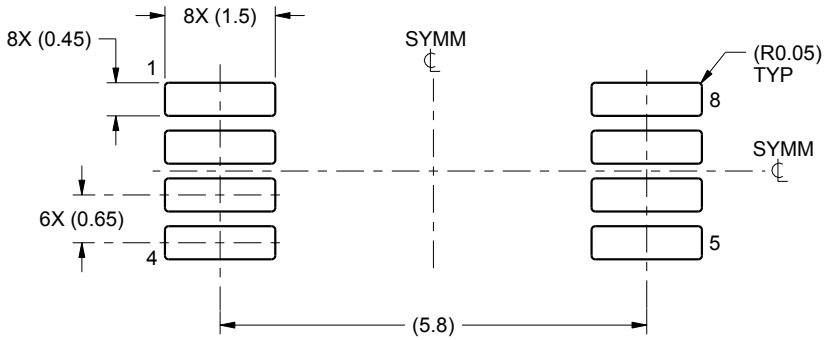
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

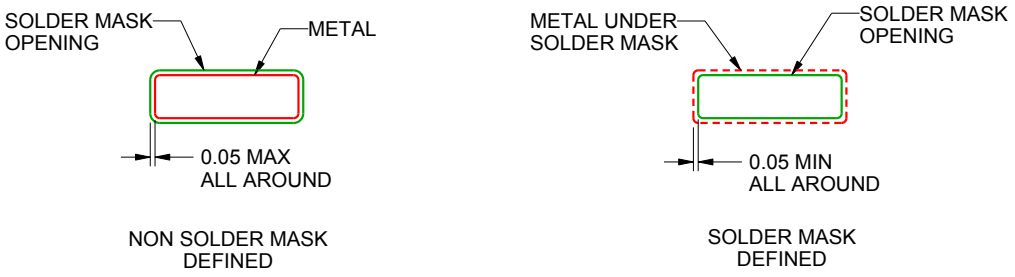
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

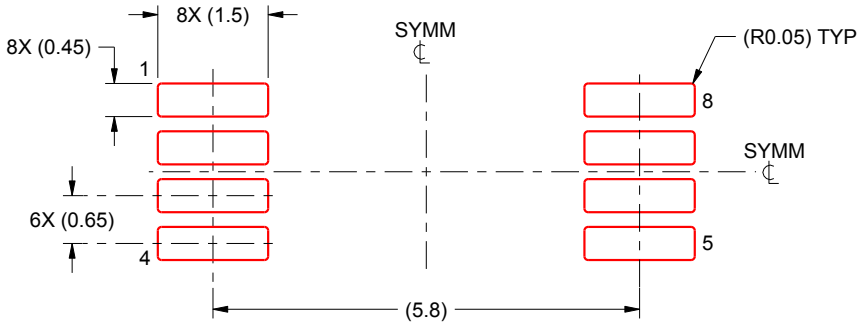
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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