

## **Excellent Integrated System Limited**

Stocking Distributor

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[Vishay/Siliconix](#)  
[IRF830A](#)

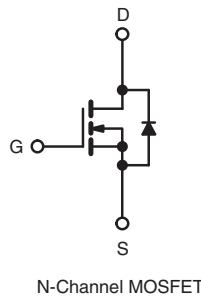
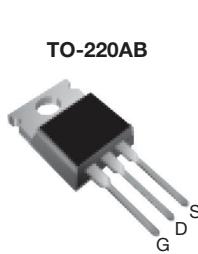
For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)



## Power MOSFET

<b>PRODUCT SUMMARY</b>	
$V_{DS}$ (V)	500
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V 1.4
$Q_g$ (Max.) (nC)	24
$Q_{gs}$ (nC)	6.3
$Q_{gd}$ (nC)	11
Configuration	Single



### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{oss}$  Specified
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed power Switching

### TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half Bridge
- Full Bridge

### ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF830APbF SiHF830A-E3
SnPb	IRF830A SiHF830A

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	500	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	5.0
		$T_C = 100$ °C	3.2
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	20	A
Linear Derating Factor		0.59	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	230	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	5.0	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	7.4	mJ
Maximum Power Dissipation	$P_D$	74	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$	5.3	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25$  °C,  $L = 18$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 5.0$  A (see fig. 12).
- $I_{SD} \leq 5.0$  A,  $dI/dt \leq 370$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

# IRF830A, SiHF830A

Vishay Siliconix



## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

## SPECIFICATIONS ( $T_J = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ µA	500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1$ mA	-	0.60	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ µA	2.0	-	4.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30$ V	-	-	± 100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500$ V, $V_{GS} = 0$ V	-	-	25	µA
		$V_{DS} = 400$ V, $V_{GS} = 0$ V, $T_J = 125$ °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 3.0$ A <sup>b</sup>	-	-	1.4
Forward Transconductance	$g_{fs}$	$V_{DS} = 50$ V, $I_D = 3.0$ A <sup>b</sup>	2.8	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1.0$ MHz, see fig. 5	-	620	-	pF
Output Capacitance	$C_{oss}$		-	93	-	
Reverse Transfer Capacitance	$C_{rss}$		-	4.3	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0$ V; $V_{DS} = 1.0$ V, $f = 1.0$ MHz		886		
Output Capacitance	$C_{oss}$	$V_{GS} = 0$ V; $V_{DS} = 400$ V, $f = 1.0$ MHz		27		
Effective Output Capacitance	$C_{oss\ eff.}$	$V_{GS} = 0$ V; $V_{DS} = 0$ V to 400 V <sup>c</sup>		39		
Total Gate Charge	$Q_g$	$V_{GS} = 10$ V	$I_D = 5.0$ A, $V_{DS} = 400$ V, see fig. 6 and 13 <sup>b</sup>	-	-	24
Gate-Source Charge	$Q_{gs}$			-	-	6.3
Gate-Drain Charge	$Q_{gd}$			-	-	11
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250$ V, $I_D = 5.0$ A, $R_g = 14$ Ω, $R_D = 49$ Ω, see fig. 10 <sup>b</sup>		-	10	-
Rise Time	$t_r$			-	21	-
Turn-Off Delay Time	$t_{d(off)}$			-	21	-
Fall Time	$t_f$			-	15	-
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.0
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	20
Body Diode Voltage	$V_{SD}$	$T_J = 25$ °C, $I_S = 5.0$ A, $V_{GS} = 0$ V <sup>b</sup>	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25$ °C, $I_F = 5.0$ A, $dI/dt = 100$ A/µs <sup>b</sup>		-	430	650
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	1.62	2.4
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300$  µs; duty cycle  $\leq 2$  %.
- $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

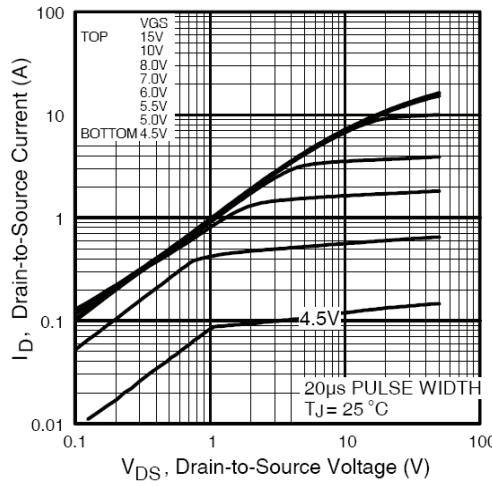


Fig. 1 - Typical Output Characteristics

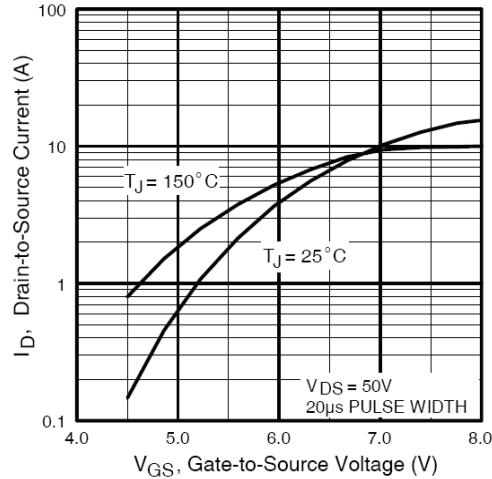


Fig. 3 - Typical Transfer Characteristics

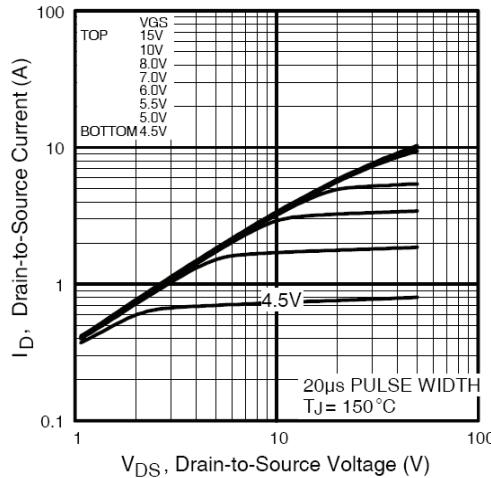


Fig. 2 - Typical Output Characteristics

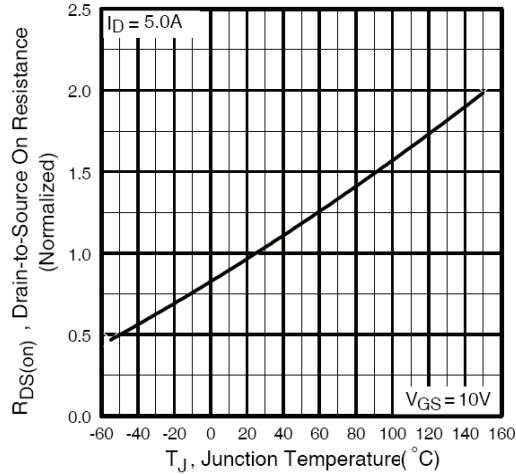


Fig. 4 - Normalized On-Resistance vs. Temperature

## IRF830A, SiHF830A

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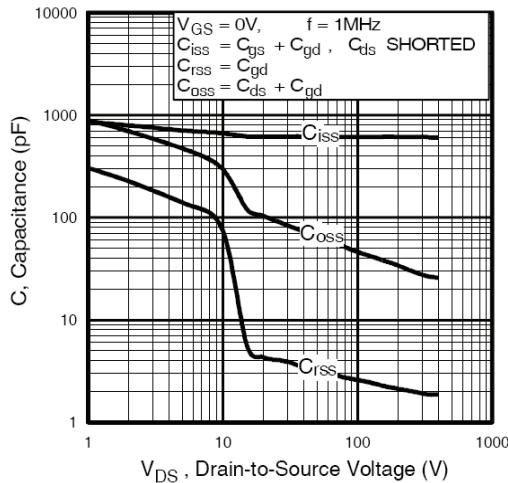


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

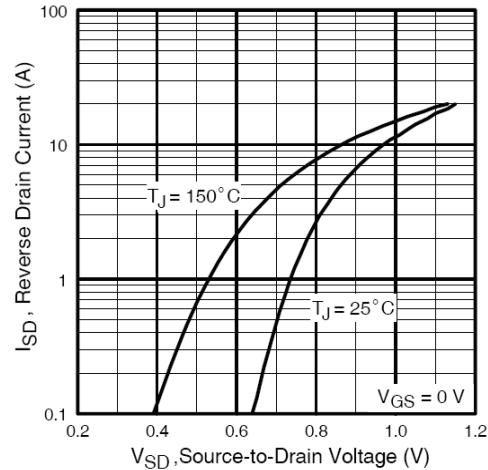


Fig. 7 - Typical Source-Drain Diode Forward Voltage

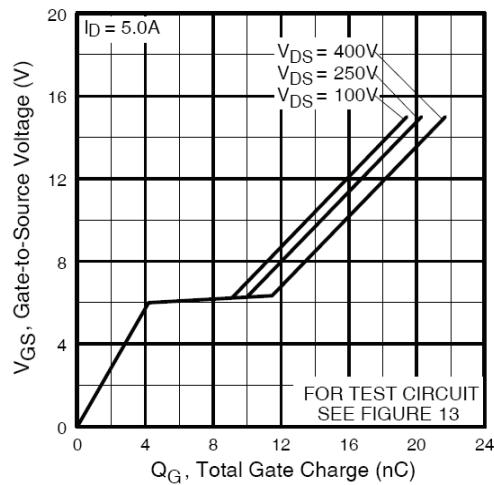


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

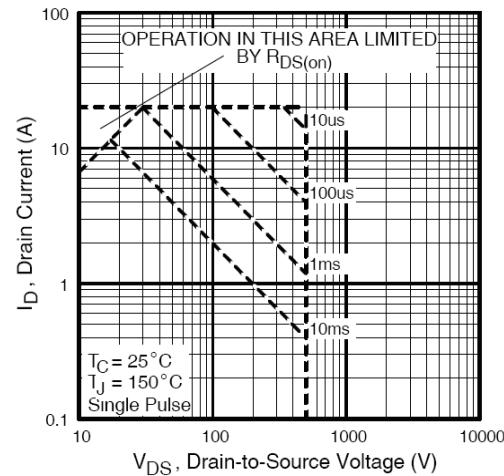


Fig. 8 - Maximum Safe Operating Area



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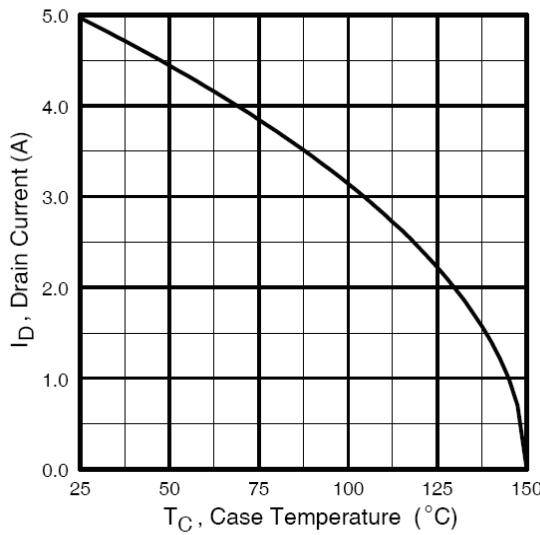


Fig. 9 - Maximum Drain Current vs. Case Temperature

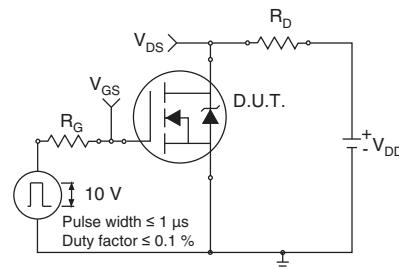


Fig. 10a - Switching Time Test Circuit

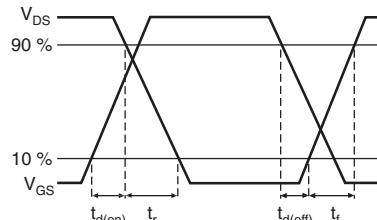


Fig. 10b - Switching Time Waveforms

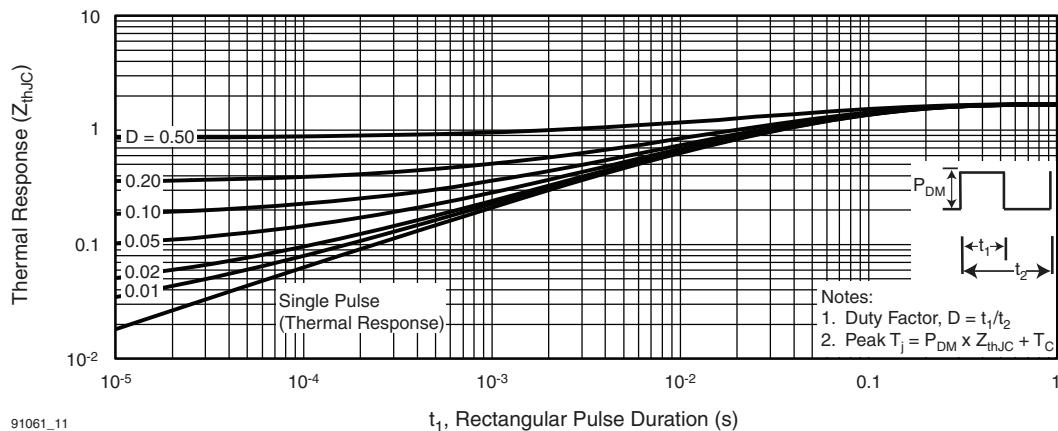


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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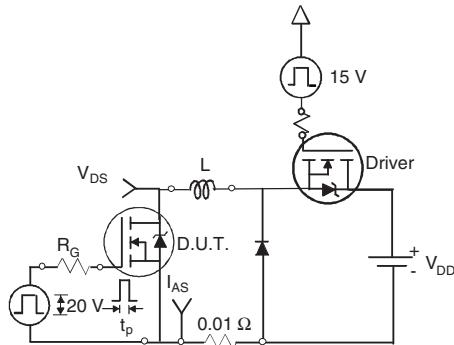


Fig. 12a - Unclamped Inductive Test Circuit

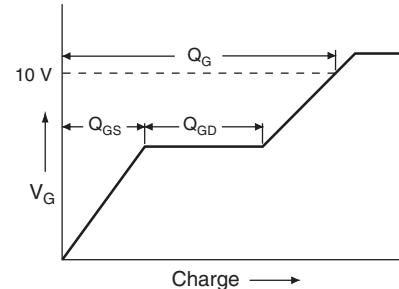


Fig. 12d - Basic Gate Charge Waveform

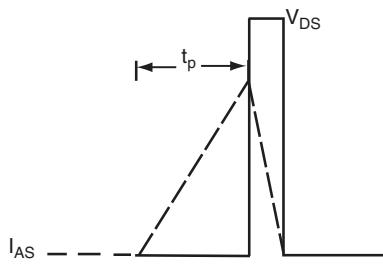


Fig. 12b - Unclamped Inductive Waveforms

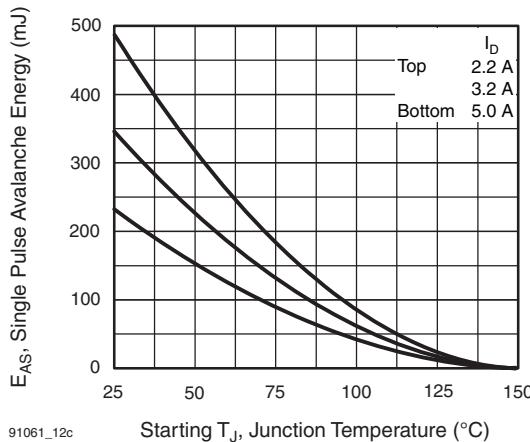


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

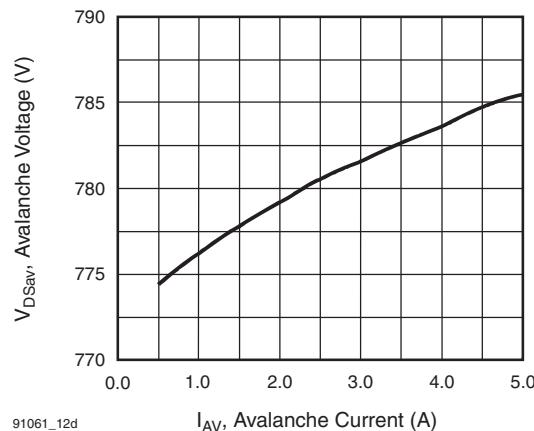


Fig. 13a - Typical Drain-to-Source Voltage vs. Avalanche Current

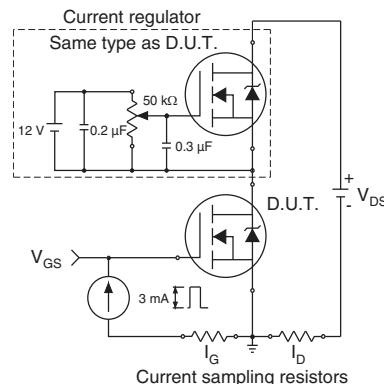
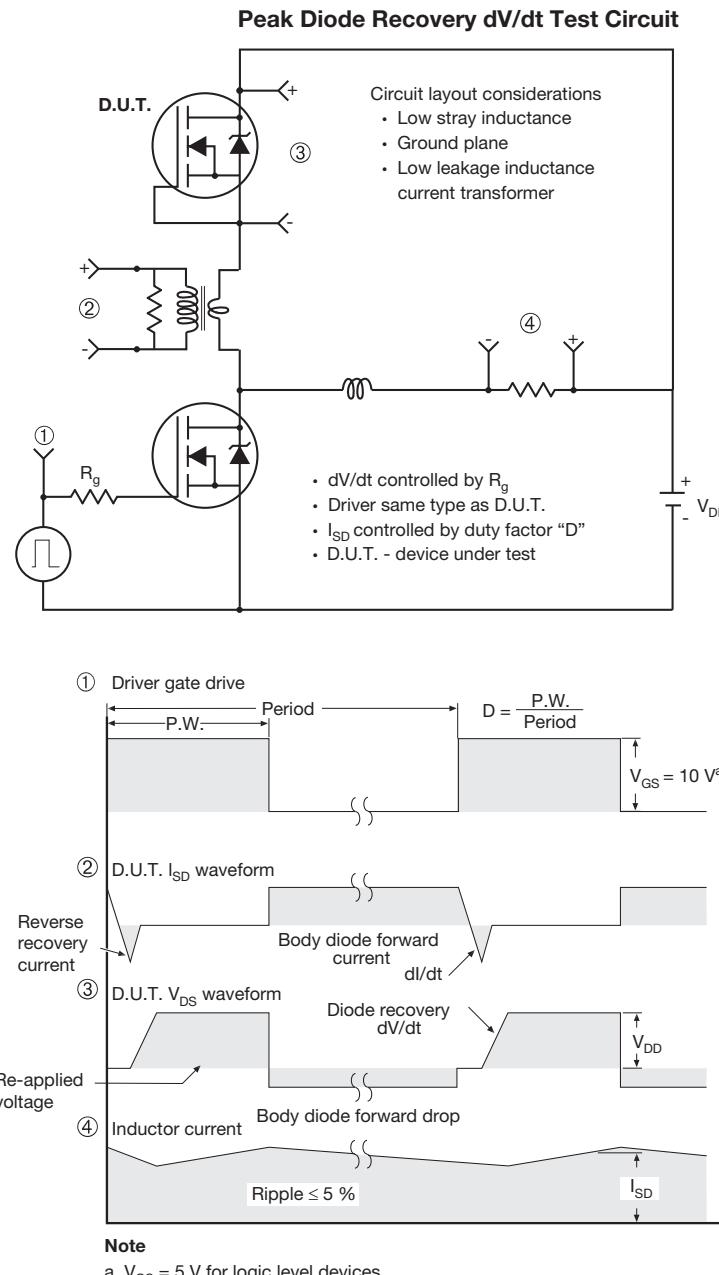


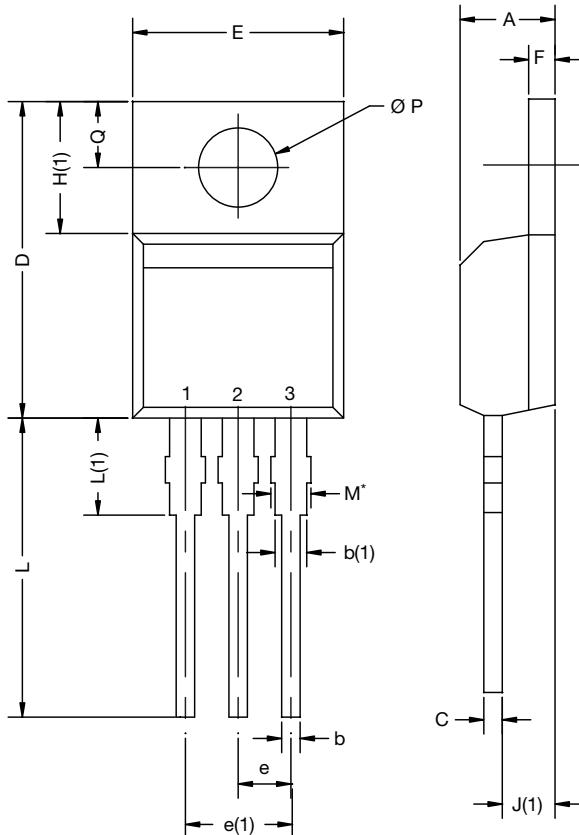
Fig. 13b - Gate Charge Test Circuit



**Fig. 14 - For N-Channel**

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**TO-220-1**



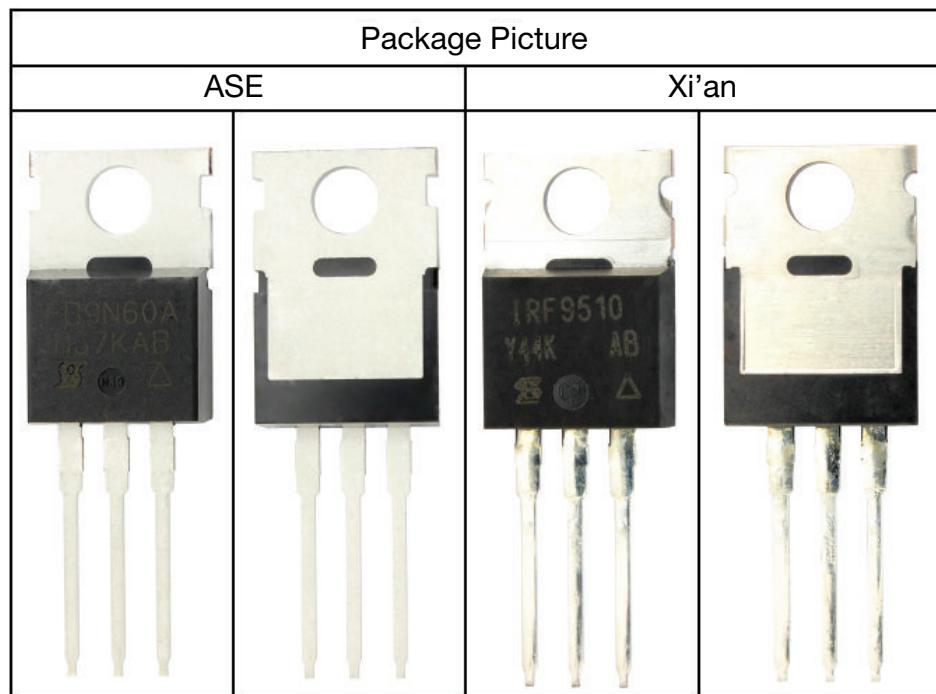
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15  
DWG: 6031

**Note**

- $M^* = 0.052$  inches to  $0.064$  inches (dimension including protrusion), heatsink hole for HVM

**Package Picture**





## Legal Disclaimer Notice

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