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Data Sheet No. PD-9.471A

T-37-21

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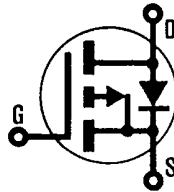
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HEXFET® TRANSISTORS

IRF9Z30

IRF9Z32

**P-CHANNEL
50 VOLT
POWER MOSFETs**



-50 Volt, 0.14 Ohm, HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuit and pulse amplifiers.

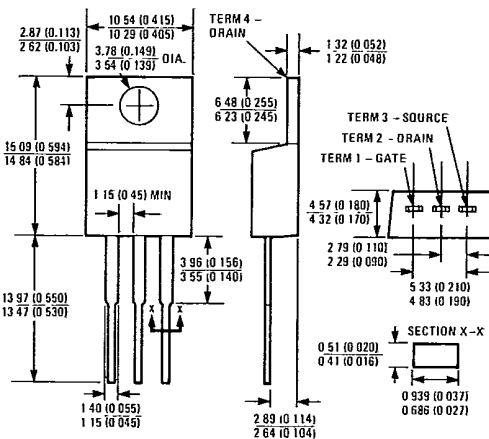
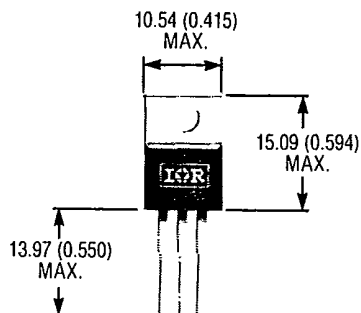
Features

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability

Product Summary

Part Number	V _{DS}	R _{DS(on)}	I _D
IRF9Z30	-50V	0.14Ω	-18A
IRF9Z32	-50V	0.21Ω	-15A

CASE STYLE AND DIMENSIONS



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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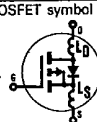
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Absolute Maximum Ratings

Parameter	IRF9Z30	IRF9Z32	Units
V_{DS} Drain - Source Voltage ①	-50	-50	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ K}\Omega$) ①	-50	-50	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	-18	-15	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	-11	-9.3	A
I_{DM} Pulsed Drain Current ②	-60	-50	A
V_{GS} Gate - Source Voltage	± 20		V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	74		W
Linear Derating Factor	0.59		W/K ③
I_{LM} Inductive Current, Clamped	(See Fig. 14) $L = 100\mu\text{H}$		A
I_L Unclamped Inductive Current (Avalanche Current) ③	(See Fig. 15) -3.1		A
T_{Jstg} Operating Junction and Storage Temperature Range	-55 to 150		$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		$^\circ\text{C}$

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DS} Drain - Source Breakdown Voltage	IRF9Z30	-50	—	—	V	$V_{GS} = 0\text{V}$
	IRF9Z32	—	—	—	V	$I_D = -250\mu\text{A}$
$V_{GS(th)}$ Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu\text{A}$
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$
	ALL	—	—	-1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ④	IRF9Z30	-18	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = -10\text{V}$
	IRF9Z32	-15	—	—	A	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ④	IRF9Z30	—	0.093	0.14	Ω	$V_{GS} = -10\text{V}$, $I_D = -9.3\text{A}$
	IRF9Z32	—	0.14	0.21	Ω	
g_{fs} Forward Transconductance ④	ALL	3.1	4.7	—	S(U)	$V_{DS} = 2 \times V_{GS}$, $I_{DS} = -9.0\text{A}$
C_{iss} Input Capacitance	ALL	—	900	—	pF	$V_{GS} = 0\text{V}$, $V_{DS} = -25\text{V}$, $f = 1.0\text{ MHz}$
C_{oss} Output Capacitance	ALL	—	570	—	pF	See Fig. 10
C_{rss} Reverse Transfer Capacitance	ALL	—	140	—	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	12	18	ns	$V_{DD} = -25\text{V}$, $I_D \approx -18\text{A}$, $R_G = 13\Omega$, $R_D = 1.3\Omega$
t_r Rise Time	ALL	—	110	170	ns	See Fig. 16
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	21	32	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f Fall Time	ALL	—	64	96	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	26	39	nC	$V_{GS} = -10\text{V}$, $I_D = -18\text{A}$, $V_{DS} = 0.8\text{ Max. Rating}$. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	6.9	10	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	9.7	15	nC	
L_D Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	1.7	K/W ⑤	
R_{thCS} Case-to-Sink	ALL	—	1.0	—	K/W ⑤	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	80	K/W ⑤	Typical socket mount

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9Z30	—	—	-18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF9Z32	—	—	-15	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9Z30	—	—	-60	A	
		IRF9Z32	—	—	-50	A	
V_{SD}	Diode Forward Voltage ②	ALL	—	—	-6.3	V	$T_J = 25^\circ\text{C}$, $I_S = -18\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	54	120	250	ns	$T_J = 25^\circ\text{C}$, $I_F = -18\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	0.20	0.47	1.1	μC	$T_J = 25^\circ\text{C}$, $I_F = -18\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C

② $K/W = ^\circ\text{C}/\text{W}$
 $W/K = \text{W}/^\circ\text{C}$

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ @ $V_{dd} = -25\text{V}$, $T_J = 25^\circ\text{C}$
 $L = 100 \mu\text{H}$, $R_G = 25\Omega$

⑤ Pulse Test: Pulse width $\leq 300 \mu\text{s}$,
Duty Cycle $\leq 2\%$

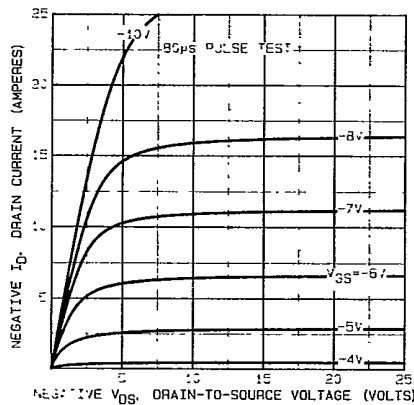


Fig. 1 — Typical Output Characteristics

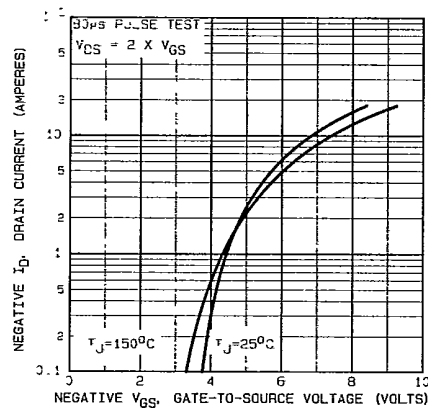


Fig. 2 — Typical Transfer Characteristics

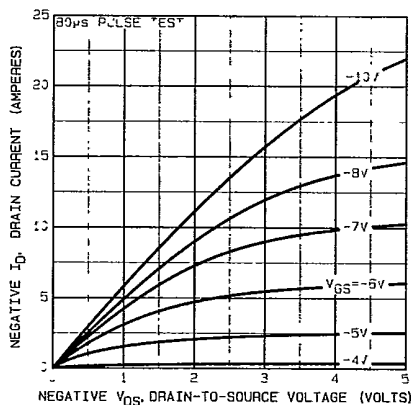


Fig. 3 — Typical Saturation Characteristics

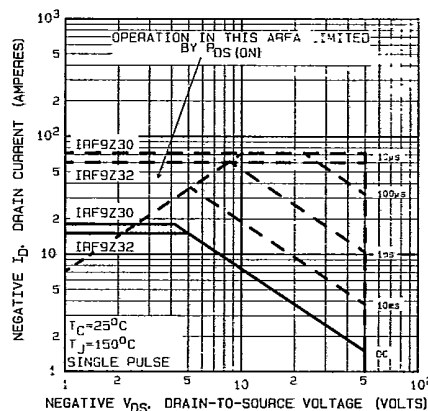


Fig. 4 — Maximum Safe Operating Area

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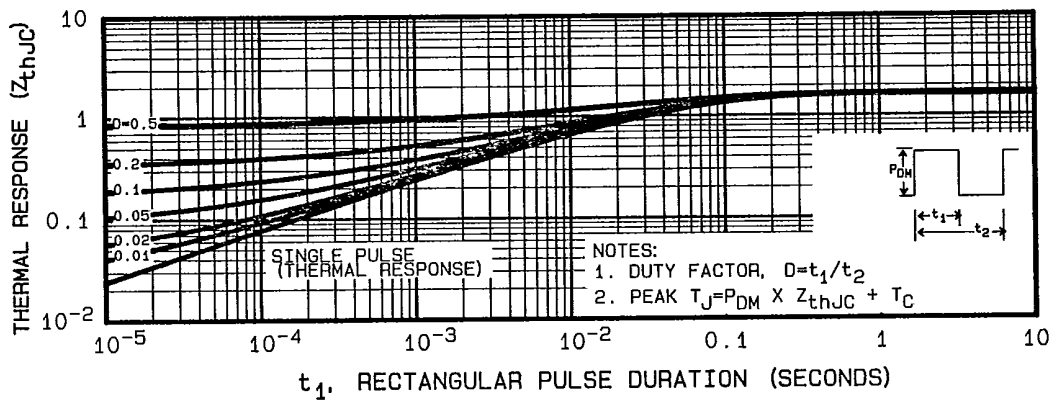


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

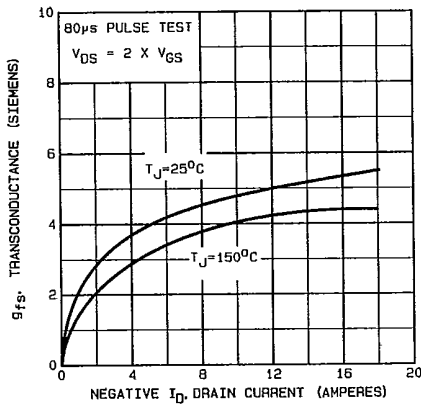


Fig. 6 — Typical Transconductance Vs. Drain Current

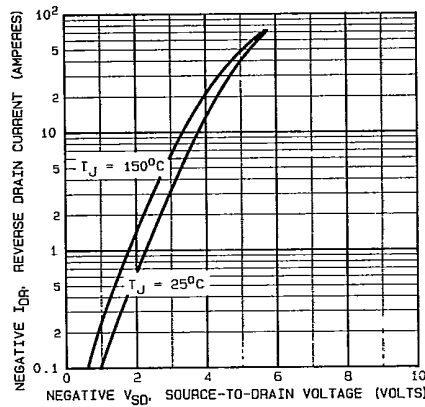


Fig. 7 — Typical Source-Drain Diode Forward Voltage

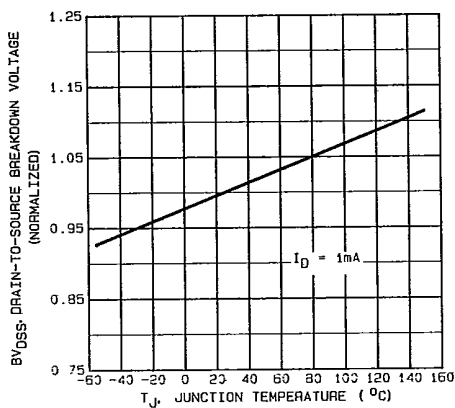


Fig. 8 — Breakdown Voltage Vs. Temperature

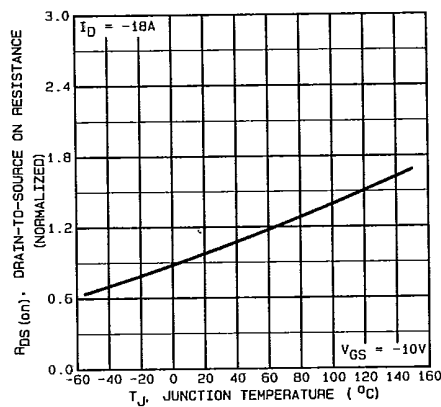
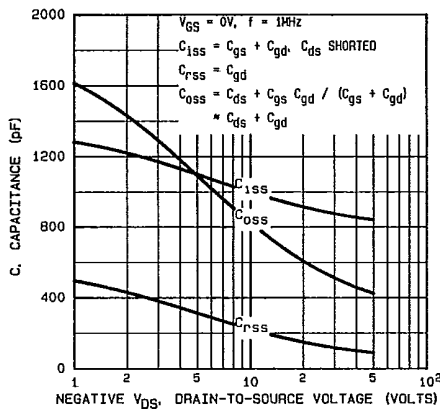
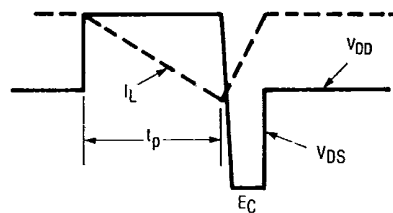
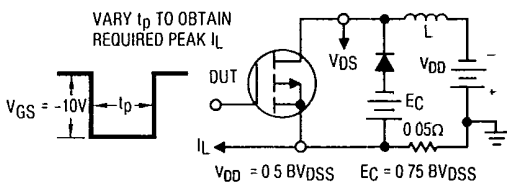
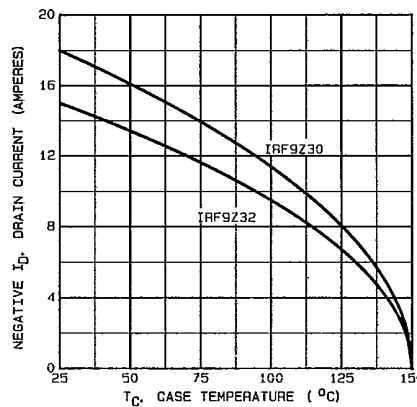
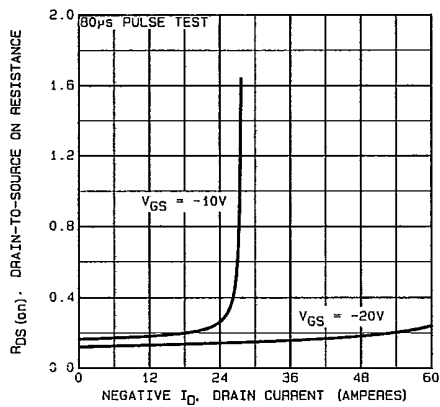
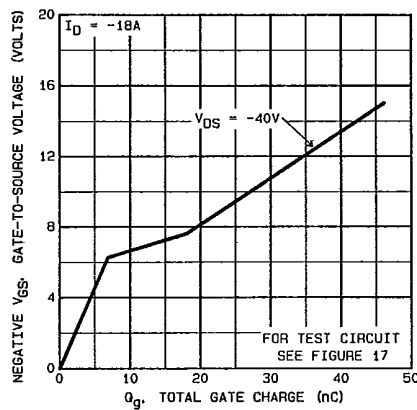


Fig. 9 — Normalized On-Resistance Vs. Temperature

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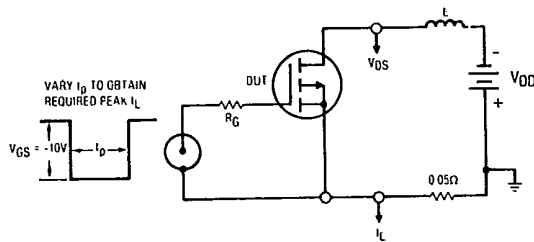


Fig. 15a — Unclamped Inductive Test Circuit

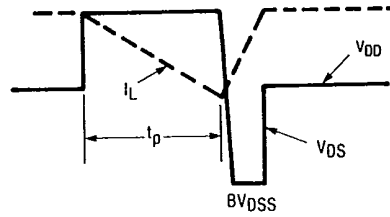


Fig. 15b — Unclamped Inductive Load Test Waveforms

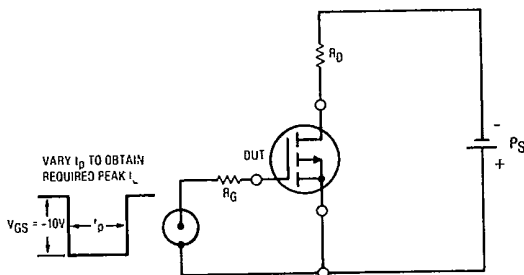


Fig. 16 — Switching Time Test Circuit

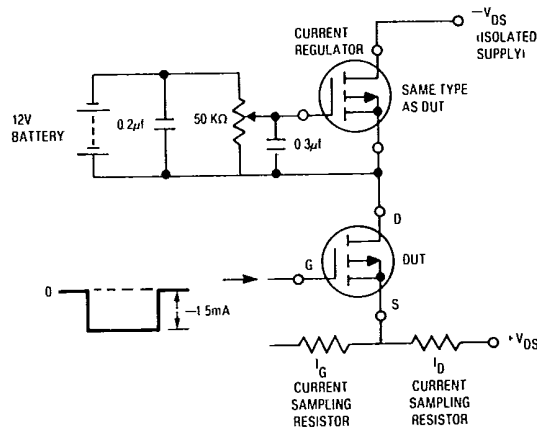
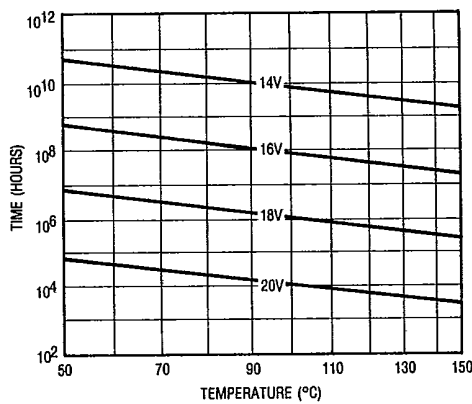
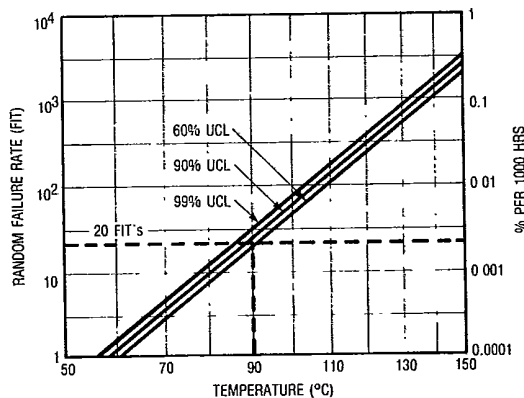


Fig. 17 — Gate Charge Test Circuit



***Fig. 18 — Typical time to Accumulated 1% Gate Failure**



***Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate**

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.