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Stocking Distributor

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[Vishay/Siliconix](#)
[IRFI9620G](#)

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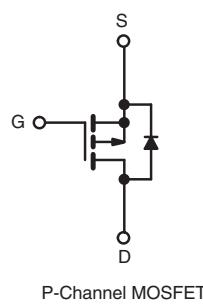
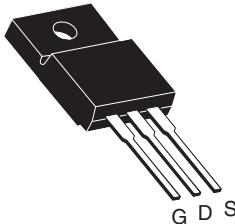
sales@integrated-circuit.com



Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	- 200
R _{DS(on)} (Ω)	V _{GS} = - 10 V 1.5
Q _g (Max.) (nC)	15
Q _{gs} (nC)	3.2
Q _{gd} (nC)	8.4
Configuration	Single

TO-220 FULLPAK



FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Dist. = 4.8 mm
- P-Channel
- Dynamic dV/dt
- Low Thermal Resistance
- Lead (Pb)-free Available



DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI9620GPbF SiHFI9620G-E3
SnPb	IRFI9620G SiHFI9620G

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	- 200	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	I _D	- 3.0	A
		- 1.9	
Pulsed Drain Current ^a	I _{DM}	- 12	
Linear Derating Factor		0.24	W/°C
Single Pulse Avalanche Energy ^b	E _{AS}	80	mJ
Repetitive Avalanche Current ^a	I _{AR}	- 3.0	A
Repetitive Avalanche Energy ^a	E _{AR}	3.0	mJ
Maximum Power Dissipation	P _D	30	W
Peak Diode Recovery dV/dt ^c	dV/dt	- 5.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating: pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = - 50 V, starting T_J = 25 °C, L = 13 mH, R_G = 25 Ω, I_{AS} = - 3.0 A (see fig. 12).
- I_{SD} ≤ - 3.9 A, dI/dt ≤ 95 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

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Thermal Resistance Ratings

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	-	4.1	

Specifications $T_J = 25^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$		- 200	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = -1 \text{ mA}$		-	- 0.22	-	$^{\circ}\text{C}/\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$		- 2.0	-	- 4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	μA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -200 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	- 100	μA	
		$V_{DS} = -160 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^{\circ}\text{C}$		-	-	- 500		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10 \text{ V}$	$I_D = -1.8 \text{ A}^b$	-	-	1.5	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = -50 \text{ V}$, $I_D = -1.8 \text{ A}^b$		1.3	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = -15 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	340	-	pF	
Output Capacitance	C_{oss}			-	110	-		
Reverse Transfer Capacitance	C_{rss}			-	33	-		
Drain to Sink Capacitance	C	$f = 1 \text{ MHz}$		-	12	-		
Total Gate Charge	Q_g	$V_{GS} = -10 \text{ V}$	$I_D = -2.1 \text{ A}$, $V_{DS} = -160 \text{ V}$, see fig. 6 and 13 ^b	-	-	15	nC	
Gate-Source Charge	Q_{gs}			-	-	3.2		
Gate-Drain Charge	Q_{gd}			-	-	8.4		
Turn-On Delay Time	$t_{d(on)}$			-	8.8	-		
Rise Time	t_r	$V_{DD} = -100 \text{ V}$, $I_D = -3.9 \text{ A}$, $R_G = 18 \Omega$, $R_D = 24 \Omega$, see fig. 10 ^b		-	27	-	ns	
Turn-Off Delay Time	$t_{d(off)}$			-	7.3	-		
Fall Time	t_f			-	19	-		
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	L_S			-	7.5	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	- 3.0	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	- 12		
Body Diode Voltage	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_S = -3.0 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	- 6.3	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_F = -3.9 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	150	300	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.97	2.0	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2\%$.



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

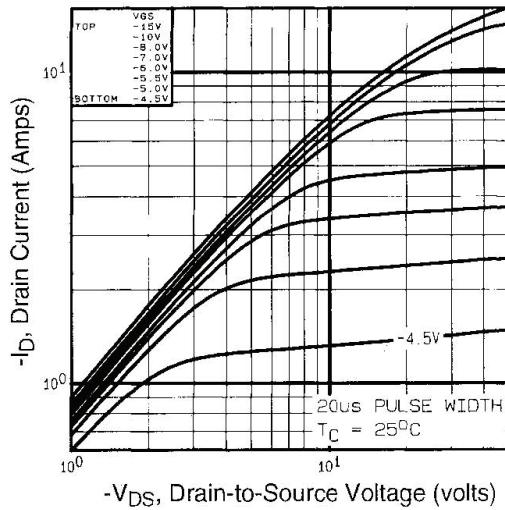


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

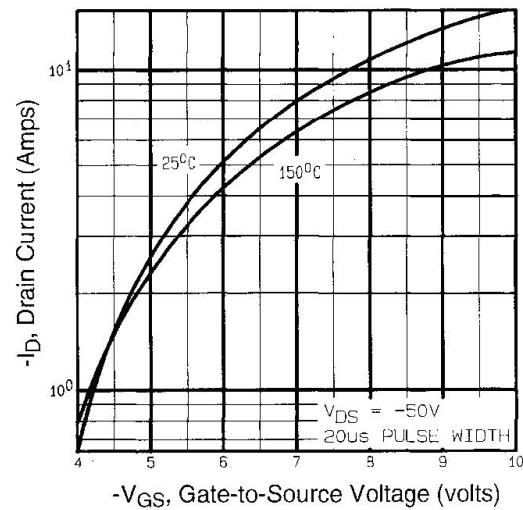


Fig. 3 - Typical Transfer Characteristics

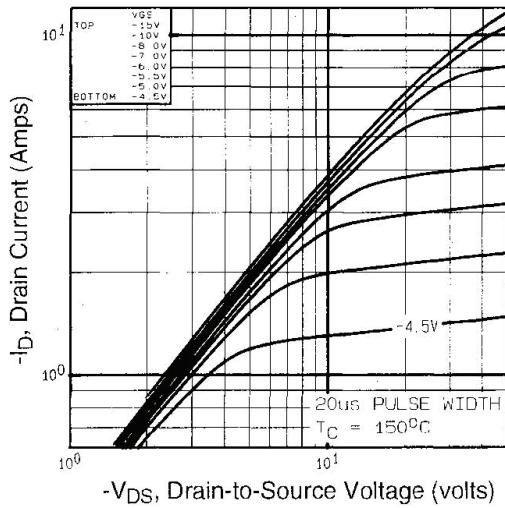


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$

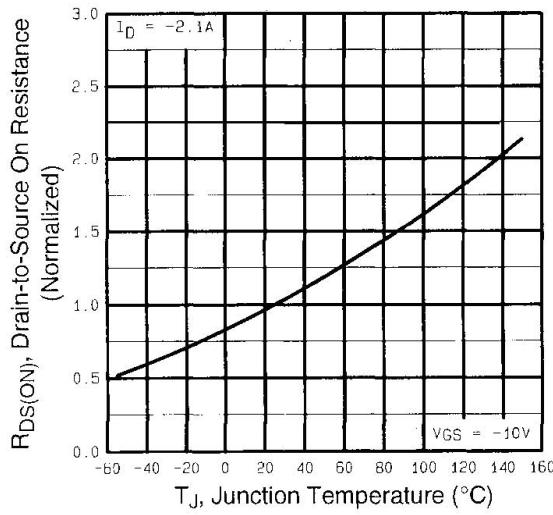


Fig. 4 - Normalized On-Resistance vs. Temperature

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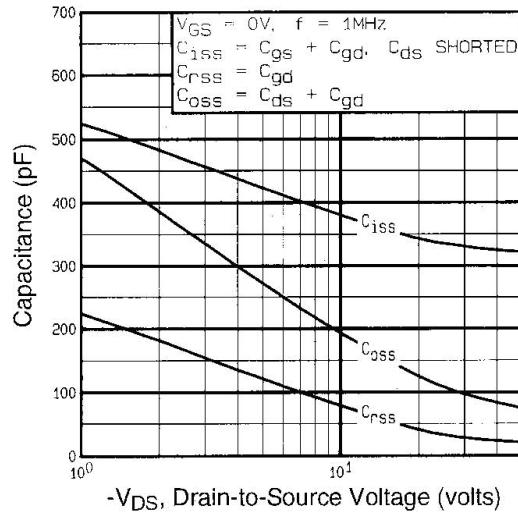


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

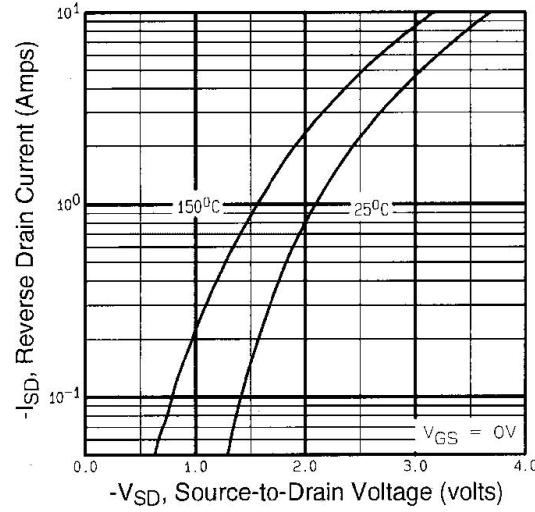


Fig. 7 - Typical Source-Drain Diode Forward Voltage

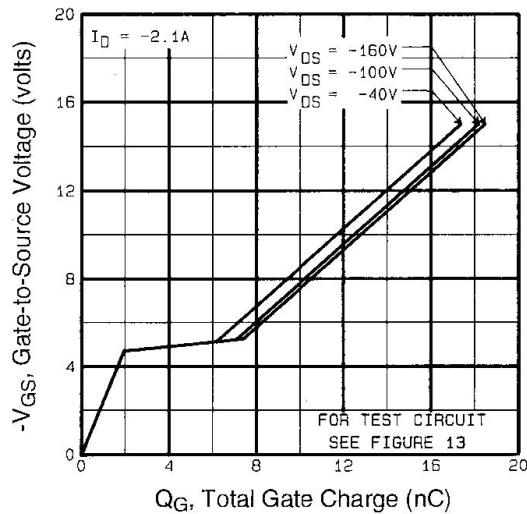


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

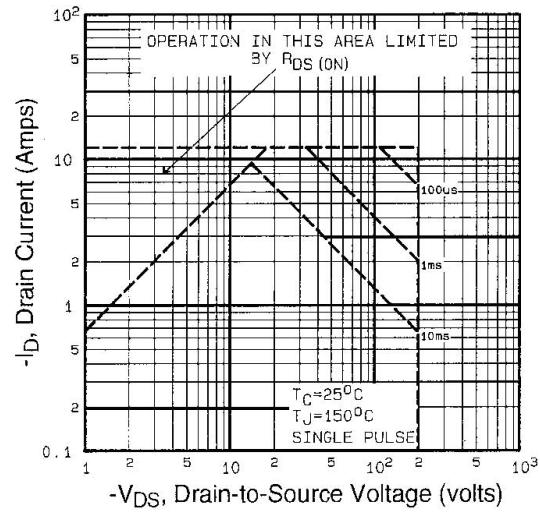


Fig. 8 - Maximum Safe Operating Area



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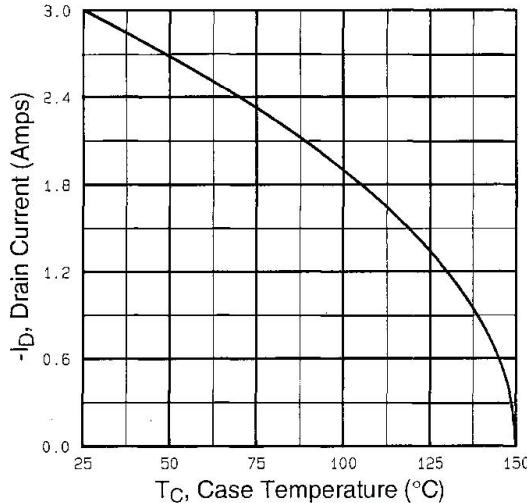


Fig. 9 - Maximum Drain Current vs. Case Temperature

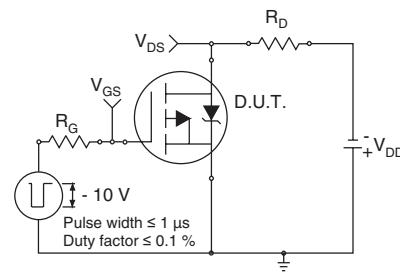


Fig. 10a - Switching Time Test Circuit

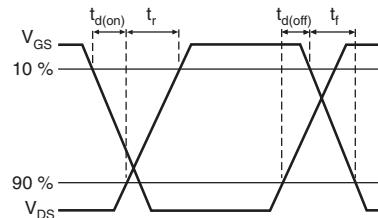


Fig. 10b - Switching Time Waveforms

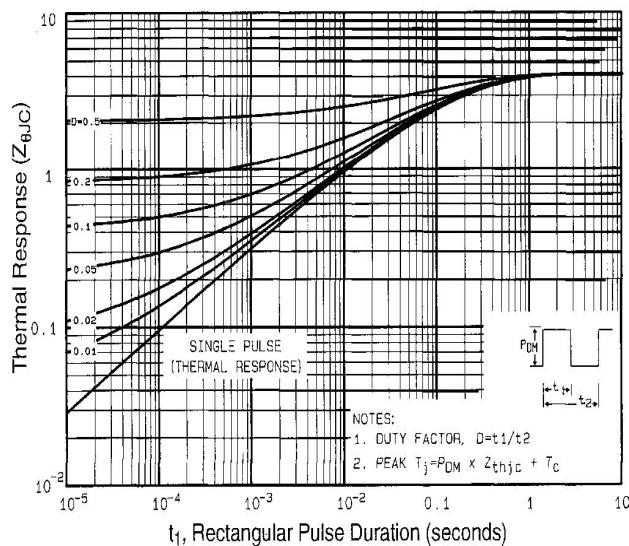


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

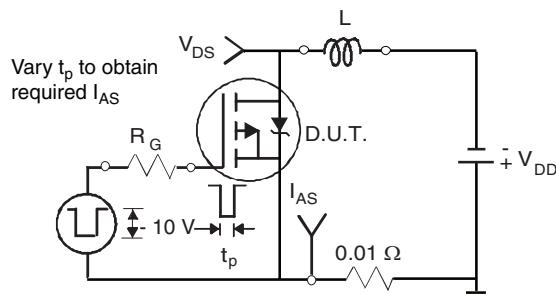


Fig. 12a - Unclamped Inductive Test Circuit

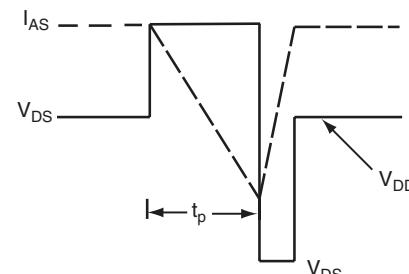


Fig. 12b - Unclamped Inductive Waveforms

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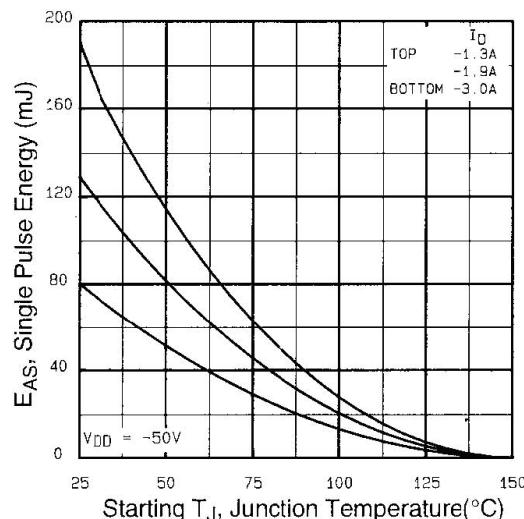


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

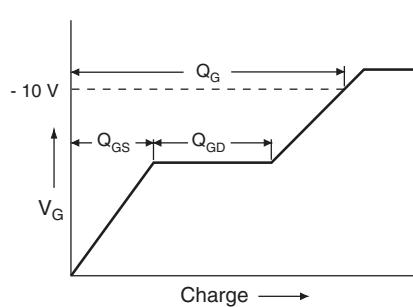


Fig. 13a - Basic Gate Charge Waveform

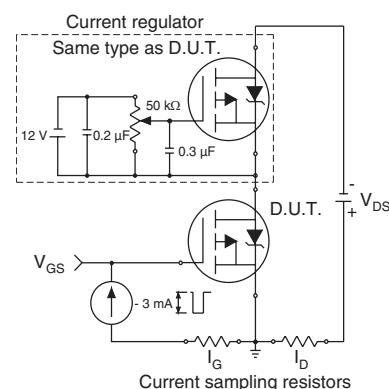
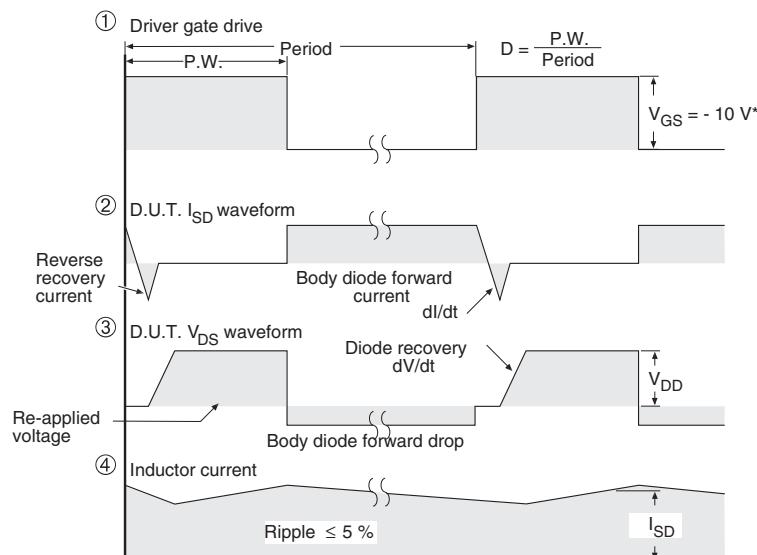
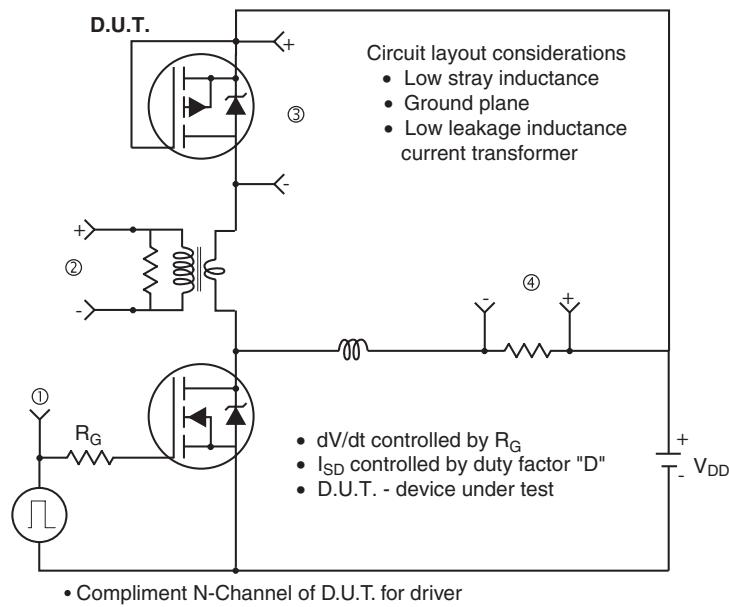


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = -5 V$ for logic level and $-3 V$ drive devices

Fig. 14 - For P-Channel

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