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ON Semiconductor
P3MS650100H-4CR

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Distributor of ON Semiconductor: Excellent Integrated System Limited
Datasheet of P3MS650100H-4CR - IC CLK GEN EMI REDUCTION 4WDFN
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P3MS650100H

1.8V/2.5V/3.3V, LVCMOS Peak EMI Reduction Clock Generator

ON Semiconductor®

http://onsemi.com

Product Description

P3MS650100H device is a spread spectrum frequency modulator clock generator with 1.8 V/2.5 V/3.3 V LVCMOS output designed specifically for clock frequencies between 15 MHz and 60 MHz. P3MS650100H reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The device allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, and shielding that are traditionally required to pass EMI regulations.

P3MS650100H accepts an LVCMOS input from an external reference clock and locks to a 1x modulated clock output. P3MS650100H goes to power down mode for power save when no clock is present on CLKIN pin. ModOUT goes 'low' in power down mode.

P3MS650100H operates over −20°C to +85°C and is available in a 4 Pin WDFN, (1.2mmX1.0mm) Package.

Features

- Peak EMI Reduction Clock Generator with LVCMOS Output
- Supply Voltage and Input / Output Clock Frequency Range
  1.6 V – 2.0 V: 15 MHz – 30 MHz
  2.3 V – 3.6 V: 15 MHz – 60 MHz
- Frequency Deviation: ±1.4% @ 24 MHz
- Power Down current less than 1 μA
- 4−pin WDFN (1.2mmX1.0mm) Package
- Output Drive Current: 1.8 V: 8 mA
  2.5 V/3.3 V: 16 mA
- Operating temperature range: −20°C to +85°C
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- P3MS650100H is targeted towards consumer electronic applications like mobile Phones, tablets, net books and MIDs

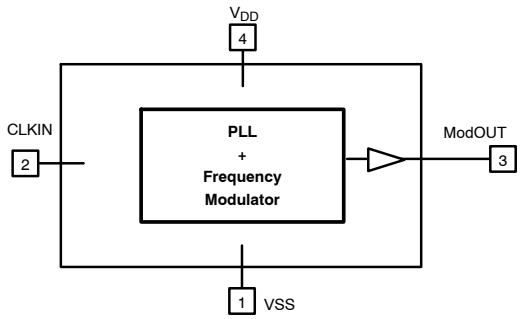
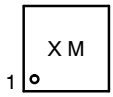


Figure 1. Simplified Block Diagram

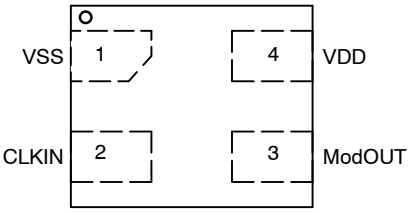
MARKING DIAGRAM

WDFN4
CASE 511BS



X = Specific Device Code
M = Date Code

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	VSS	Power	Ground connection.
2	CLKIN	Input	LVCMOS External reference clock input.
3	ModOUT	Output	Spread Spectrum Clock Output.
4	VDD	Power	Power supply for the entire chip

Table 2. OPERATING CONDITIONS

Symbol	Description	Min	Max	Unit
V_{DD} (1.8 V)	Supply Voltage with respect to V_{SS}	1.6	2.0	V
V_{DD} (2.5 V/3.3 V)		2.3	3.6	
T_A	Operating temperature	−20	+85	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		5	pF

Table 3. ABSOLUTE MAXIMUM RATING

Symbol	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any input pin with respect to V_{SS}	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. DC Electrical Characteristics V_{DD} = 1.6 V – 2.0 V, T_A= –20°C to +85°C

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Supply Voltage with respect to VSS		1.6	1.8	2.0	V
I_{DD}	Dynamic supply current (Unloaded Output)	15MHz		1.3	1.8	mA
		30MHz		2	2.8	
I_{CC}	Static supply current (No Clock @ CLKIN)				1	μA
V_{IH}	Input high voltage		0.65*VDD			V
V_{IL}	Input low voltage				0.3*VDD	V
I_{IH}	Input high current (CLKIN pin)				10	μA
I_{IL}	Input low current (CLKIN pin)				10	μA
V_{OH}	Output high voltage, I_{OH} = – 8mA		0.75*VDD			V
V_{OL}	Output low voltage , I_{OL} = 8mA				0.2*VDD	V
Z_{OUT}	Output impedance			28		Ω

Table 5. AC ELECTRICAL CHARACTERISTICS V_{DD} = 1.6 V – 2.0 V, T_A = –20°C to +85°C

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN	Input Clock frequency		15		30	MHz
ModOUT	Output Clock frequency		15		30	MHz
t_{LH} (Notes 1 and 2)	Output rise time (Measured between 20% to 80%)			1.7	2.7	nS
t_{HL} (Notes 1 and 2)	Output fall time (Measured between 80% to 20%)			1.4	2.4	nS
t_{JC} (Notes 2)	Cycle–to–cycle Jitter, Peak (1000 cycles)	15 MHz		400		pS
		24 MHz		250		
		30 MHz				
t_D (Notes 1 and 2)	Output duty cycle (Measured @ 50%)		45	50	55	%
t_{ON} (Notes 1 and 2)	PLL lock Time (Stable power supply, valid clock presented on CLKIN)				3	mS
fd	Frequency Deviation @ 24 MHz			±1.4	±1.55	%

1. All parameters are specified with 15 pF loaded output.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

Table 6. DC ELECTRICAL CHARACTERISTICS V_{DD} = 2.3 V – 3.6 V, T_A = –20°C to +85°C

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Supply Voltage with respect to VSS		2.3	2.8	3.6	V
I_{DD}	Dynamic supply current (Unloaded Output)	15MHz		1.7	3	mA
		30MHz		2.8	5	
		60MHz		5	9	
I_{CC}	Static supply current (No Clock @ CLKIN)				2	μA
V_{IH}	Input high voltage		0.65 * V_{DD}			V
V_{IL}	Input low voltage				0.3 * V_{DD}	V
I_{IH}	Input high current (CLKIN pin)				10	μA
I_{IL}	Input low current (CLKIN pin)				10	μA
V_{OH}	Output high voltage, I_{OH} = –16 mA		0.75 * V_{DD}			V
V_{OL}	Output low voltage, I_{OL} = 16 mA				0.2 * V_{DD}	V
Z_{OUT}	Output impedance			20		Ω

Table 7. AC ELECTRICAL CHARACTERISTICS V_{DD} = 2.3 V – 3.6 V, T_A = –20°C to +85°C

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN	Input Clock frequency		15		60	MHz
ModOUT	Output Clock frequency		15		60	MHz
t_{LH} (Notes 3 and 4)	Output rise time (Measured between 20% to 80%)			0.8	1.6	nS
t_{HL} (Notes 3 and 4)	Output fall time (Measured between 80% to 20%)			0.8	1.6	nS
t_{JC} (Notes 4)	Cycle–to–cycle Jitter, Peak (1000 cycles)	15 MHz		350		pS
		24 MHz		250		
		60 MHz		100		
t_D (Notes 3 and 4)	Output duty cycle		45	50	55	%
t_{ON} (Notes 3 and 4)	PLL lock Time (Stable power supply, valid clock presented on CLKIN)				3	mS
fd	Frequency Deviation @ 24 MHz			±1.4	±1.55	%

3. All parameters are specified with 15 pF loaded output.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production

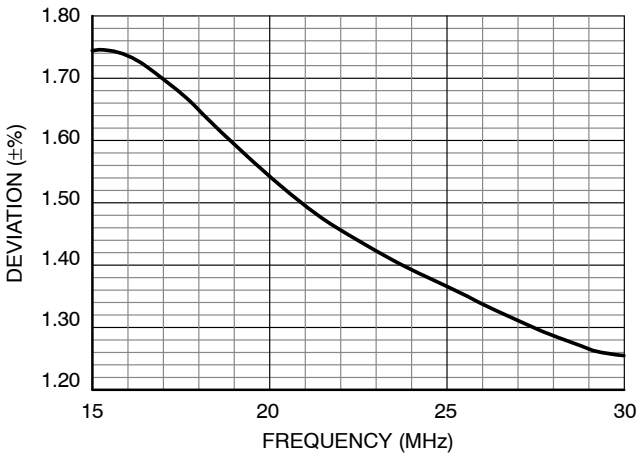


Figure 2. Deviation vs. Frequency (V_{DD} = 1.6 V – 2.0 V)

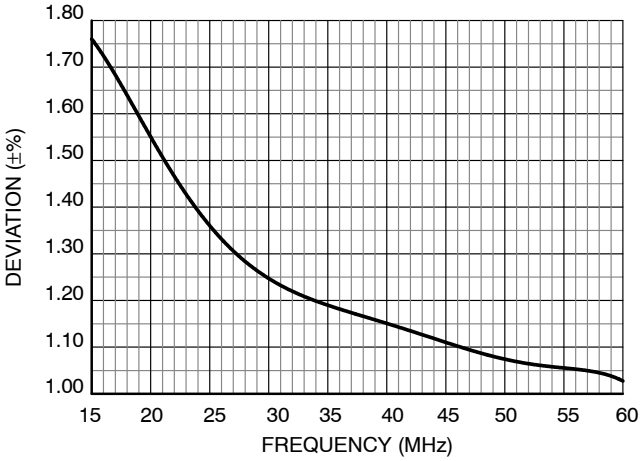
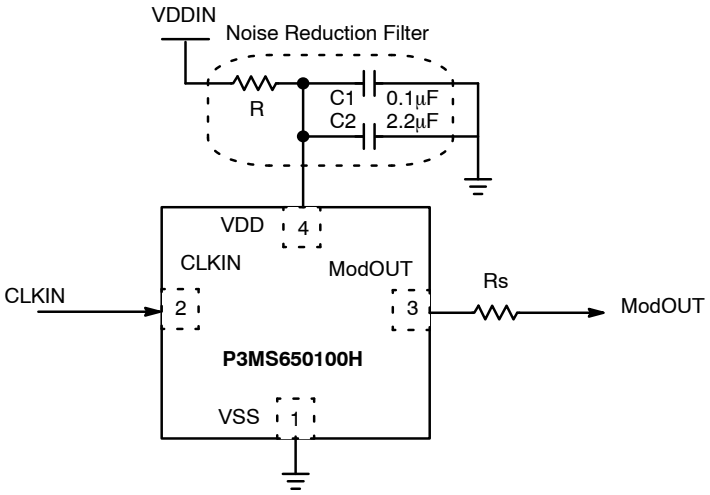


Figure 3. Deviation vs. Frequency (V_{DD} = 2.3 V – 3.6 V)



Rs = Trace Impedance of PCB – Output Impedance of Device (Z0)
Note: Refer Pin Description table for Functionality details

Figure 4. Typical Application Schematic

PCB Layout Recommendation

For optimum device performance, following guidelines are recommended.

- Dedicated V_{DD} and GND planes.
- The device must be isolated from system power supply noise. A 0.1μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the figure below.

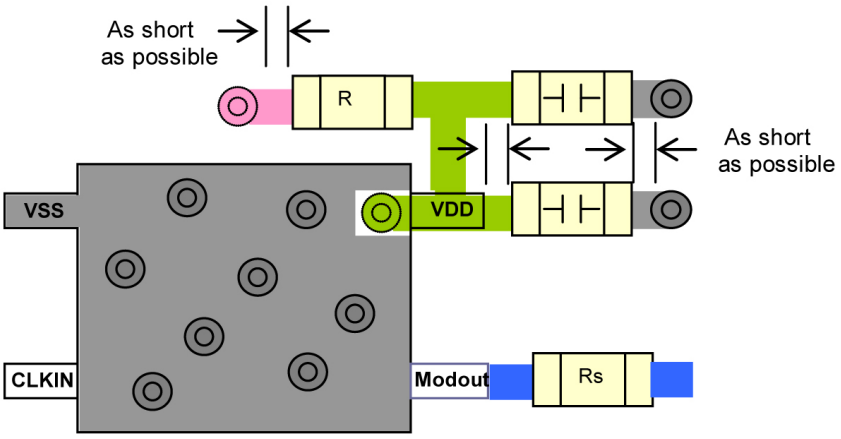


Figure 5. Recommended PCB Layout

ORDERING INFORMATION

Ordering Code	Marking	Temperature	Package Type	Shipping†
P3MS650100H−4CR	A	−20°C to +85°C	4−pin (1.2 mm x 1.0 mm) WDFN (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

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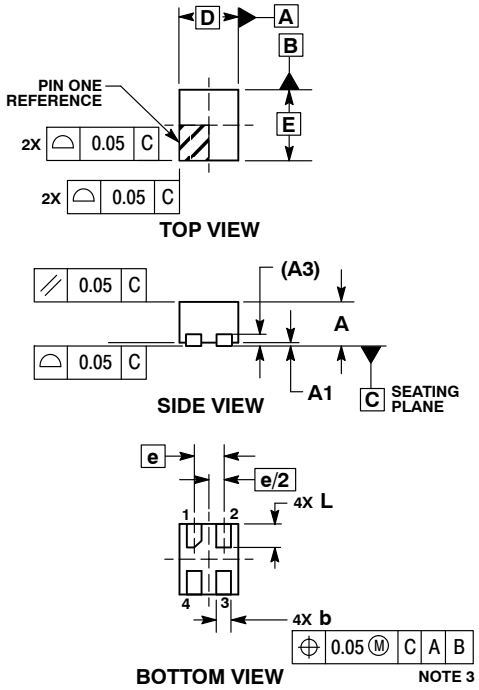
P3MS650100H

PACKAGE DIMENSIONS

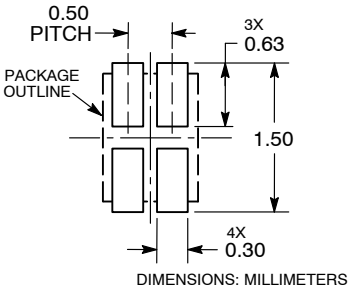
WDFN4, 1.0x1.2, 0.5P
CASE 511BS−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	1.00 BSC	
E	1.20 BSC	
e	0.50 BSC	
L	0.35	0.45

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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