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DS90UR903QSQ/NOPB

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DS90UR903Q/DS90UR904Q 10 - 43MHz 18 Bit Color FPD-Link II Serializer and Deserializer

1 Features

- 10 MHz to 43 MHz Input PCLK Support
- 210 Mbps to 903 Mbps Data Throughput
- Single Differential Pair Interconnect
- Embedded Clock with DC Balanced Coding to Support AC-coupled Interconnects
- Capable to Drive up to 10 meters Shielded Twisted-Pair
- I^2C Compatible Serial Interface for Device Configuration
- Single Hardware Device Addressing Pin
- LOCK Output Reporting Pin to Validate Link Integrity
- Integrated Termination Resistors
- 1.8V- or 3.3V-compatible Parallel Bus Interface
- Single Power Supply at 1.8V
- ISO 10605 ESD and IEC 61000-4-2 ESD Compliant
- Automotive Grade Product: AEC-Q100 Grade 2 Qualified
- Temperature Range −40°C to +105°C
- No Reference Clock Required on Deserializer
- Programmable Receive Equalization
- EMI/EMC Mitigation
  - DES Programmable Spread Spectrum (SSCG) outputs
  - DES Receiver Staggered Outputs

2 Applications

- Automotive Display Systems
  - Central Information Displays
  - Navigation Displays
  - Rear Seat Entertainment

3 Description

The DS90UR903Q/DS90UR904Q chipset offers a FPD-Link II interface with a high-speed forward channel for data transmission over a single differential pair. The Serializer/ Deserializer pair is targeted for direct connections between graphics host controller and displays modules. This chipset is ideally suited for driving video data to displays requiring 18-bit color depth (RGB666 + HS, VS, and DE). The serializer converts 21 bit data over a single high-speed serial stream. This single serial stream simplifies transferring a wide data bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. This significantly saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

The Deserializer inputs provide equalization control to compensate for loss from the media over longer distances. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects.

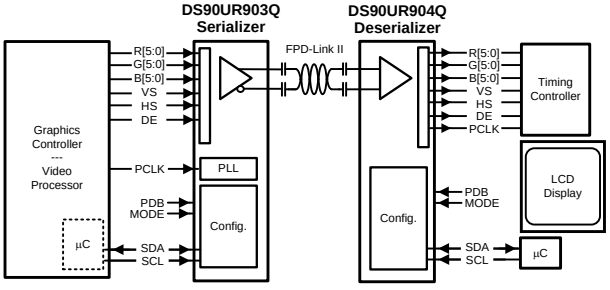
The Serializer is offered in a 40-pin WQFN package and the Deserializer is offered in a 48-pin WQFN package.

Device Information(1)

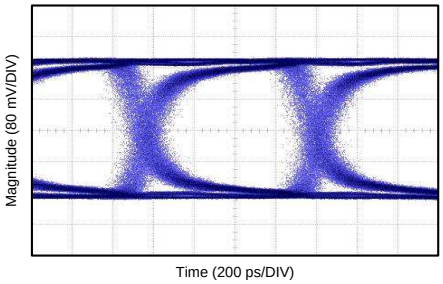
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UR903Q-Q1	WQFN RTA (40)	6.00 mm × 6.00 mm
DS90UR904Q-Q1	WQFN RHS (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Typical Eye Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C — **Page**

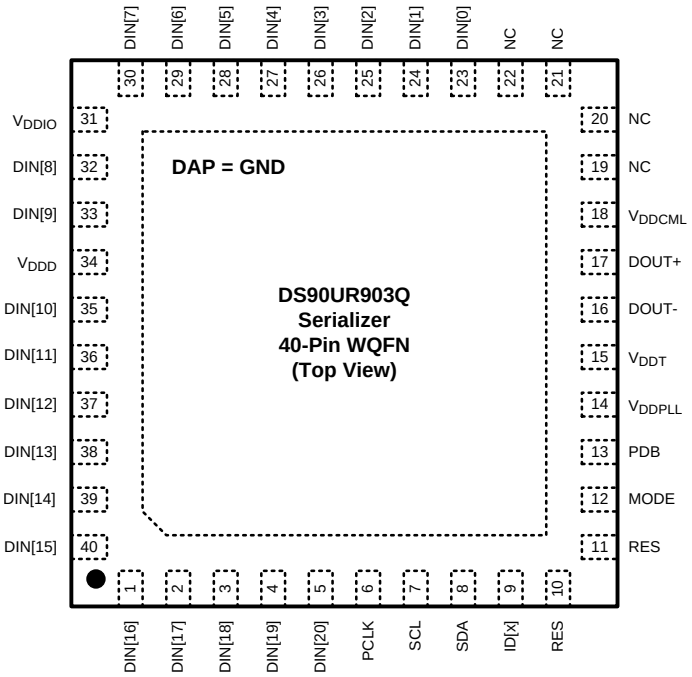
- Added data sheet flow and layout to conform with new TI standards. Added the following sections: Application and Implementation; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information ... 1
- Added additional thermal charateristics ... 7
- Changed test condition V_{in} to V_{ddio} ... 7
- Added power up sequencing information and timing diagram. ... 29
- Added application graphics of the serializer CML output. ... 30

Changes from Revision A (April 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 30

5 Pin Configuration and Functions

40 Pin Serializer – DS90UR903Q
Package RTA
Top View



DS90UR903Q Serializer Pin Functions

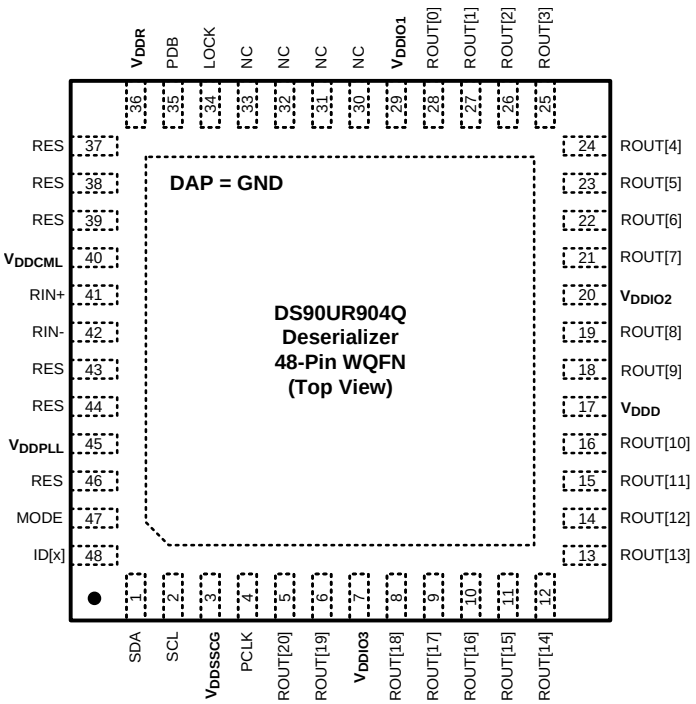
PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
LVCMOS PARALLEL INTERFACE			
DIN[20:0]	5, 4, 3, 2, 1, 40, 39, 38, 37, 36, 35, 33, 32, 30, 29, 28, 27, 26, 25, 24, 23	Inputs, LVCMOS w/ pull down	Parallel data inputs.
PCLK	6	Input, LVCMOS w/ pull down	Pixel Clock Input Pin. Strobe edge set by TRFB control register.
SERIAL CONTROL BUS - I^2C COMPATIBLE			
SCL	7	Input, Open Drain	Clock line for the serial control bus communication SCL requires an external pull-up resistor to V_{DDIO}.
SDA	8	Input/Output, Open Drain	Data line for the serial control bus communication SDA requires an external pull-up resistor to V_{DDIO}.
MODE	12	Input, LVCMOS w/ pull down	I^2C Mode select MODE = H, -**REQUIRED**. The MODE pin must be set HIGH to allow I^2C configuration of the serializer.
ID[x]	9	Input, analog	Device ID Address Select Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See Table 1
CONTROL AND CONFIGURATION			
PDB	13	Input, LVCMOS w/ pull down	Power down Mode Input Pin. PDB = H, Serializer is enabled and is ON. PDB = L, Serailizer is in Power Down mode. When the Serializer is in Power Down, the PLL is shutdown, and IDD is minimized. Programmed control register data are NOT retained and reset to default values
RES	10, 11	Input, LVCMOS w/ pull down	Reserved. This pin MUST be tied LOW.
NC	22, 21, 20, 19		No Connect

DS90UR903Q Serializer Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
FPD-LINK II INTERFACE			
DOUT+	17	Output, CML	Non-inverting differential output. The interconnect must be AC Coupled with a 100 nF capacitor.
DOUT-	16	Output, CML	Inverting differential output. The interconnect must be AC Coupled with a 100 nF capacitor.
POWER AND GROUND(1)			
VDDPLL	14	Power, Analog	PLL Power, 1.8V ±5%
VDDT	15	Power, Analog	Tx Analog Power, 1.8V ±5%
VDDCML	18	Power, Analog	CML Power, 1.8V ±5%
VDDD	34	Power, Digital	Digital Power, 1.8V ±5%
VDDIO	31	Power, Digital	Power for I/O stage. The single-ended inputs and SDA, SCL are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8V ±5% or 3.3V ±10%
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the ground plane (GND) with at least 16 vias.

(1) See Power Up Requirements and PDB PIN.

48 Pin Deserializer - DS90UR904Q
Package RHS
Top View



DS90UR904Q Deserializer Pin Descriptions

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
LVCMOS PARALLEL INTERFACE			
ROUT[20:0]	5, 6, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 26, 27, 28	Outputs, LVCMOS	Parallel data outputs.
PCLK	4	Output, LVCMOS	Pixel Clock Output Pin. Strobe edge set by RRFB control register.
SERIAL CONTROL BUS - I^2C COMPATIBLE			
SCL	2	Input, Open Drain	Clock line for the serial control bus communication SCL requires an external pull-up resistor to V_{DDIO}.
SDA	1	Input/Output, Open Drain	Data line for the serial control bus communication SDA requires an external pull-up resistor to V_{DDIO}.
MODE	47	Input, LVCMOS w/ pull up	I^2C Mode select MODE = H -**REQUIRED**. The MODE pin must be set HIGH to allow I^2C configuration of the deserializer.
ID[x]	9	Input, analog	Device ID Address Select Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See Table 2
CONTROL AND CONFIGURATION			
PDB	35	Input, LVCMOS w/ pull down	Power down Mode Input Pin. PDB = H, Deserializer is enabled and is ON. PDB = L, Deserializer is in Power Down mode. When the Deserializer is in Power Down. Programmed control register data are NOT retained and reset to default values.
LOCK	34	Output, LVCMOS	LOCK Status Output Pin. LOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL control register. May be used as Link Status.
RES	37, 38, 39, 43, 44, 46	-	Reserved. Pin 46: This pin MUST be tied LOW. Pin 37, 43, 44: Leave pin open. Pins 38, 39: Route to test point or leave open if unused.
NC	30, 31, 32, 33		No Connect
FPD-LINK II INTERFACE			
RIN+	41	Input, CML	Noninverting differential input. The interconnect must be AC Coupled with a 100 nF capacitor.
RIN-	42	Inputt, CML	Inverting differential input. The interconnect must be AC Coupled with a 100 nF capacitor.
POWER AND GROUND (1)			
VDDSSCG	3	Power, Digital	SSCG Power, 1.8V ±5% Power supply must be connected regardless if SSCG function is in operation.
VDDIO1/2/3	29, 20, 7	Power, Digital	LVCMOS I/O Buffer Power, The single-ended outputs and control input are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8V ±5% or 3.3V ±10%
VDDD	17	Power, Digital	Digital Core Power, 1.8V ±5%
VDDR	36	Power, Analog	Rx Analog Power, 1.8V ±5%
VDDCML	40	Power, Analog	1.8V ±5%
VDDPLL	45	Power, Analog	PLL Power, 1.8V ±5%
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the ground plane (GND) with at least 16 vias.

(1) See Power Up Requirements and PDB PIN.

6 Specifications

6.1 Absolute Maximum Ratings (1) (2)

PARAMETER	MIN	MAX	UNIT
Supply Voltage – V_{DDn} (1.8V)	−0.3	+2.5	V
Supply Voltage – V_{DDIO}	−0.3	+4.0V	V
LVCMOS Input Voltage I/O Voltage	−0.3	(VDDIO + 0.3V)	V
CML Driver I/O Voltage (V_{DD})	−0.3	(V_{DD} + 0.3V)	V
CML Receiver I/O Voltage (V_{DD})	−0.3	(V_{DD} + 0.3V)	V
Junction Temperature		+150	°C
Maximum Package Power Dissipation Capacity		$1/\theta_{JA}$ above +25°	°C/W

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional; the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	-8	+8	kV
		Charged device model (CDM), per AEC Q100-011	-1	+1	
		Machine Model (MM)	-250	+250	V
ESD Rating (IEC 61000-4-2) R_D = 330Ω, C_S = 150pF		Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	-25	+25	kV
		Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	-10	+10	
ESD Rating (ISO10605) R_D = 330Ω, C_S = 150/330pF R_D = 2KΩ, C_S = 150/330pF		Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	-15	+15	
		Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	-10	+10	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply Voltage (V_{DDn})		1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO}) (1.8V)		1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO}) (3.3V)		3.0	3.3	3.6	V
Supply Noise	V_{DDn} (1.8V)			25	mVp-p
	V_{DDIO} (1.8V)			25	mVp-p
	V_{DDIO} (3.3V)			50	mVp-p
Operating Free Air Temperature (T_A)		-40	+25	+105	°C
PCLK Clock Frequency		10		43	MHz

6.4 Thermal Information(1)

THERMAL METRIC(2)		DS90UR903Q 40L WQFN	DS90UR904Q 48L WQFN	UNIT
		RTA	RHS	
		40 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.9	30.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.5	11.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.1	6.9	
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.1	
ψ_{JB}	Junction-to-board characterization parameter	8.1	6.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	2.4	

(1) For soldering specifications, see SNOA549
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics(1) (2) (3)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS 3.3V I/O (SER INPUTS, DES OUTPUTS, CONTROL INPUTS AND OUTPUTS)						
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0V to 3.6V	2.0		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0V to 3.6V	GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V V_{DDIO} = 3.0V to 3.6V	-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OH} = -4 mA	2.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OL} = +4 mA	GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		-39		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	-20	±1	+20	µA
LVCMOS DC SPECIFICATIONS 1.8V I/O (SER INPUTS, DES OUTPUTS, CONTROL INPUTS AND OUTPUTS)						
V_{IH}	High Level Input Voltage	V_{DDIO} = 1.71V to 1.89V	0.65 V_{DDIO}		V_{DDIO} +0.3	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 1.71V to 1.89V	GND		0.35 V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or 1.89V V_{DDIO} = 1.71V to 1.89V	-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OH} = −4 mA	V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OL} = +4 mA	GND		0.45	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		-20		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	-20	±1	+20	µA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
(3) Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

Electrical Characteristics[1] [2] [3] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CML DRIVER DC SPECIFICATIONS (DOUT+, DOUT-)							
$\|V_{OD}\|$	Output Differential Voltage	R_T = 100Ω, Figure 5		268	340	412	mV
ΔV_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω			1	50	mV
V_{OS}	Output Differential Offset Voltage	R_L = 100Ω Figure 5		$V_{DD\ (MIN)}$ - $V_{OD\ (MAX)}$	V_{DD} - V_{OD}	$V_{DD\ (MAX)}$ - $V_{OD\ (MIN)}$	V
ΔV_{OS}	Offset Voltage Unbalance	R_L = 100Ω			1	50	mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V			-27		mA
R_T	Differential Internal Termination Resistance	Differential across DOUT+ and DOUT-		80	100	120	Ω
CML RECEIVER DC SPECIFICATIONS (RIN+, RIN-)							
V_{TH}	Differential Threshold High Voltage	Figure 7				+90	mV
V_{TL}	Differential Threshold Low Voltage			-90			
V_{IN}	Differential Input Voltage Range	RIN+ - RIN-		180			mV
I_{IN}	Input Current	V_{IN} = V_{DD} or 0V, V_{DD} = 1.89V		-20	±1	+20	µA
R_T	Differential Internal Termination Resistance	Differential across RIN+ and RIN-		80	100	120	Ω
SER/DES SUPPLY CURRENT *DIGITAL, PLL, AND ANALOG VDD							
I_{DDT}	Serializer (Tx) VDDn Supply Current (includes load current)	R_T = 100Ω WORST CASE pattern Figure 2	VDDn = 1.89V PCLK = 43 MHz Default Registers		62	90	mA
		R_T = 100Ω RANDOM PRBS-7 pattern			55		
I_{DDIOT}	Serializer (Tx) VDDIO Supply Current (includes load current)	R_T = 100Ω WORST CASE pattern Figure 2	VDDIO = 1.89V PCLK = 43 MHz Default Registers		2	5	mA
			VDDIO = 3.6V PCLK = 43 MHz Default Registers		7	15	
I_{DDTZ}	Serializer (Tx) Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	V_{DDn} = 1.89V		370	775	µA
I_{DDIOTZ}			V_{DDIO} = 1.89V		55	125	
			V_{DDIO} = 3.6V		65	135	

Electrical Characteristics(1) (2) (3) (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DDR}	Deserializer (Rx) VDDn Supply Current (includes load current)	V_{DDn} = 1.89V C_L = 8 pF WORST CASE Pattern Figure 2	PCLK = 43 MHz SSCG[3:0] = ON Default Registers		60	96	mA
		V_{DDn} = 1.89V C_L = 8 pF RANDOM PRBS-7 Pattern	PCLK = 43 MHz Default Registers		53		
I_{DDIOR}	Deserializer (Rx) VDDIO Supply Current (includes load current)	V_{DDIO} = 1.89V C_L = 8 pF WORST CASE Pattern Figure 2	PCLK = 43 MHz Default Registers		21	32	
		V_{DDIO} = 3.6V C_L = 8 pF WORST CASE Pattern	PCLK = 43 MHz Default Registers		49	83	
I_{DDRZ}	Deserializer (Rx) Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	V_{DDn} = 1.89V		42	400	µA
I_{DDIORZ}			V_{DDIO} = 1.89V		8	40	
			V_{DDIO} = 3.6V		350	800	

6.6 Recommended Serializer Timing for PCLK(1)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TCP}	Transmit Clock Period	10 MHz – 43 MHz	23.3	T	100	ns
t_{TCIH}	Transmit Clock Input High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Clock Input Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	PCLK Input Transition Time Figure 8		0.5		3	ns
f_{OSC}	Internal oscillator clock source			25		MHz

(1) Recommended Input Timing Requirements are input specifications and not tested in production.

6.7 Serial Control Bus AC Timing Specifications (SCL, SDA) - I²C Compliant (See Figure 1)

Over recommended supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RECOMMENDED INPUT TIMING REQUIREMENTS (1)						
f_{SCL}	SCL Clock Frequency		>0		100	kHz
t_{LOW}	SCL Low Period	f_{SCL} = 100 kHz	4.7			µs
t_{HIGH}	SCL High Period		4.0			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition		4.0			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition		4.7			µs
$t_{HD:DAT}$	Data Hold Time		0		3.45	µs
$t_{SU:DAT}$	Data Set Up Time		250			ns
$t_{SU:STO}$	Set Up Time for STOP Condition		4.0			µs
t_r	SCL & SDA Rise Time				1000	ns
t_f	SCL & SDA Fall Time				300	ns
C_b	Capacitive load for bus				400	pF
SWITCHING CHARACTERISTICS (2)						
$t_{HD:DAT}$	Data Hold Time		0		3.45	µs
$t_{SU:DAT}$	Data Set Up Time		250			ns
t_f	SCL & SDA Fall Time				300	ns

(1) Recommended Input Timing Requirements are input specifications and not tested in production.
(2) Specification is ensured by design.

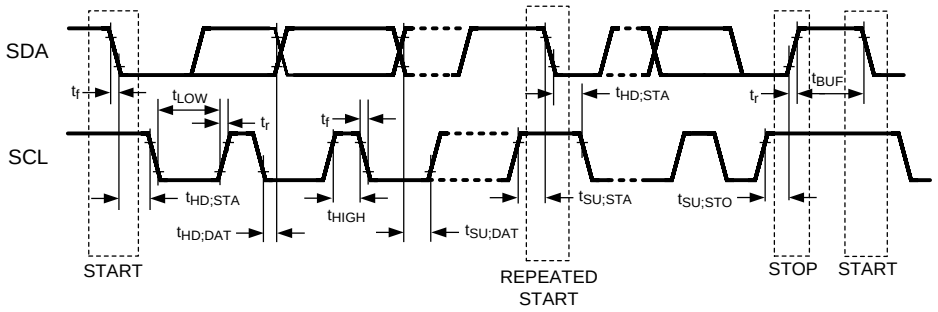


Figure 1. Serial Control Bus Timing

6.8 Serial Control Bus DC Characteristics (SCL, SDA) - I²C Compliant

Over recommended supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Level	SDA and SCL	0.7 x V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3 x V_{DDIO}	V
V_{HY}	Input Hysteresis	SDA and SCL		>50		mV
I_{OZ}	TRI-STATE Output Current	PDB = 0V V_{OUT} = 0V or V_{DD}	-20	±1	+20	µA
I_{IN}	Input Current	SDA or SCL, Vin = V_{DDIO} or GND	-20	±1	+20	µA
C_{IN}	Input Pin Capacitance			<5		pF
V_{OL}	Low Level Output Voltage	SCL and SDA V_{DDIO} = 3.0V I_{OL} = 1.5mA			0.36	V
		SCL and SDA V_{DDIO} = 1.71V I_{OL} = 1mA			0.36	V

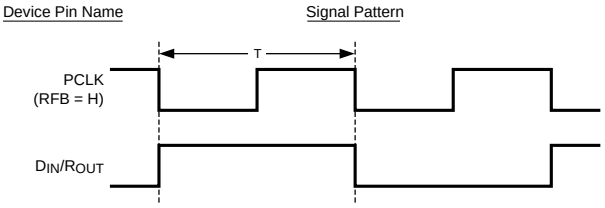


Figure 2. "Worst Case" Test Pattern

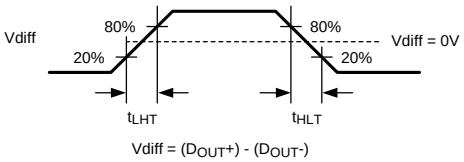


Figure 3. Serializer CML Output Load and Transition Times

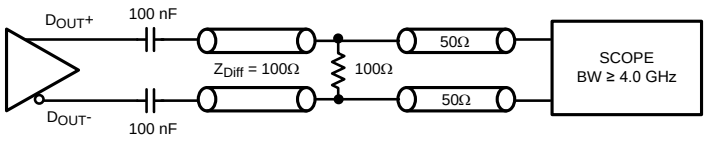


Figure 4. Serializer CML Output Load and Transition Times

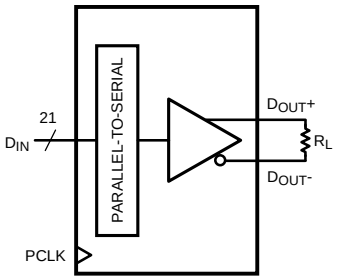


Figure 5. Serializer VOD DC Diagram

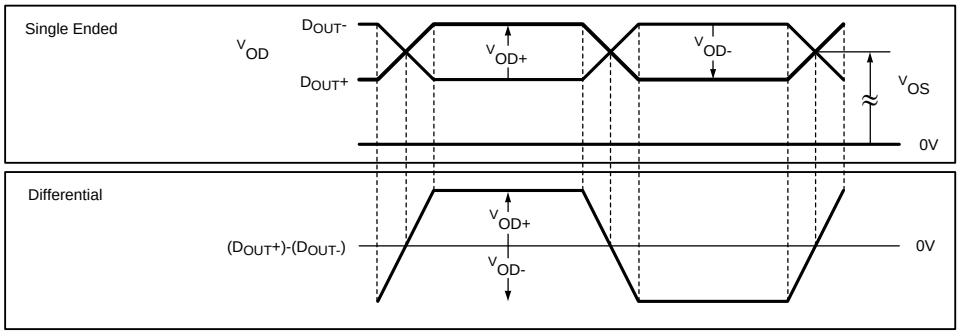


Figure 6. Serializer VOD DC Diagram

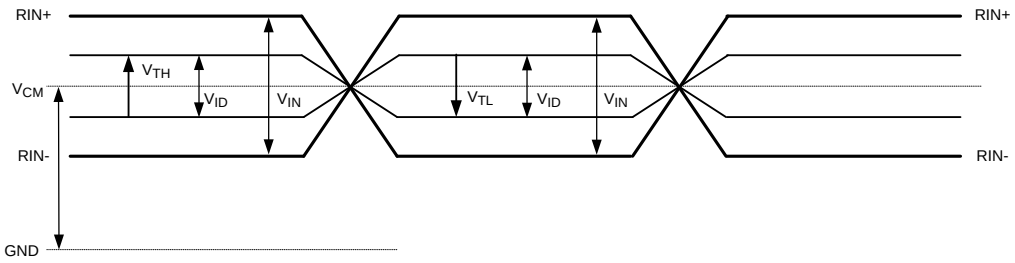


Figure 7. Differential VTH/VTL Definition Diagram

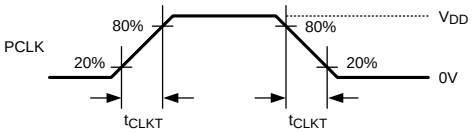


Figure 8. Serializer Input Clock Transition Times

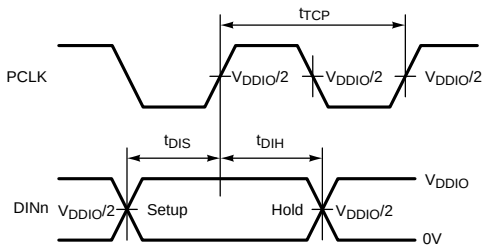


Figure 9. Serializer Setup/Hold Times

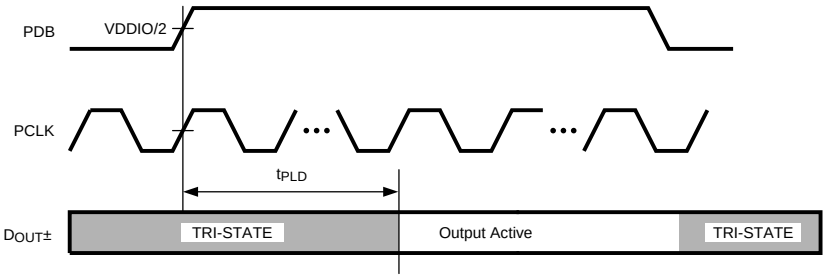


Figure 10. Serializer Data Lock Time

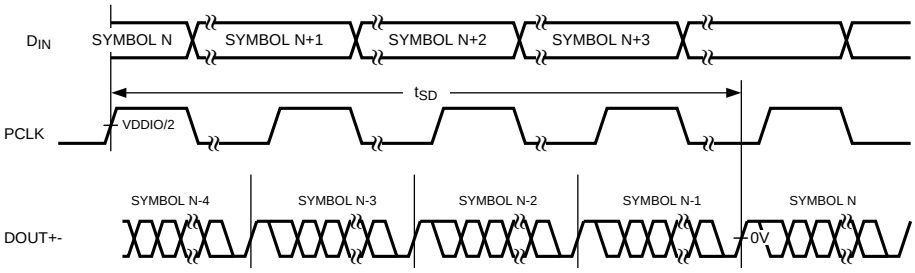


Figure 11. Serializer Delay

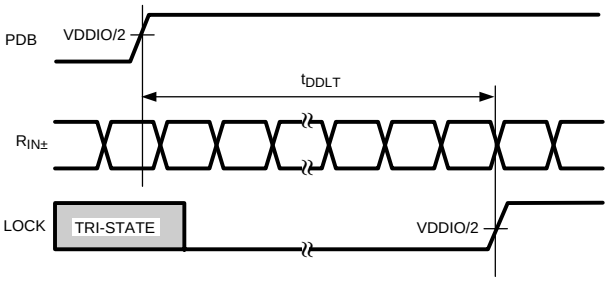


Figure 12. Deserializer Data Lock Time

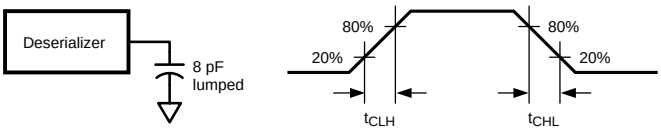


Figure 13. Deserializer LVCMOS Output Load and Transition Times

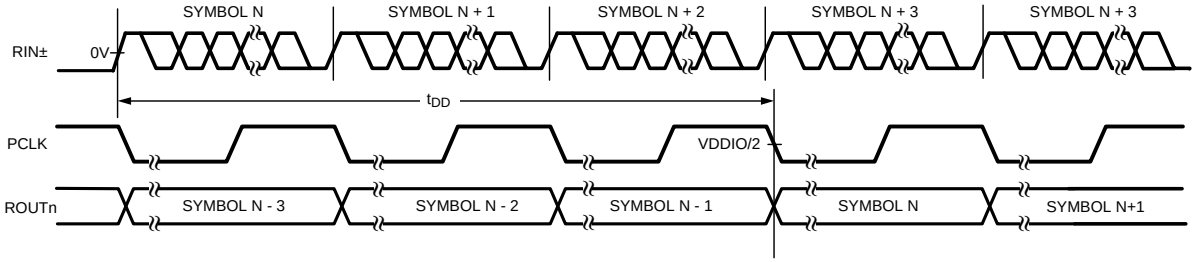


Figure 14. Deserializer Delay

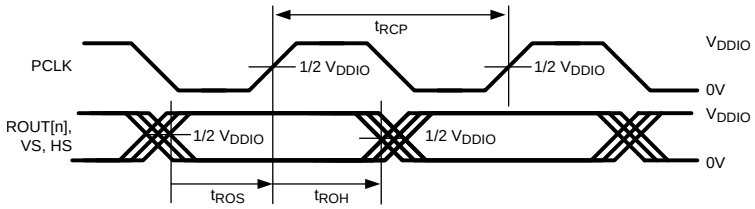


Figure 15. Deserializer Output Setup/Hold Times

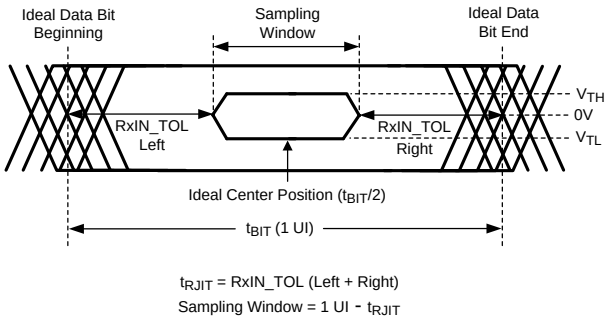


Figure 16. Receiver Input Jitter Tolerance

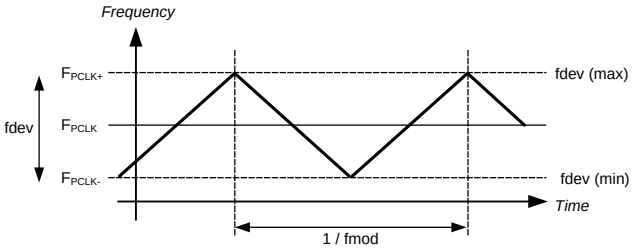


Figure 17. Spread Spectrum Clock Output Profile

6.9 Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LHT}	CML Low-to-High Transition Time	R_L = 100Ω Figure 3		150	330	ps
t_{HLT}	CML High-to-Low Transition Time	R_L = 100Ω Figure 3		150	330	ps
t_{DIS}	Data Input Setup to PCLK	Serializer Data Inputs Figure 9	2.0			ns
t_{DIH}	Data Input Hold from PCLK		2.0			ns
t_{PLD}	Serializer PLL Lock Time	R_L = 100Ω (1) (2)		1	2	ms
t_{SD}	Serializer Delay	R_T = 100Ω PCLK = 10–43 MHz Register 0x03h b[0] (TRFB = 1) Figure 11	6.386T + 5	6.386T + 12	6.386T + 19.7	ns
t_{JIND}	Serializer Output Deterministic Jitter	Serializer output intrinsic deterministic jitter . Measured (cycle-cycle) with PRBS-7 test pattern PCLK = 43 MHz (3) (4)		0.13		UI
t_{JINR}	Serializer Output Random Jitter	Serializer output intrinsic random jitter (cycle-cycle). Alternating-1,0 pattern. PCLK = 43 MHz (3) (4)		0.04		UI
t_{JINT}	Peak-to-peak Serializer Output Jitter	Serializer output peak-to-peak jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input. Measured (cycle-cycle) with PRBS-7 test pattern. PCLK = 43 MHz (3) (4)		0.396		UI
λ_{STXBW}	Serializer Jitter Transfer Function -3 dB Bandwidth	PCLK = 43 MHz Default Registers Figure 18 (3)		1.90		MHz
δ_{STX}	Serializer Jitter Transfer Function (Peaking)	PCLK = 43 MHz Default Registers Figure 18 (3)		0.944		dB
δ_{STXf}	Serializer Jitter Transfer Function (Peaking Frequency)	PCLK = 43 MHz Default Registers Figure 18 (3)		500		kHz

(1) t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK
(2) Specification is ensured by design.
(3) Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.

6.10 Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
t_{RCP}	Receiver Output Clock Period	$t_{RCP} = t_{TCP}$	PCLK	23.3	T	100	ns
t_{PDC}	PCLK Duty Cycle	Default Registers SSCG[3:0] = OFF	PCLK	45	50	55	%
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71V to 1.89V or 3.0 to 3.6V, C_L = 8 pF (lumped load) Default Registers Figure 13 (1)	PCLK	1.3	2.0	2.8	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1.3	2.0	2.8	
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71V to 1.89V or 3.0 to 3.6V, C_L = 8 pF (lumped load) Default Registers Figure 13 (1)	Deserializer ROUTn Data Outputs	1.6	2.4	3.3	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1.6	2.4	3.3	
t_{ROS}	ROUT Setup Data to PCLK	V_{DDIO}: 1.71V to 1.89V or 3.0V to 3.6V, C_L = 8 pF (lumped load) Default Registers	Deserializer ROUTn Data Outputs	0.38T	0.5T		ns
t_{ROH}	ROUT Hold Data to PCLK			0.38T	0.5T		
t_{DD}	Deserializer Delay	Default Registers Register 0x03h b[0] (RRFB = 1) Figure 14	10 MHz–43 MHz	4.571T + 8	4.571T + 12	4.571T + 16	ns
t_{DDLT}	Deserializer Data Lock Time	Figure 12 (2)	10 MHz–43 MHz			10	ms
t_{RJIT}	Receiver Input Jitter Tolerance	Figure 16, Figure 19 (3) (4)	43 MHz		0.53		UI
t_{RCJ}	Receiver Clock Jitter	PCLK SSCG[3:0] = OFF (1) (5)	10 MHz		300	550	ps
			43 MHz		120	250	
t_{DPJ}	Deserializer Period Jitter	PCLK SSCG[3:0] = OFF (1) (6)	10 MHz		425	600	ps
			43 MHz		320	480	
t_{DCCJ}	Deserializer Cycle-to-Cycle Clock Jitter	PCLK SSCG[3:0] = OFF (1) (7)	10 MHz		320	500	ps
			43 MHz		300	500	
fdev	Spread Spectrum Clocking Deviation Frequency	LVCMOS Output Bus SSC[3:0] = ON Figure 17	20 MHz–43 MHz		±0.5% to ±2.0%		%
fmod	Spread Spectrum Clocking Modulation Frequency		20 MHz–43 MHz		9 kHz to 66 kHz		kHz

(1) Specification is ensured by characterization and is not tested in production.
(2) t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK
(3) UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.
(4) t_{RJIT} max (0.61UI) is limited by instrumentation and actual t_{RJIT} of in-band jitter at low frequency (<2 MHz) is greater 1 UI.
(5) t_{DCJ} is the maximum amount of jitter measured over 30,000 samples based on Time Interval Error (TIE).
(6) t_{DPJ} is the maximum amount the period is allowed to deviate measured over 30,000 samples.
(7) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles measured over 30,000 samples.

6.11 Typical Characteristics

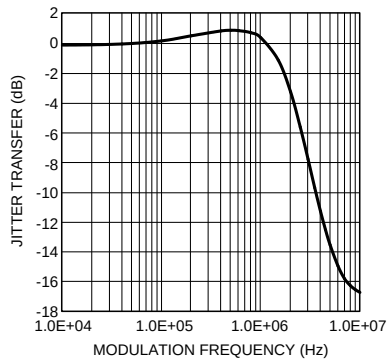


Figure 18. Typical Serializer Jitter Transfer Function Curve at 43 MHz

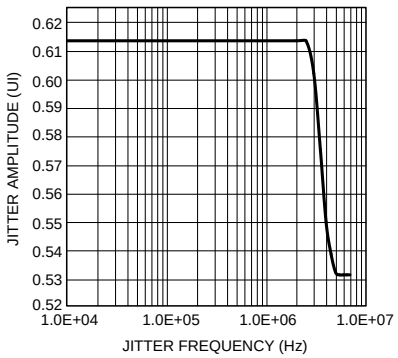


Figure 19. Typical Deserializer Input Jitter Tolerance Curve at 43 MHz

7 Detailed Description

7.1 Overview

The DS90UR903Q/904Q FPD-Link II chipset is intended for video display applications. The Serializer/ Deserializer chipset operates from a 10 MHz to 43 MHz pixel clock frequency. The DS90UR903Q transforms a 21-bit wide parallel LVCMOS data bus into a single high-speed differential pair. The high-speed serial bit stream contains an embedded clock and DC-balance information which enhances signal quality to support AC coupling. The DS90UR904Q receives the single serial data stream and converts it back into a 21-bit wide parallel data bus.

7.2 Functional Block Diagram

7.2.1 Typical Application Diagram

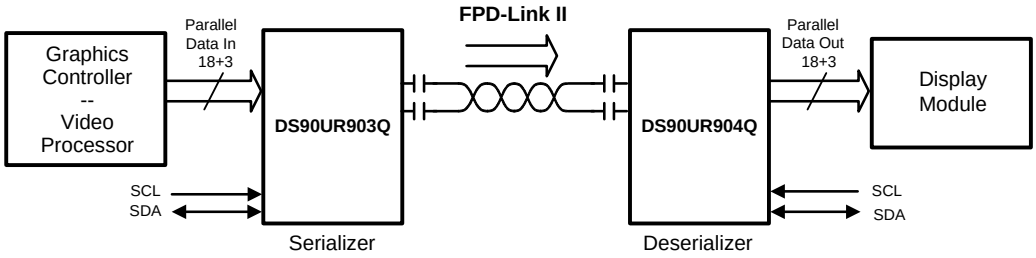


Figure 20. Typical Application Circuit

7.2.2 Block Diagrams

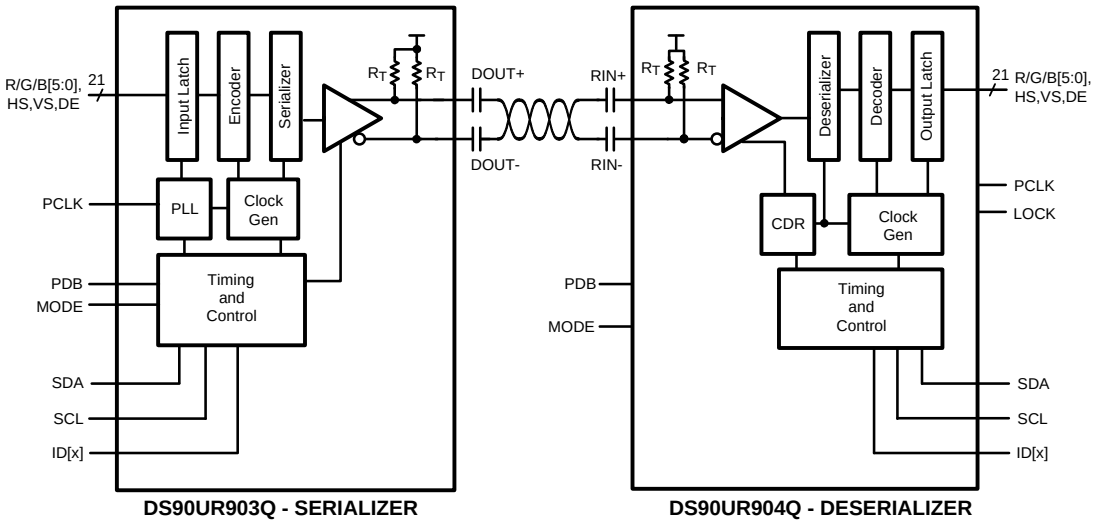


Figure 21. Block Diagram

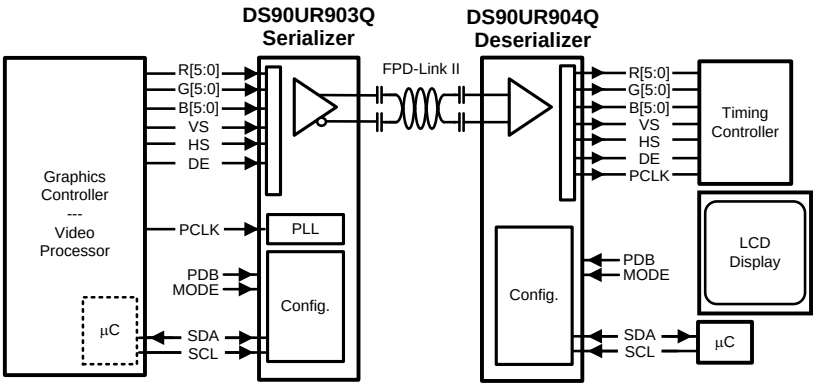


Figure 22. Application Block Diagram

7.3 Feature Description

7.3.1 Serial Frame Format

The DS90UR903Q/904Q chipset will transmit and receive a pixel of data in the following format:

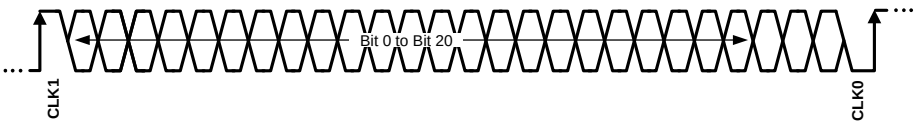


Figure 23. Serial Bitstream for 28-bit Symbol

The High Speed Serial Channel is a 28-bit symbol composed of 21 bits of data containing video data & control information transmitted from Serializer to Deserializer. CLK1 and CLK0 represent the embedded clock in the serial stream. CLK1 is always HIGH and CLK0 is always LOW. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

7.3.2 Signal Quality Enhancers

7.3.2.1 Des - Receiver Input Equalization (EQ)

The receiver inputs provided input equalization filter in order to compensate for loss from the media. The level of equalization is controlled via register setting.

7.3.3 Emi Reduction

7.3.3.1 Des - Receiver Staggered Output

The Receiver staggered outputs allows for outputs to switch in a random distribution of transitions within a defined window. Outputs transitions are distributed randomly. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

7.3.3.2 Des Spread Spectrum Clocking

The DS90UR904Q parallel data and clock outputs have programmable SSCG ranges from 9 kHz–66 kHz and ±0.5%–±2% from 20 MHz to 43 MHz. The modulation rate and modulation frequency variation of output spread is controlled through the SSC control registers.

7.4 Device Functional Modes

7.4.1 LVCMOS VDDIO Option

1.8V or 3.3V SER Inputs and DES Outputs are user selectable to provide compatibility with 1.8V and 3.3V system interfaces.

7.4.2 Powerdown

The SER has a PDB input pin to ENABLE or Powerdown the device. The modes can be controlled by the host and is used to disable the Link to save power when the remote device is not operational. An auto mode is also available. In this mode, the PDB pin is tied High and the SER switches over to an internal oscillator when the PCLK stops or not present. When a PCLK starts again, the SER will then lock to the valid input PCLK and transmits the data to the DES. In powerdown mode, the high-speed driver outputs are static (High).

The DES has a PDB input pin to ENABLE or Powerdown the device. This pin can be controlled by the system and is used to disable the DES to save power. An auto mode is also available. In this mode, the PDB pin is tied High and the DES will enter powerdown when the serial stream stops. When the serial stream starts up again, the DES will lock to the input stream and assert the LOCK pin and output valid data. In powerdown mode, the Data and PCLK outputs are set by the OSS_SEL control register.

7.4.3 Pixel Clock Edge Select (TRFB/RRFB)

The TRFB/RRFB selects which edge of the Pixel Clock is used. For the SER, this register determines the edge that the data is latched on. If TRFB register is 1, data is latched on the Rising edge of the PCLK. If TRFB register is 0, data is latched on the Falling edge of the PCLK. For the DES, this register determines the edge that the data is strobed on. If RRFB register is 1, data is strobed on the Rising edge of the PCLK. If RRFB register is 0, data is strobed on the Falling edge of the PCLK.

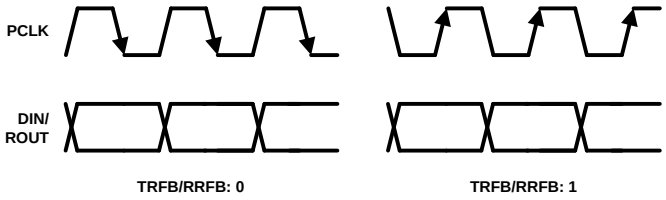


Figure 24. Programmable PCLK Strobe Select

7.5 Programming

7.5.1 Description of Serial Control Bus

An integrated I^2C slave controller is embedded in each of the DS90UR903Q Serializer and DS90UR904Q Deserializer. It must be used to access and program the extra features embedded within the configuration registers. Refer to Table 3 and Table 4 for details of control registers.

7.5.2 ID[X] Address Decoder

The ID[x] pin is used to decode and set the physical slave address of the Serializer/Deserializer (I^2C only) to allow up to six devices on the bus using only a single pin. The pin sets one of six possible addresses for each Serializer/Deserializer device. The pin must be pulled to VDD (1.8V, NOT VDDIO)) with a 10 kΩ resistor and a pull down resistor (RID) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 0.1% worst case (0.2% total tolerance).

Programming (continued)

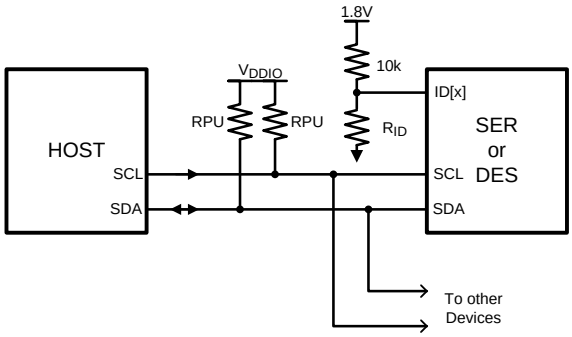


Figure 25. Serial Control Bus Connection

Table 1. ID[x] Resistor Value – DS90UR903Q

ID[x] RESISTOR VALUE - DS90UR903Q Ser		
RESISTOR RID Ω (±0.1%)	**ADDRESS 7'b(1)**	**ADDRESS 8'b 0 APPENDED (WRITE)**
0 GND	7b' 101 1000 (h'58)	8b' 1011 0000 (h'B0)
2.0k	7b' 101 1001 (h'59)	8b' 1011 0010 (h'B2)
4.7k	7b' 101 1010 (h'5A)	8b' 1011 0100 (h'B4)
8.2k	7b' 101 1011 (h'5B)	8b' 1011 0110 (h'B6)
12.1k	7b' 101 1100 (h'5C)	8b' 1011 1000 (h'B8)
39.0k	7b' 101 1110 (h'5E)	8b' 1011 1100 (h'BC)

(1) Specification is ensured by design.

Table 2. ID[x] Resistor Value – DS90UR904Q

ID[x] RESISTOR VALUE - DS90UR904Q Des		
RESISTOR RID Ω (±0.1%)	**ADDRESS 7'b(1)**	**ADDRESS 8'b 0 APPENDED (WRITE)**
0 GND	7b' 110 0000 (h'60)	8b' 1100 0000 (h'C0)
2.0k	7b' 110 0001 (h'61)	8b' 1100 0010 (h'C2)
4.7k	7b' 110 0010 (h'62)	8b' 1100 0100 (h'C4)
8.2k	7b' 110 0011 (h'63)	8b' 1101 0110 (h'C6)
12.1k	7b' 110 0100 (h'64)	8b' 1101 1000 (h'C8)
39.0k	7b' 110 0110 (h'66)	8b' 1100 1100 (h'CC)

(1) Specification is ensured by design.

7.6 Register Maps

Table 3. DS90UR903Q Control Registers

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0	I^2C Device ID	7:1	DEVICE ID	RW	0xB0'h	7-bit address of Serializer; 0x58'h (1011_000X'b) default
		0	SER ID SEL			0: Device ID is from ID[x] 1: Register I^2C Device ID overrides ID[x]
1	Reset	7:3	RESERVED		0x00'h	Reserved
		2	RESERVED	RW	0	Reserved
		1	DIGITAL RESET0	RW	0 self clear	1: Resets the device to default register values. Does not affect device I^2C Bus or Device ID
		0	DIGITAL RESET1	RW	0 self clear	1: Digital Reset, retains all register values
2	Reserved	7:0	RESERVED		0x20'h	Reserved
3	Reserved	7:6	RESERVED		11'b	Reserved
	VDDIO Control	5	VDDIO CONTOL	RW	1	Auto VDDIO detect Allows manual setting of VDDIO by register. 0: Disable 1: Enable (auto detect mode)
	VDDIO Mode	4	VDDIO MODE	RW	1	VDDIO voltage set Only used when VDDIOCONTROL = 0 0: 1.8V 1: 3.3V
	RESERVED	3	RESERVED	RW	1	Reserved
	RESERVED	2	RESERVED		0	Reserved
	PCLK_AUTO	1	PCLK_AUTO	RW	1	Switch over to internal 25 MHz Oscillator clock in the absence of PCLK 0: Disable 1: Enable
	TRFB	0	TRFB	RW	1	Pixel Clock Edge Select: 0: Parallel Interface Data is strobed on the Falling Clock TRFB 0 TRFB RW 1 Edge. 1: Parallel Interface Data is strobed on the Rising Clock Edge.
4	Reserved	7:0	RESERVED		0x80'h	Reserved
5	Reserved	7:0	RESERVED	RW	0x40'h	Reserved
6	Reserved	7:0	RESERVED	RW	0xC0'h	Reserved
7	Reserved	7:0	RESERVED	RW	0x00'h	Reserved
8	Reserved	7:0	RESERVED		0x00'h	Reserved
9	Reserved	7:0	RESERVED		0x01'h	Reserved
A	Reserved	7:0	RESERVED		0x00'h	Reserved
B	Reserved	7:0	RESERVED		0x00'h	Reserved
C	Reserved	7:3	RESERVED		0x00'h	Reserved
	PCLK Detect	2	PCLK DETECT	R	0	1: Valid PCLK detected 0: Valid PCLK not detected
	Reserved	3	RESERVED		0	Reserved
	Reserved	0	RESERVED	R	0	Reserved
D	Reserved	7:0	RESERVED		0x11'h	Reserved
E	Reserved	7:0	RESERVED		0x01'h	Reserved
F	Reserved	7:0	RESERVED		0x03'h	Reserved
10	Reserved	7:0	RESERVED		0x03'h	Reserved
11	Reserved	7:0	RESERVED		0x03'h	Reserved
12	Reserved	7:0	RESERVED		0x03'h	Reserved

Register Maps (continued)

Table 3. DS90UR903Q Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
13	General Purpose Control Reg	7:0	GPCR[7] GPCR[6] GPCR[5] GPCR[4] GPCR[3] GPCR[2] GPCR[1] GPCR[0]	RW	0x00'h	0: LOW 1: HIGH

Table 4. DS90UR904Q Control Registers

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0	I^2C Device ID	7:1	DEVICE ID	RW	0xC0'h	7-bit address of Deserializer; 0x60h (1100_000X) default
		0	DES ID SEL			0: Device ID is from ID[x] 1: Register I^2C Device ID overrides ID[x]
1	Reset	7:3	RESERVED		0x00'h	Reserved
		2	RESERVED	RW	0	Reserved
		1	DIGITALRESET0	RW	0 self clear	1: Resets the device to default register values. Does not affect device I^2C Bus or Device ID
		0	DIGITALRESET1	RW	0 self clear	1: Digital Reset, retains all register values
2	RESERVED	7:6	RESERVED		00'b	Reserved
	Auto Clock	5	AUTO_CLOCK	RW	0	1: Output PCLK or Internal 25 MHz Oscillator clock 0: Only PCLK when valid PCLK present
	OSS Select	4	OSS_SEL	RW	0	Output Sleep State Select 0: Outputs = TRI-STATE, when LOCK = L 1: Outputs = LOW , when LOCK = L
	SSCG	3:0	SSCG		0000'b	SSCG Select 0000: Normal Operation, SSCG OFF (default) 0001: fmod (kHz) PCLK/2168, fdev ±0.50% 0010: fmod (kHz) PCLK/2168, fdev ±1.00% 0011: fmod (kHz) PCLK/2168, fdev ±1.50% 0100: fmod (kHz) PCLK/2168, fdev ±2.00% 0101: fmod (kHz) PCLK/1300, fdev ±0.50% 0110: fmod (kHz) PCLK/1300, fdev ±1.00% 0111: fmod (kHz) PCLK/1300, fdev ±1.50% 1000: fmod (kHz) PCLK/1300, fdev ±2.00% 1001: fmod (kHz) PCLK/868, fdev ±0.50% 1010: fmod (kHz) PCLK/868, fdev ±1.00% 1011: fmod (kHz) PCLK/868, fdev ±1.50% 1100: fmod (kHz) PCLK/868, fdev ±2.00% 1101: fmod (kHz) PCLK/650, fdev ±0.50% 1110: fmod (kHz) PCLK/650, fdev ±1.00% 1111: fmod (kHz) PCLK/650, fdev ±1.50%

Table 4. DS90UR904Q Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
3	RESERVED	7:6	RESERVED		11'b	Reserved
	VDDIO Control	5	VDDIO CONTROL	RW	1	Auto voltage control 0: Disable 1: Enable (auto detect mode)
	VDDIO Mode	4	VDDIO MODE	RW	0	VDDIO voltage set 0: 1.8V 1: 3.3V
	RESERVED	3	RESERVED	RW	1	Reserved
	RESERVED	2	RESERVED	RW	0	Reserved
	RESERVED	1	RESERVED		0	Reserved
	RRFB	0	RRFB	RW	1	Pixel Clock Edge Select 0: Parallel Interface Data is strobed on the Falling Clock Edge 1: Parallel Interface Data is strobed on the Rising Clock Edge.
4	EQ Control	7:0	EQ	RW	0x00'h	EQ Gain 00'h = ~0.0 dB 01'h = ~4.5 dB 03'h = ~6.5 dB 07'h = ~7.5 dB 0F'h = ~8.0 dB 1F'h = ~11.0 dB 3F'h = ~12.5 dB FF'h = ~14.0 dB
5	RESERVED	7:0	RESERVED		0x00'h	Reserved
6	RESERVED	7	RESERVED		0	Reserved
	RESERVED	6:4	RESERVED	RW	000'b	Reserved
	RESERVED	3:0	RESERVED	RW	1111'b	Reserved
7	RESERVED	7:0	RESERVED	RW	0xB0'h	Reserved
8:17	RESERVED	7:0	RESERVED	RW	0x00'h	Reserved
18	RESERVED	7:0	RESERVED		0x00'h	Reserved
19	RESERVED	7:0	RESERVED		0x01'h	Reserved
1A	RESERVED	7:0	RESERVED		0x00'h	Reserved
1B	RESERVED	7:0	RESERVED		0x00'h	Reserved
1C	RESERVED	7:3	RESERVED		0x00'h	Reserved
	RESERVED	2	RESERVED		0	Reserved
	Signal Detect Status	1		R	0	0: Active signal not detected 1: Active signal detected
	LOCK Pin Status	0		R	0	0: CDR/PLL Unlocked 1: CDR/PLL Locked
1D	Reserved	7:0	RESERVED		0x17'h	Reserved
1E	Reserved	7:0	RESERVED		0x07'h	Reserved
1F	Reserved	7:0	RESERVED		0x01'h	Reserved
20	Reserved	7:0	RESERVED		0x01'h	Reserved
21	Reserved	7:0	RESERVED		0x01'h	Reserved
22	Reserved	7:0	RESERVED		0x01'h	Reserved
23	General Purpose Control Reg	7:0	GPCR[7] GPCR[6] GPCR[5] GPCR[4] GPCR[3] GPCR[2] GPCR[1] GPCR[0]	RW	0x00'h	0: LOW 1: HIGH

Table 4. DS90UR904Q Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
24	RESERVED	0	RESERVED	RW	0	Reserved
25	RESERVED	7:0	RESERVED	R	0x00'h	Reserved
26	RESERVED	7:6	RESERVED	RW	00'b	Reserved
		5:0	RESERVED	RW	0	Reserved

8 Application and Implementation

8.1 Application Information

The DS90UR903Q/904Q chipset is intended for interface between a host (graphics processor) and a Display. It supports a 21 bit parallel video bus for 18-bit color depth (RGB666) display format. In a RGB666 configuration, 18 color bits (R[5:0], G[5:0], B[5:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link.

The DS90UR903Q Serializer accepts a 21-bit parallel data bus. The parallel data is converted into a single differential link. The DS90UR904Q Deserializer extracts the clock/control information from the incoming data stream and reconstructs the 21-bit parallel data.

Camera applications are also supported by the DS90UR903Q/904Q chipset. The host controller/processsor is connected to the deserializer, while the CMOS image sensor provides data to the serializer.

8.2 Typical Applications

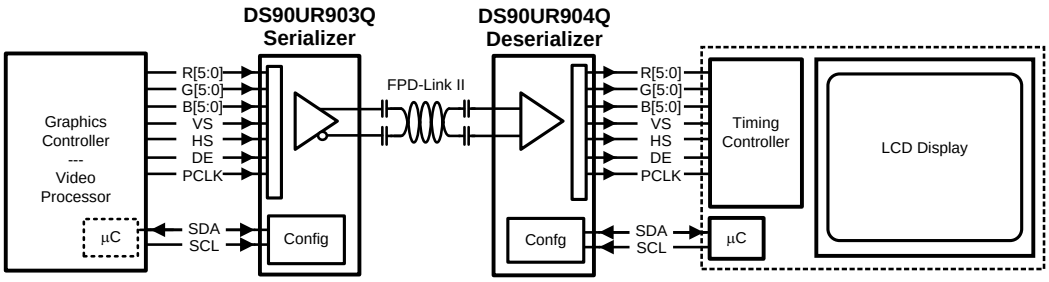


Figure 26. Typical Display System Diagram

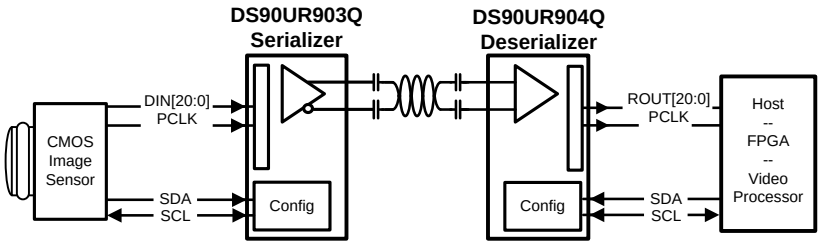


Figure 27. Typical Camera System Diagram

8.2.1 Design Requirements

For the typical design applications, use the following as input parameters.

Table 5. Design Parameters

Design Parameter	Example Value
VDDIO	1.8 V or 3.3 V
VDDn	1.8 V
AC Coupling Capacitor for DOUT± and RIN±	100 nF
PCLK Frequency	43 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Typical Application Connection

Figure 28 shows a typical connection of the DS90UR903Q Serializer for an 18-bit application. The CML outputs require 0.1 µF AC coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply Terminals. System GPO (General Purpose Output) signals control the PDB and MODE Terminals. The interface to the host is with 1.8 V LVCMOS levels, thus the VDDIO Terminal is connected also to the 1.8V rail. The optional Serial Bus control is used in this example, thus SCL and SDA are connected to the system and the ID[x] Terminal is connected to a resistor divider.

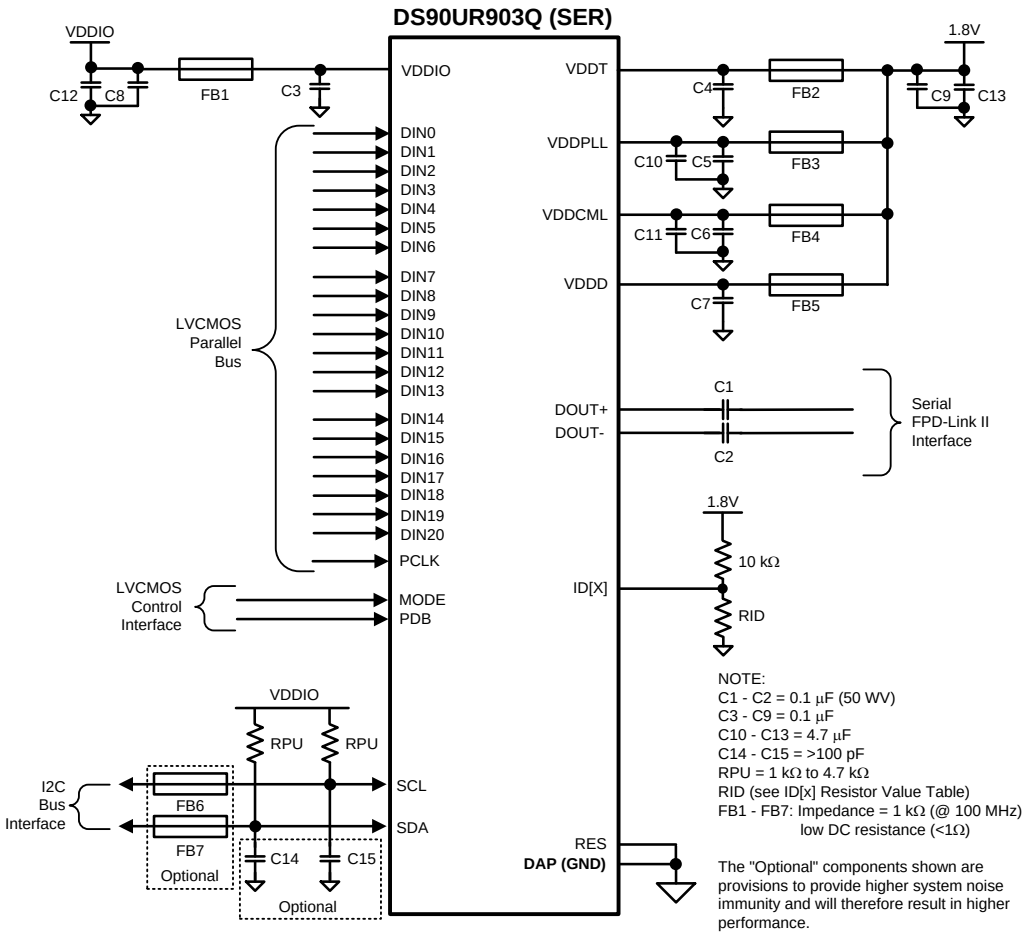


Figure 28. DS90UR903Q Typical Connection Diagram — Pin Control 40-Pin WQFN (RTA Package)

Figure 29 shows a typical connection of the DS90UR904Q Deserializer for an 18-bit application. The CML inputs utilize 0.1 µF coupling capacitors to the line and the receiver provides internal termination. Bypass capacitors are placed near the power supply Terminals. System GPO (General Purpose Output) signals control the PDB and the MODE Terminals. The interface to the target display is with 3.3V LVCMOS levels, thus the VDDIO Terminal is connected to the 3.3 V rail. The optional Serial Bus control is used in this example, thus SCL and SDA are connected to the system and the ID[x] Terminal is connected to a resistor divider. LOCK is monitored by a system GPI (General Purpose Input).

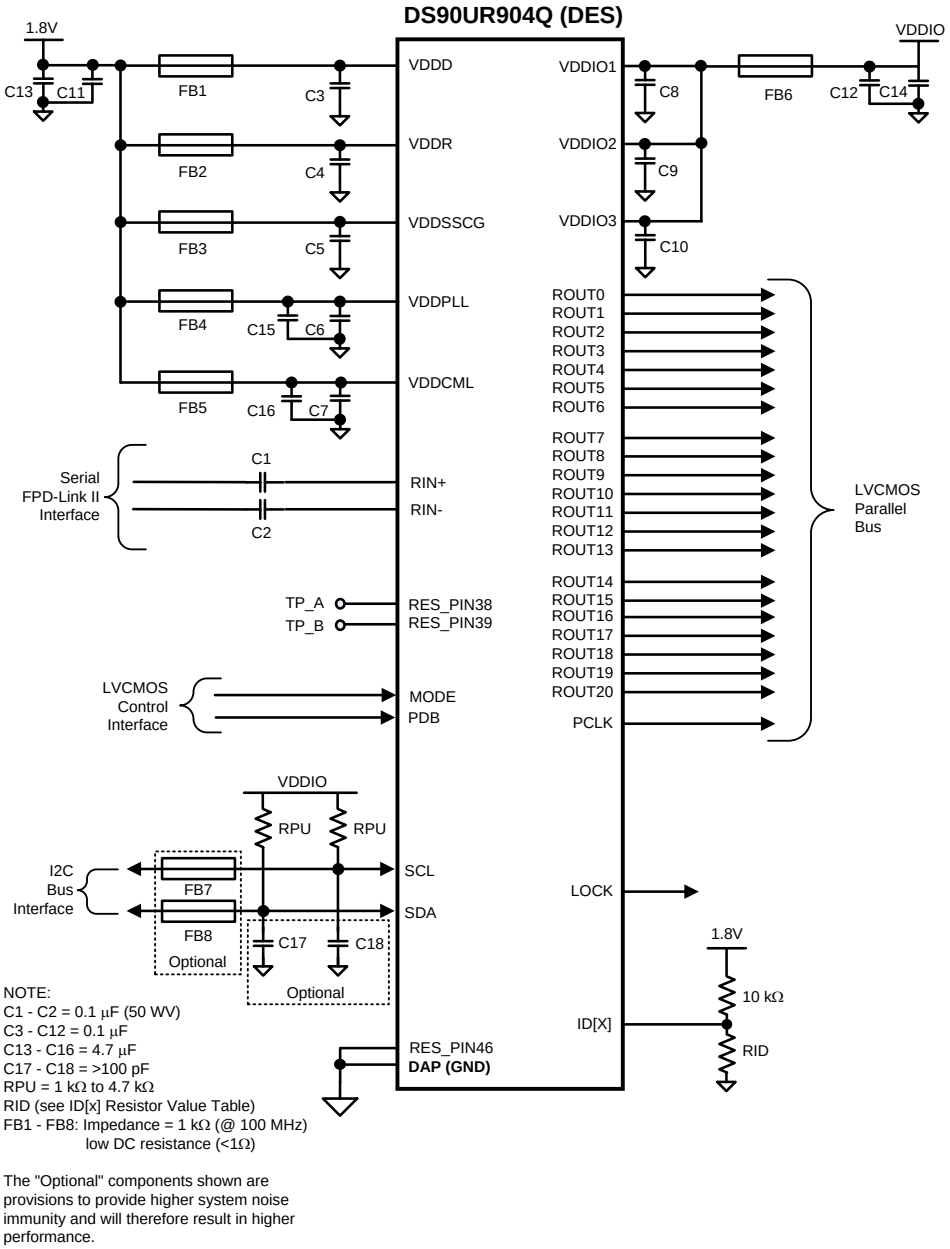


Figure 29. DS90UR904Q Typical Connection Diagram — Pin Control 48-Pin WQFN (RHS Package)

8.2.2.2 AC Coupling

The SER/DES supports only AC-coupled interconnects through an integrated DC balanced decoding scheme. External AC coupling capacitors must be placed in series in the FPD-Link II signal path as illustrated in Figure 30.

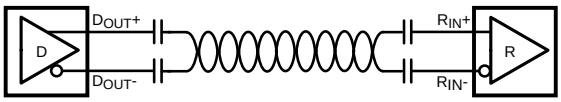


Figure 30. AC-Coupled Connection

For high-speed FPD-Link II transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The I/O's require a 100 nF AC coupling capacitors to the line.

8.2.2.3 Power Up Requirements and PDB PIN

When power is applied, the VDDIO supply needs to reach the expected operating voltage (1.8V or 3.3V) before the other supplies (VDDn) begin to ramp. It is also required to delay and release the PDB input signal after VDD (VDDn and VDDIO) power supplies have settled to the recommended operating voltages. A external RC network can be connected to the PDB pin to ensure PDB arrives after all the VDD have stabilized.

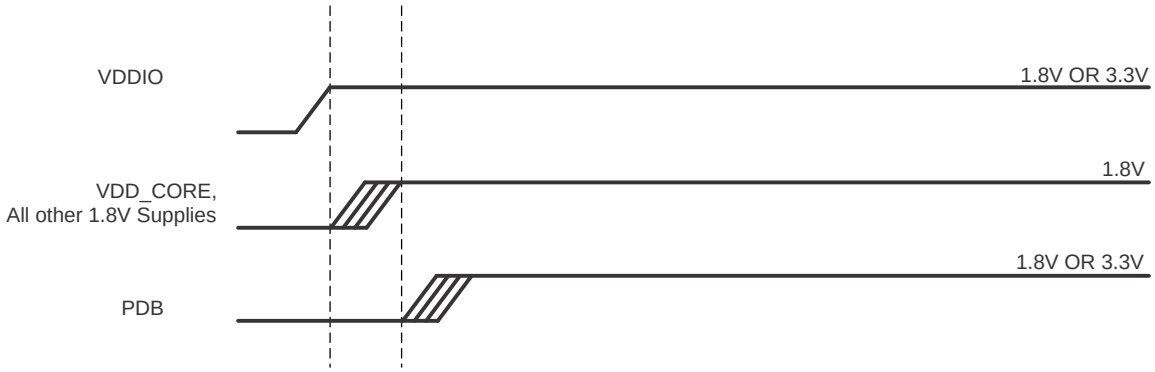


Figure 31. Power Up Sequence

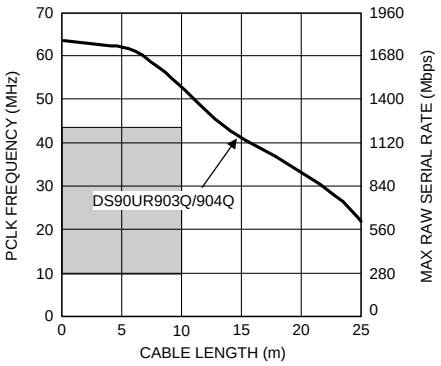
8.2.2.4 Transmission Media

The Ser/Des chipset is intended to be used over a wide variety of balanced cables depending on distance and signal quality requirements. The Ser/Des employ internal termination providing a clean signaling environment. The interconnect for FPD-Link II interface should present a differential impedance of 100 Ohms. Use of cables and connectors that have matched differential impedance will minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements. The chipset's optimum cable drive performance is achieved at 43 MHz at 10 meters length. The maximum signaling rate increases as the cable length decreases. Therefore, the chipset supports 50 MHz at shorter distances. Other cable parameters that may limit the cable's performance boundaries are: cable attenuation, near-end crosstalk and pair-to-pair skew.

For obtaining optimal performance, we recommend:

- Use Shielded Twisted Pair (STP) cable
- 100Ω differential impedance and 24 AWG (or lower AWG) cable
- Low skew, impedance matched
- Ground and/or terminate unused conductors

Figure 32 shows the Typical Performance Characteristics demonstrating various lengths and data rates using Rosenberger HSD and Leoni DACAR 538 Cable.



*Note: Equalization is enabled for cable lengths greater than 7 meters

Figure 32. Rosenberger HSD & Leoni DACAR 538 Cable Performance

8.2.2.5 Serial Interconnect Guidelines

For full details, see the *Channel-Link PCB and Interconnect Design-In Guidelines* (literature number SNLA008) and the *Transmission Line RAPIDESIGNER Operation and Applications Guide* (literature number SNLA035).

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the *LVDS Owner's Manual* (literature number SNLA187), which is available in PDF format from the TI LVDS & CML Solutions web site.

8.2.2.6 Application Curves

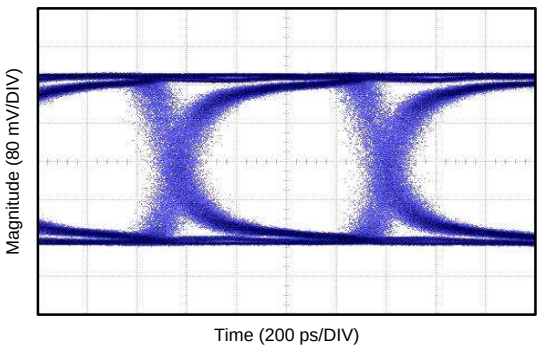


Figure 33. Serializer Eye Diagram at 1.2 Gbps Line Rate (43MHz Pixel Clock)

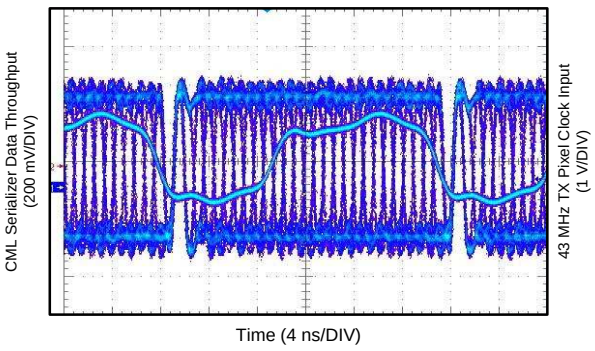


Figure 34. Serializer CML Output with 43MHz TX Pixel Clock

9 Power Supply Recommendations

These devices are designed to operate from an input core voltage supply of 1.8V. Some devices provide separate power and ground Terminals for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Terminal Description tables typically provide guidance on which circuit blocks are connected to which power Terminal pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100 Ohms are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in the *AN-1187 Leadless Leadframe Package (LLP) Application Report* (literature number SNOA401).

10.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the LLP package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown below:

Layout Example (continued)

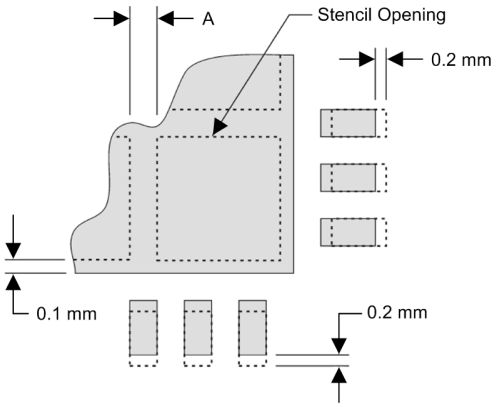


Figure 35. No Pullback LLP, Single Row Reference Diagram

Table 6. No Pullback LLP Stencil Aperture Summary for DS90UR903Q-Q1 and DS90UR904Q-Q1

Device	Pin Count	MKT Dwg	PCB I/O Pad Size (mm)	PCB Pitch (mm)	PCB DAP size(mm)	Stencil I/O Aperture (mm)	Stencil DAP Aperture (mm)	Number of DAP Aperture Openings	Gap Between DAP Aperture (Dim A mm)
DS90UR903Q-Q1	40	SNA40A	0.25 x 0.6	0.5	4.6 x 4.6	0.25 x 0.7	1.0 x 1.0	16	0.2
DS90UR904Q-Q1	48	SNA48A	0.25 x 0.6	0.5	5.1 x 5.1	0.25 x 0.7	1.1 x 1.1	16	0.2

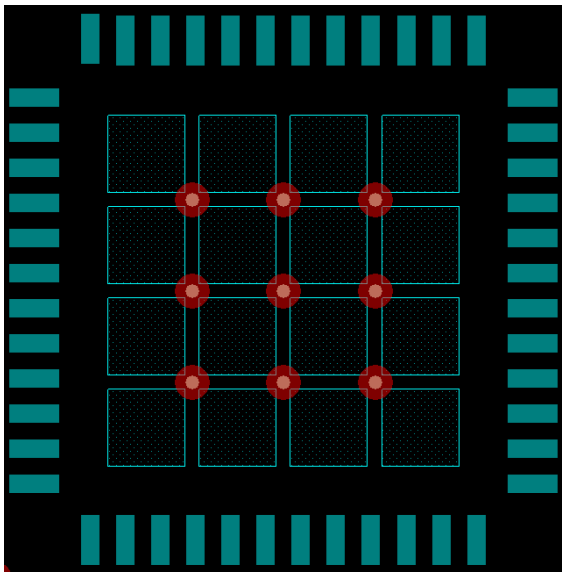


Figure 36. 48-Pin WQFN Stencil Example of Via and Opening Placement

The following PCB layout examples are derived from the layout design of the DS90UB903Q-Q1 and DS90UB904Q-Q1 in the SERDESUB-21USB Evaluation Module User's Guide (SNLU101). These graphics and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in the Ser/Des pair.

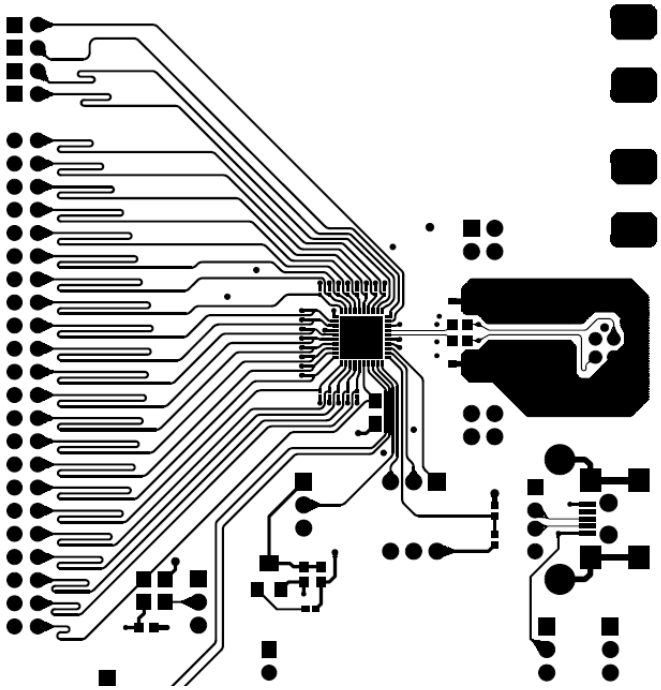


Figure 37. DS90UR903Q-Q1 Serializer Example Layout

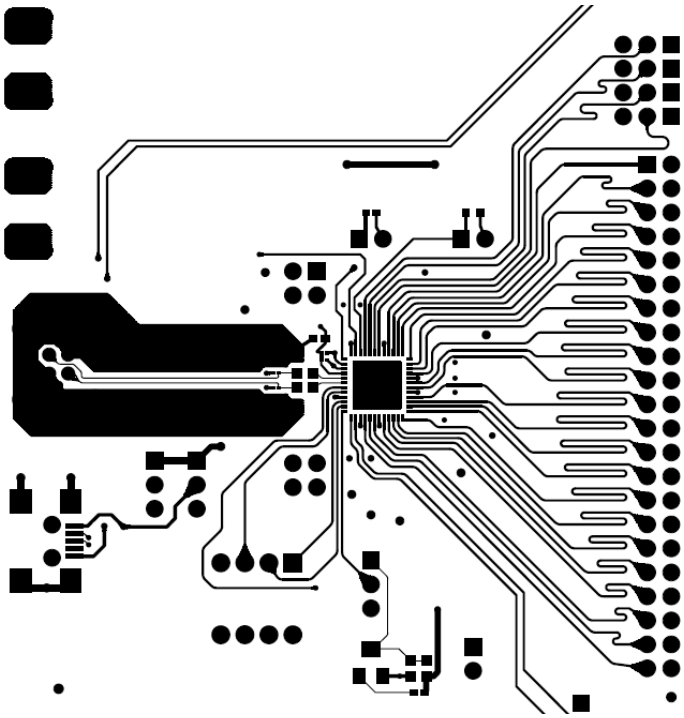


Figure 38. DS90UR904Q-Q1 Deserializer Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Soldering Specifications Application Report, SNOA549
- IC Package Thermal Metrics Application Report, SPRA953
- Channel-Link PCB and Interconnect Design-In Guidelines, SNLA008
- Transmission Line RAPIDESIGNER Operation and Application Guide, SNLA035
- Leadless Leadframe Package (LLP) Application Report, SNOA401
- LVDS Owner's Manual, SNLA187

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DS90UR903Q-Q1	Click here	Click here	Click here	Click here	Click here
DS90UR904Q-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UR903QSQ/NOPB	ACTIVE	WQFN	RTA	40	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UR903QSQ	Samples
DS90UR903QSQE/NOPB	ACTIVE	WQFN	RTA	40	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UR903QSQ	Samples
DS90UR903QSQX/NOPB	ACTIVE	WQFN	RTA	40	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UR903QSQ	Samples
DS90UR904QSQ/NOPB	ACTIVE	WQFN	RHS	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UR904QSQ	Samples
DS90UR904QSQE/NOPB	ACTIVE	WQFN	RHS	48	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UR904QSQ	Samples
DS90UR904QSQX/NOPB	ACTIVE	WQFN	RHS	48	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	UR904QSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

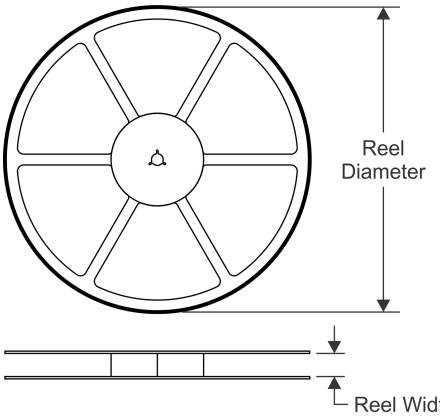
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

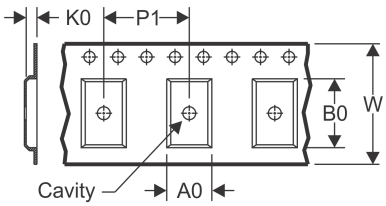
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

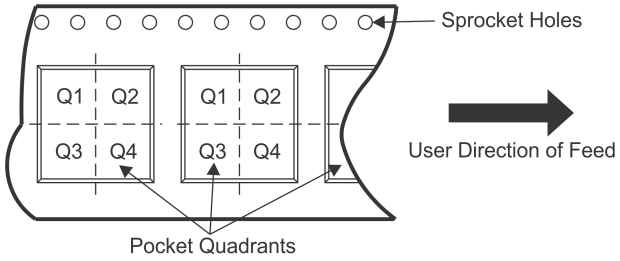


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

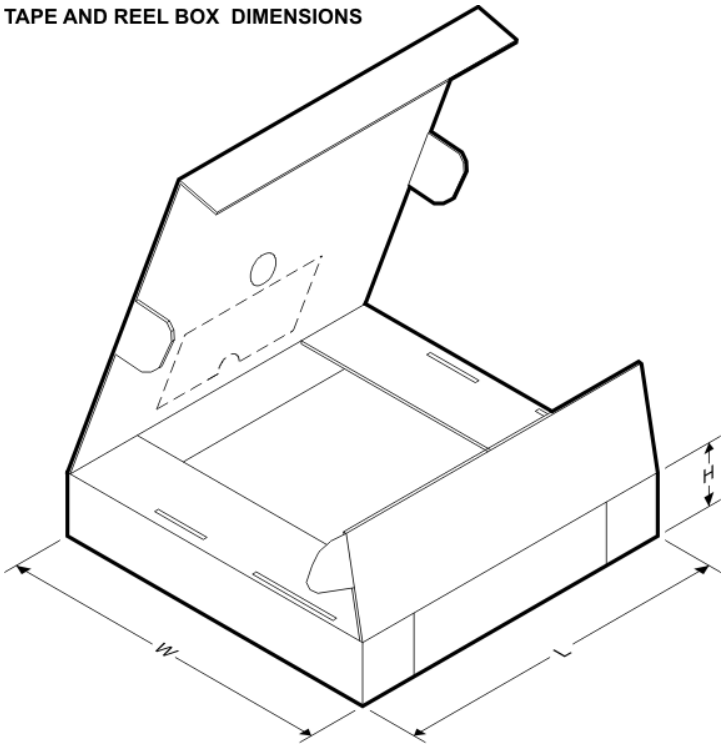


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UR903QSQ/NOPB	WQFN	RTA	40	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90UR903QSQE/NOPB	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90UR903QSQX/NOPB	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90UR904QSQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UR904QSQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UR904QSQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

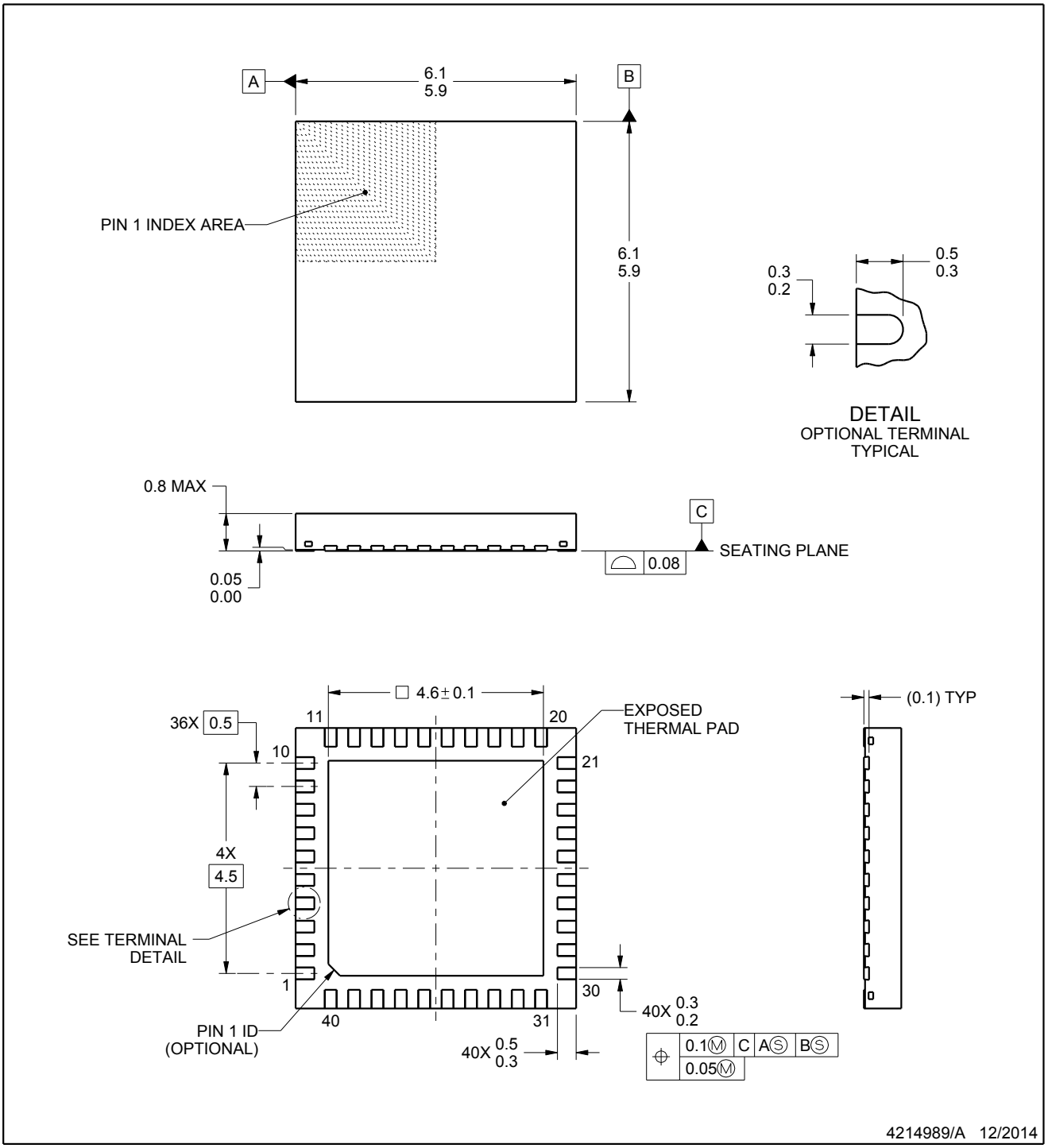
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UR903QSQ/NOPB	WQFN	RTA	40	1000	367.0	367.0	38.0
DS90UR903QSQE/NOPB	WQFN	RTA	40	250	213.0	191.0	55.0
DS90UR903QSQX/NOPB	WQFN	RTA	40	2500	367.0	367.0	38.0
DS90UR904QSQ/NOPB	WQFN	RHS	48	1000	367.0	367.0	38.0
DS90UR904QSQE/NOPB	WQFN	RHS	48	250	213.0	191.0	55.0
DS90UR904QSQX/NOPB	WQFN	RHS	48	2500	367.0	367.0	38.0

RTA0040A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

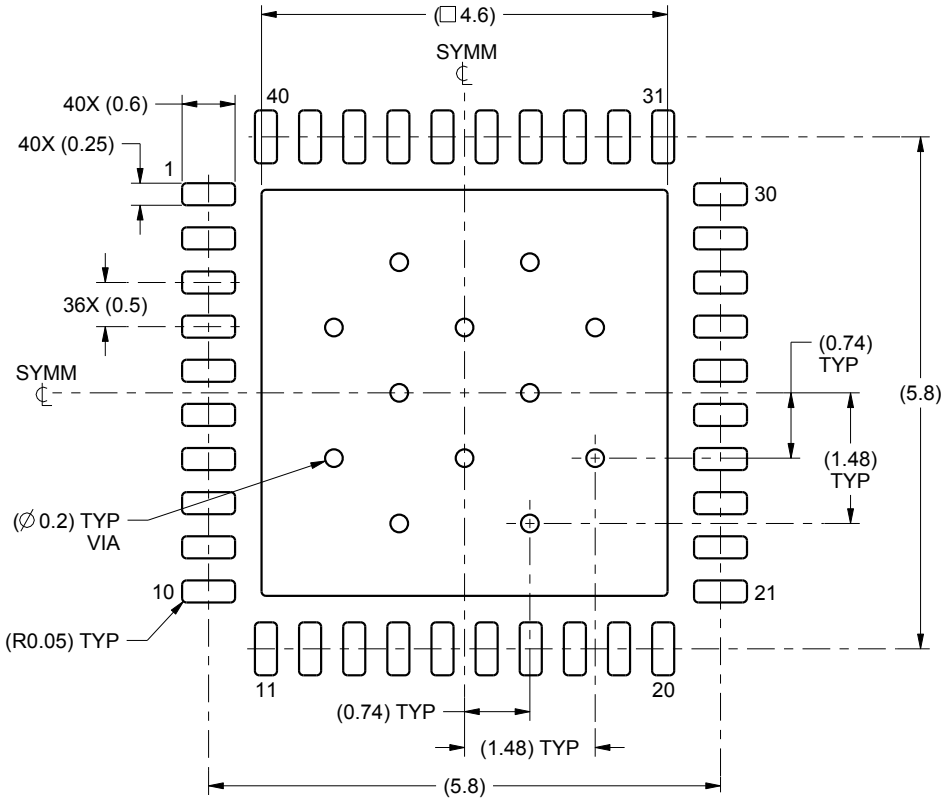
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

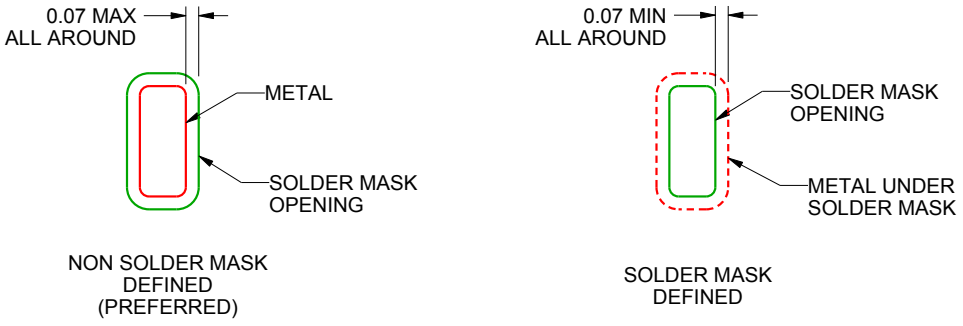
RTA0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

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NOTES: (continued)

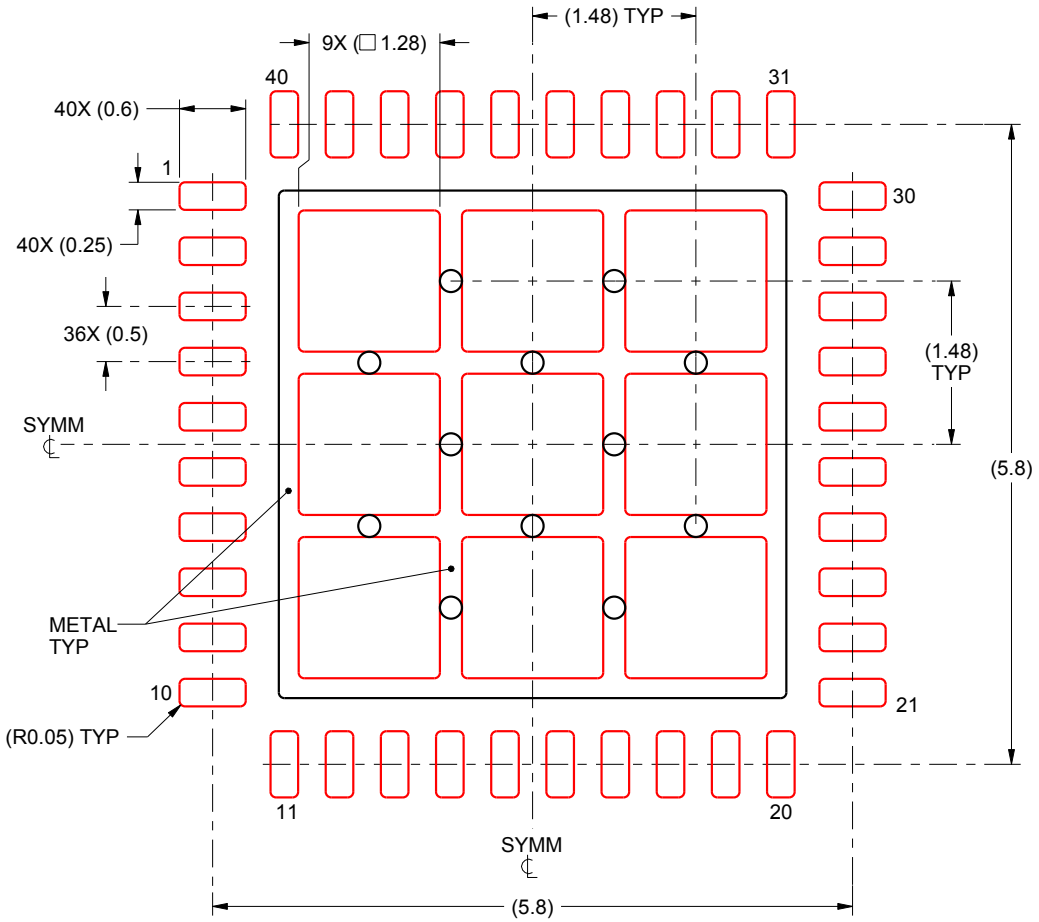
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RTA0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4214989/A 12/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

THERMAL PAD MECHANICAL DATA

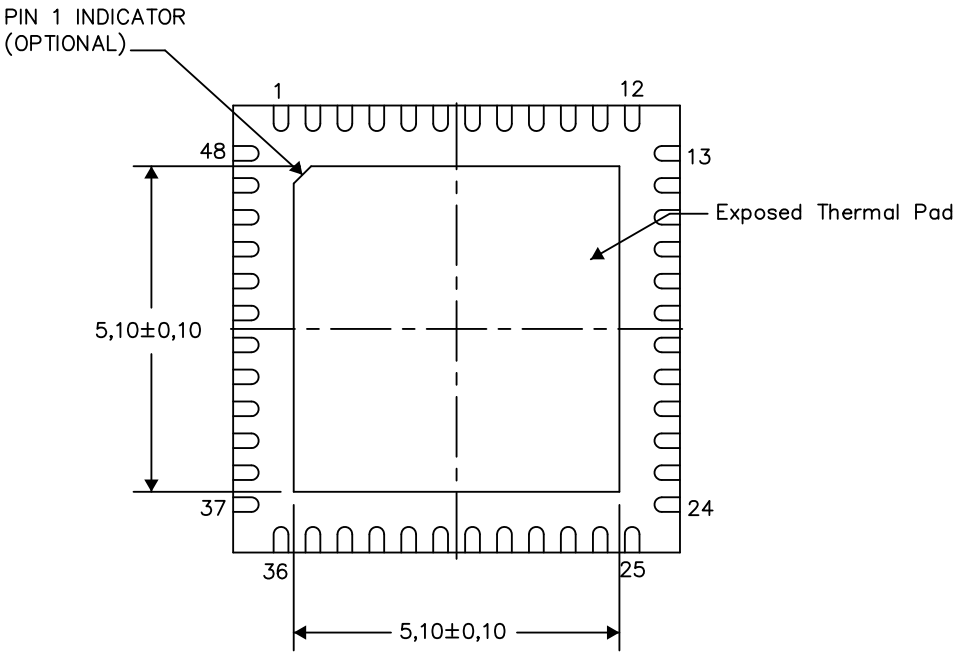
RHS (S–PWQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4221096–2/B 03/14

NOTE: All linear dimensions are in millimeters

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