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TPS65471RHAR

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# TPS65471 Single-Chip Power and Battery Management IC for Li-Ion Powered Systems

## 1 Features

- 40-Pin QFN package (6 mm x 6 mm) with PowerPAD™
- Integrated Dynamic Power Path Circuitry (VBUS, VAC, VBAT) With Power Good Signal Outputs and Reverse Current Protection
- 550-mA Li-Ion Battery Charger With 2 State Pins and Safety Timers
- Integrated 4.25-V Synchronous Boost Converter (PWM) and LDO to Provide Voltage Source for LEDs
- 4 LDOs for Each Function in the System
- USB Suspend Mode
- Reset Output
- 3 LED Drivers With PWM Control
- Integrated 3.0-V LDO Regulators
- Integrated 3.2-V LDO Regulators
- A Motor Driver Control
- LDO Regulators and Boost Converter On/Off Control
- Status Outputs to Indicate the Status of the Linear Charger
- Reverse Current Prevention and Thermal Shut Down Circuitry

## 2 Applications

Handheld Devices

## 3 Description

TPS65471 integrates a Li-ion linear charger, power path management, four LDO regulators, 4.25-V synchronous boost converter and 4.25-V LDO regulator, three LED drivers and one motor driver.

With the power path circuitry, USB-port, AC-DC adapter and Li-ion battery power can be switched seamlessly as the power source of 3.2-V LDO output regulators. This prevents instability in the system.

The TPS65471 charger automatically selects the USB port or the AC-DC adapter.

The EN_VLDO digital input is used to turn the output of VLED4P25, VLD02 and VLD04 on or off.

The EN_VLDO3 digital input is used to turn the output of VLDO3 on or off.

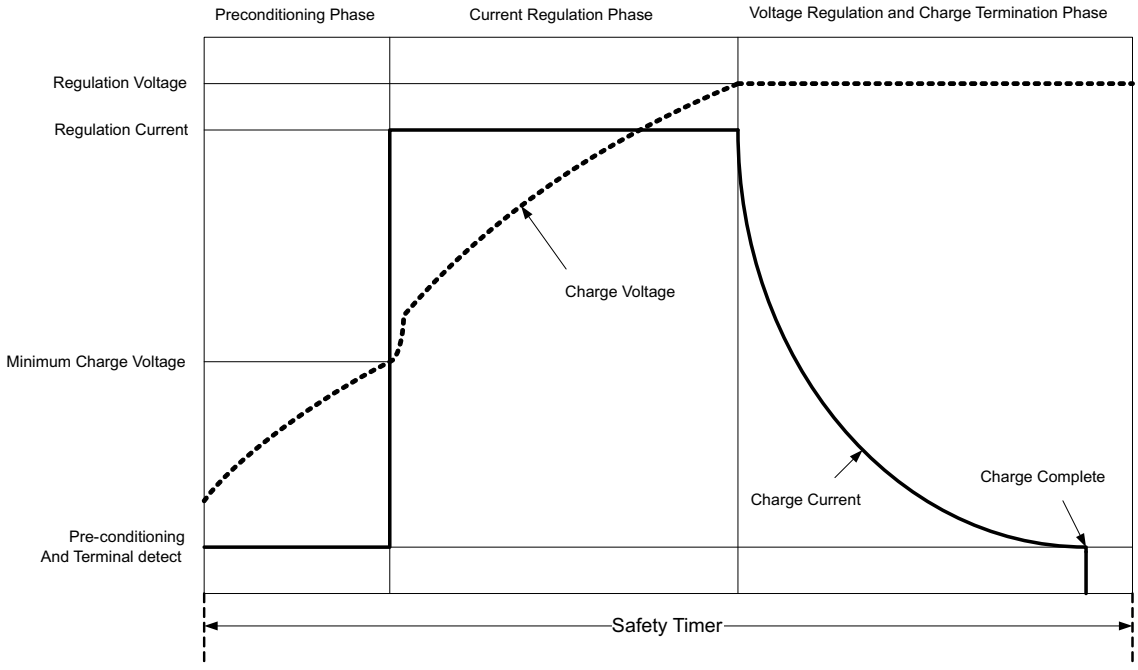
The TPS65471 is available in a 40-pin QFN package with PowerPAD™.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS65471 | VQFN (40) | 6.00 mm x 6.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Charging Profile**



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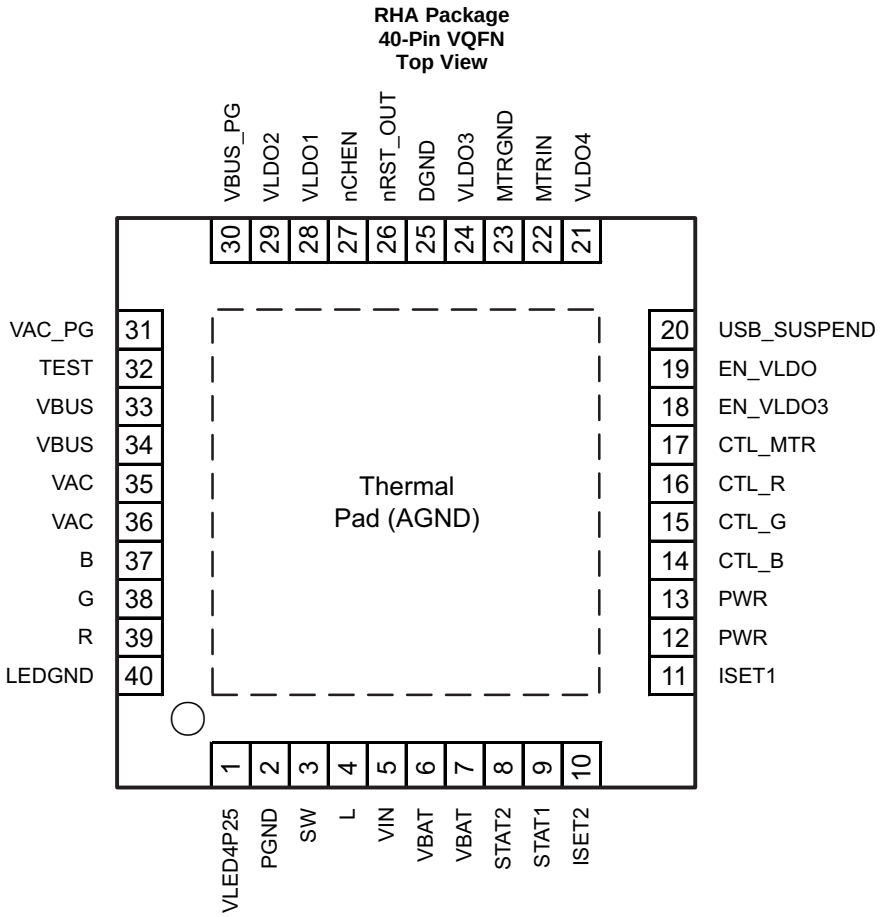
## 4 Revision History

| Changes from Original (June 2012) to Revision A | Page |
|---|---|
| • Added *Pin Configuration and Functions* section, *Feature Description* section, *Application and Implementation* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |

## 5 Pin Configuration and Functions




**Pin Functions**

| PIN | | DESCRIPTION | EXTERNAL REQUIRED COMPONENTS (SEE TYPICAL APPLICATION) |
|---|---|---|---|
| NAME | NO. | | |
| VAC | 35, 36 | Power input from AC-DC adapter | 1-µF capacitor to AGND to minimize overvoltage transients during AC power hot-plug events. Also Zener diode for surge protection is connected. |
| VBUS | 33, 34 | Power input from USB-port | 1-µF capacitor to AGND to minimize overvoltage transients during BUS power hot-plug events. Also Zener diode for surge protection is connected. |
| VBUS_PG | 30 | VBUS power-good status output. (CMOS output) | Can be used to indicate Power Good signal to system. |
| VAC_PG | 31 | VAC power-good status output (CMOS output) | Can be used to indicate Power Good signal to system. |
| STAT1 | 9 | Charge status output 1 (open-drain output) | Connect 100-kΩ external pullup resistor between STAT1 and VLDO1. |
| STAT2 | 8 | Charge status output 2 (open-drain output) | Connect 100-kΩ external pullup resistor between STAT2 and VLDO1. |
| ISET1 | 11 | Charge current set point for VBUS input | External resistor from ISET1 pin and AGND pin sets charge current value when the power input from USB-port. |
| ISET2 | 10 | Charge current set point for VAC input | External resistor from ISET1 pin and ISET2 pin sets charge current value when the power input from AC-DC adapter. |
| nCHEN | 27 | Charge enable input (active low) | Charge enable signal from system. |
| VIN | 5 | Power input for boost regulator. It is connected to the Li-ion battery. | Connect to Li-ion battery positive terminal. Connect 22-µF capacitor from VIN pin to PGND. |

## Pin Functions (continued)

| PIN | | DESCRIPTION | EXTERNAL REQUIRED COMPONENTS (SEE TYPICAL APPLICATION) |
|---|---|---|---|
| NAME | NO. | | |
| L | 4 | The inductor is connected between this pin and the SW pin | 6.8-µH inductor to SW pin. |
| SW | 3 | Switching node of the IC. Connect the inductor between this pin and the L pin. | 6.8-µH inductor to L pin. |
| VLED4P25 | 1 | LDO and synchronous boost converter output | 22-µF capacitor to PGND. Connect series resistor for current limitation to each LED (R,G,B). |
| PGND | 2 | Synchronous boost converter power ground | Connect to ground plane. |
| VBAT | 6, 7 | Power input and output for Li-ion battery | Connect to Li-ion battery positive terminal. Connect 1-µF capacitor from VBAT pin to AGND. |
| R | 39 | Output for Red LED driver. The open-drain output pulls low when the CTL_R pin goes to H level. $R_{ON}$ = 1 Ω (typical) | Connect to RED input of Red LED. |
| G | 38 | Output for Green LED driver. The open-drain output pulls low when the CTL_G pin goes to H level. $R_{ON}$ = 1 Ω (typical) | Connect to GREEN input of Green LED. |
| B | 37 | Output for Blue LED driver. The open-drain output pulls low when the CTL_B pin goes to H level. $R_{ON}$ = 1 Ω (typical) | Connect to BLUE input of Blue LED. |
| LEDGND | 40 | LED drivers power ground | Connect to ground plane. |
| VLDO1 | 28 | LDO output, fixed 3.2 V. The output current of VLOD1 is limited to 20 mA (maximum), when both EN_VLDO and EN_VLDO3 input pins are low level. | 1-µF capacitor to AGND |
| VLDO2 | 29 | LDO output, fixed 3.2 V | 1-µF capacitor to AGND |
| VLOD3 | 24 | LDO output, fixed 3.2 V | 1-µF capacitor to AGND |
| VLDO4 | 21 | LDO output, fixed 3.0 V | 1-µF capacitor to AGND |
| nRST_OUT | 26 | System reset output, generated according to the VLDO1 output voltage (open-drain output). Connect 100-kΩ internal pullup resistor between nRST_OUT and VLDO1. | Can be used to indicate the reset output signal to system. |
| MTRIN | 22 | Motor driver output. The open-drain output pulls low when the CTL_MTR pin goes to H level. $R_{ON}$ = 1 Ω (typical) | Can be used to drive motor. |
| CTL_MTR | 17 | Control input for motor driver (active H) | Motor driver control input signal from system |
| MTRGND | 23 | Motor driver power ground | Connect ground plane |
| CTL_B | 14 | Control input for (B pin) Blue LED driver (active H) | Blue LED driver control input signal from system |
| CTL_G | 15 | Control input for (G pin) Green LED driver (active H) | Green LED driver control input signal from system |
| CTL_R | 16 | Control input for (R pin) Red LED driver (active H) | Red LED driver control input signal from system |
| DGND | 25 | Digital ground | Connect to ground plane. |
| PWR | 12,13 | Power path output. The power supply for each LDO. | 10-µF capacitor to AGND. Regarding an effect of DC bias on capacitor, select a capacitor that can secure at least 4.7-µF in worse case. |
| EN_VLDO | 19 | Enable input for VLDO2, VLDO4 and VLED4P25 (active H) | LDO2, LDO4 and 4.25 VLDO control input signal from system |
| EN_VLDO3 | 18 | Enable input for VLDO3 | LDO3 control input signal from system |
| TEST | 32 | Test pin. Normally open. | |
| USB_SUSPEND | 20 | Control input for USB suspended mode. To reduce supply current from VBUS (active H). | USB suspended input signal from system |
| Thermal Pad (AGND) | | Analog ground (AGND) input. Thermal ground should be soldered to the analog ground, use thermal via to connect to ground plane for ideal power dissipation. | Connect the PowerPAD to ground plane. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VBUS, VAC, PWR, SW, ISET1, ISET2 | –0.3 | 7 | V |
| | VBAT, VLDO1, VLDO2, VDLO3, VDLO4, VLED4P25, VIN, L, R, G, B, MTRIN | –0.3 | 5.5 | |
| | nCHEN, USB_SUSPEND, CTL_R, CTL_G, CTL_B, CTL_MTR, EN_VLDO, EN_VLDO3, nRST_OUT, VBUS_PG, VAC_PG, STAT1, STAT2 | –0.3 | 3.6 | |
| Output sink/source current | VBUS_PG, VAC_PG, nRST_OUT, STAT1, STAT2 | | 15 | mA |
| Operating junction temperature | | –40 | 150 | °C |
| Storage temperature range, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

## 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{VBUS}$ | Supply voltage (VBUS) | 4.75 | 5.25 | V |
| $V_{VAC}$ | Supply voltage (VAC) | 4.75 | 5.75 | V |
| $V_{VBAT1}$ | Supply voltage (VBAT) for linear charger | 2.7 | 4.3 | V |
| $V_{VBAT2}$ | Supply voltage (VBAT) for 4.25-V boost output | 3.2 | 4.3 | V |
| $T_A$ | Operating ambient temperature | –10 | 85 | °C |
| $T_J$ | Operating junction temperature | –10 | 125 | °C |

(1) Current dissipation and junction temperature must be confirmed on maximum $V_{VBUS}$, $V_{VAC}$ and $V_{VBAT}$.
(2) If any $V_{VBUS}$ or $V_{VAC}$ or $V_{VBAT}$ is a recommended operating condition, this device can operate. Refer to Table 1.
(3) LDO1 operates when the output voltage of LDO1 is less than $V_{RST}$.

## 6.3 Thermal Information

| THERMAL METRIC(1) | | TPS65471 RHA (VQFN) 40 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 30.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.4 Electrical Characteristics

over –10°C < $T_J$ < 125°C and recommended supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CURRENT** | | | | | | |
| $I_{VAC}$ | Active supply current from VAC | No load, EN_VLDO = H, EN_VLDO3 = H, nCHEN = H, USB_SUSPEND = L, VBAT = 3.8 V, VAC = 5.25 V | | 237 | | µA |
| $I_{VBUS}$ | Active supply current from VBUS | No load, EN_VLDO = H, EN_VLDO3 = H, nCHEN = H, USB_SUSPEND = L, VBAT = 3.8 V, VAC = 5 V | | 237 | | µA |
| $I_{VBUS(USPND)}$ | VBUS current at USB suspend mode | No load, EN_VLDO = H, EN_VLDO3 = H, nCHEN = H, USB_SUSPEND = H, VBAT = 2.8 V, VAC = 5.25 V | | 207 | 290 | µA |
| $I_{VBAT}$ | Active supply current from VBAT | No load, EN_VLDO = H, EN_VLDO3 = H, nCHEN = H, USB_SUSPEND = L, VBAT = 4.2 V | | 1.4 | | mA |

## Electrical Characteristics (continued)

over –10°C < $T_J$ < 125°C and recommended supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{VBAT(STBY)}$ | VBAT standby current | No load, EN_VLDO = L, EN_VLDO3 = L, nCHEN = H, USB_SUSPEND = L, VBAT = 4.2 V, $T_J$ = 60°C | | 56 | 88 | µA |
| $I_{VBAT(SUP)}$ | Sleep current at VBAT | Sum of current into VBAT pin. VBAT = 2.5 V < $V_{(BATUVLO)}$ At nCHEN=H and state #01, 02, 03, 04, 09, 10, $T_J$ = 60°C | | 3 | | µA |
| **UVLO/PG COMPARATOR/OVER DISCHARGE PROTECTION FOR LI-ION** | | | | | | |
| $V_{(VBUSPG)}$ | Power good threshold voltage for VBUS | At VBUS pin, L to H | 4.08 | 4.25 | 4.42 | V |
| $V_{(VBUSPGHYS)}$ | Hysteresis voltage on $V_{(VBUSPG)}$ | At VBUS pin, $V_{(VBUSPG)}$ - $V_{(VBUSPGHYS)}$ is threshold voltage for H to L | | 100 | | mV |
| $V_{(VACPG)}$ | Power good threshold voltage for VAC | At VAC pin, L to H | 4.08 | 4.25 | 4.42 | V |
| $V_{(VACPGHYS)}$ | Hysteresis voltage on $V_{(VACPG)}$ | At VAC pin, $V_{(VAC)}$ - $V_{(VACHYS)}$ is threshold voltage for H to L | | 100 | | mV |
| $V_{(BATUVLO)}$ | Under voltage lock out voltage for Li-ion | At VBAT pin | 2.6 | 2.7 | 2.8 | V |
| $V_{BATmin(BATUVLO)}$ | Minimum $V_{BAT}$ for over discharge protection | At VBAT pin(1) | | 1.5 | | V |
| $t_{dly(BATUVLO)}$ | Li-ion UVLO deglitch time | Only for falling edge (H to L) | | 420 | | µs |
| **POWER PATH** | | | | | | |
| $R_{ON(BUS)}$ | Resistance of a FET between VBUS and PWR | VBUS = 4.75 V | | 130 | | mΩ |
| $R_{ON(AC)}$ | Resistance of a FET between VAC and PWR | VAC = 4.75 V | | 130 | | mΩ |
| $R_{ON(BAT)}$ | Resistance of a FET between VBAT and PWR | VABT = 3.3 V | | 50 | | mΩ |
| | | VBAT = 3.3 V, EN_VLDO = L, EN_VLDO3 = L | | 5 | | Ω |
| **LDO REGULATORS** | | | | | | |
| **LDO4 ($C_{OUT}$ = 1 µF, 3.4 V < PWR < 5.75 V)** | | | | | | |
| $V_{(VLDO4)}$ | VLDO4 output voltage | 3.4 V < PWR < 5.75 V | 2.9 | 3 | 3.1 | V |
| $I_{(VLDO4)}$ | VLDO4 output current | | 1 | | 150 | mA |
| $V_{DO(VLDO4)}$ | VLDO4 dropout voltage | $I_O$ = 150 mA | | 0.14 | | V |
| $I_{(VLDO4\_ILMT)}$ | VLDO4 output current limit | | 350 | | | mA |
| $PSRR_{(VLDO4)}$ | Power supply rejection ratio | | | -60 | | dB |
| **LDO1 ($C_{OUT}$ = 1 µF, 3.4 V < PWR < 5.75 V)** | | | | | | |
| $V_{(VLDO1)}$ | VLDO1 output voltage | 3.4 V < PWR < 5.75 V | 3.136 | 3.2 | 3.264 | V |
| $I_{(VLDO1)}$ | VLDO1 output current | | 1 | | 100 | mA |
| $V_{DO(VLDO1)}$ | VLDO1 dropout voltage | $I_O$ = 100 mA | | 0.12 | | V |
| $I_{(VLDO1\_ILMT)}$ | VLDO1 output current limit | | | 250 | | mA |
| $PSRR_{(VLDO1)}$ | Power supply rejection ratio | | | -60 | | dB |
| $R_{ON(VLDO1\_dichg)}$ | Discharge resistance on VLDO1 | | | 630 | | Ω |
| **RESET CIRCUIT** | | | | | | |
| $V_{(RST)}$ | Reset threshold voltage | At VLDO1, H to L | 2.7 | 2.8 | 2.9 | V |
| $V_{(RSTHYS)}$ | Hysteresis voltage for reset | At VLDO1, $V_{(RST)}$ + $V_{(RSTHYS)}$ is threshold voltage for L to H | | 140 | | mV |
| **LDO2 ($C_{OUT}$ = 1 µF, 3.4 V < PWR < 5.75 V)** | | | | | | |
| $V_{(VLDO2)}$ | VLDO2 output voltage | 3.4 V < PWR < 5.75 V | 3.136 | 3.2 | 3.232 | V |
| $I_{(VLDO2)}$ | VLDO2 output current | | 1 | | 30 | mA |
| $V_{DO(VLDO2)}$ | VLDO2 dropout voltage | $I_O$ = 30 mA | | 0.03 | | V |
| $I_{(VLDO2\_ILMT)}$ | VLDO2 output current limit | | | 250 | | mA |
| $PSRR_{(VLDO2)}$ | Power supply rejection ratio | | | -60 | | dB |

(1) Not tested in production.

## Electrical Characteristics (continued)

over –10°C < $T_J$ < 125°C and recommended supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LDO3 ($C_{OUT}$ = 1 µF, 3.4 V < PWR < 5.75 V)** | | | | | | |
| $V_{(VLDO3)}$ | VLDO3 output voltage | 3.4 V < PWR < 5.75 V | 3.136 | 3.2 | 3.264 | V |
| $I_{(VLDO3)}$ | VLDO3 output current | | 1 | | 150 | mA |
| $V_{DO(VLDO3)}$ | VLDO3 dropout voltage | $I_O$ = 150 mA | | 0.13 | | V |
| $I_{(VLDO3\_ILMT)}$ | VLDO3 output current limit | | | 250 | | mA |
| $PSRR_{(VLDO3)}$ | Power supply rejection ratio | | | –60 | | dB |
| **LINEAR CHARGER** | | | | | | |
| **VOLTAGE REGULATION ($V_{O(REG)}$ + $V_{(DO\_MAX)}$ < $V_{PWR}$, $I_{(TERM)}$ < $I_{O(OUT)}$ < 550 mA)** | | | | | | |
| $V_{O(REG)}$ | Output voltage | | | 4.2 | | V |
| $A_{CC(REG)}$ | Voltage regulation accuracy | $T_A$ = 25°C, $I_{O(OUT)}$ = 50 mA | –0.35 | | 0.35 | % |
| | | See (2) | –1 | | 1 | |
| $V_{(DO)}$ | Dropout voltage ($V_{(PWR)}$ - $V_{(OUT)}$) | | | 350 | 500 | mV |
| **CURRENT REGULATION** | | | | | | |
| $I_{O(OUT)}$ | Output current range | $V_{PWR}$ > $V_{(LOWV)}$<br>$V_{PWR}$ - $V_{VBAT}$ > $V_{(DO)}$<br>$V_{PWR}$ > 4.6 V | 50 | | 550 | mA |
| $V_{(SET)}$ | Output current set voltage | Voltage on ISET1 pin,<br>$V_{PWR}$ = 4.85 V, $I_{O(OUT)}$ = 550 mA<br>$V_{BAT}$ = 4 V | 2.463 | 2.5 | 2.538 | V |
| $K_{(SET)}$ | Output current set factor | $V_{PWR}$ = 4.85 V, $I_{O(OUT)}$ = 60 mA<br>$V_{BAT}$ = 2.8 V, Pre-charge mode | 299 | 319 | 339 | |
| | | $V_{PWR}$ = 4.85 V, $I_{O(OUT)}$ = 60 mA<br>$V_{BAT}$ = 4 V, CC mode | 285 | 321 | 357 | |
| | | $V_{PWR}$ = 4.85 V, $I_{O(OUT)}$ = 550 mA<br>$V_{BAT}$ = 4 V, CC mode | 307 | 322 | 337 | |
| **PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION** | | | | | | |
| $V_{(LOWV)}$ | Precharge to fast-charge transition threshold | Voltage on VBAT pin | 2.8 | 3 | 3.2 | V |
| $t_{(DEG\text{-}FtoP)}$ | Deglitch time for fast-charge to precharge transition | $V_{PWR(min)}$ > 4.6 V, $t_{FALL}$ = 100 ns,<br>10-mV overdrive,<br>VBAT decreasing below threshold. | 250 | 375 | 500 | ms |
| $I_{O(PRECHARGE)}$ | Precharge range | 0 V < $V_{PWR}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$ | 5 | | 55 | mA |
| $V_{(PRECHG)}$ | Precharge set voltage | Voltage on ISET1 pin,<br>$V_{O(REG)}$ = 4.2 V,<br>0 V < $V_{PWR}$ > $V_{(LOWV)}$, t < $t_{(PRECHG)}$ | 235 | 250 | 265 | mV |
| **TERMINATION DETECTION** | | | | | | |
| $I_{(TERM)}$ | Charge termination detection range | $V_{BAT}$ > $V_{(RCH)}$, t < $t_{(TRMDET)}$ | 5 | | 55 | mA |
| $V_{(TERM)}$ | Charge termination detection set voltage | Voltage on ISET1 pin,<br>$V_{O(REG)}$ = 4.2 V<br>$V_{BAT}$ > $V_{(RCH)}$, t < $t_{(TRMDET)}$ | 235 | 250 | 265 | mV |
| $t_{(TRMDET)}$ | Deglitch time for termination detection | $V_{PWR(min)}$ > 4.6 V, $t_{FALL}$ = 100 ns,<br>Charging current decreasing below<br>10-mV overdrive | 250 | 375 | 500 | ms |

(2) Specified by characterization. Not tested in production.

## Electrical Characteristics (continued)

over –10°C < $T_J$ < 125°C and recommended supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BATTERY RECHARGE THRESHOLD** | | | | | | |
| $V_{(RCH)}$ | Recharge threshold | $T_A$ = 25°C | $V_{O(REG)}$ - 0.115 | $V_{O(REG)}$ - 0.10 | $V_{O(REG)}$ - 0.085 | V |
| $t_{(DEGL)}$ | Deglitch time for recharge detect | $V_{PWR(min)}$ > 4.6 V, $t_{FALL}$ = 100 ns, Decreasing below or increasing above threshold, 10-mV overdrive | 250 | 375 | 500 | ms |
| **TIMERS** | | | | | | |
| $t_{(PRECHG)}$ | Precharge time | | 1620 | 1800 | 1989 | s |
| $t_{(CHG)}$ | Charge time | | 22680 | 25200 | 27720 | s |
| $I_{(FAULT)}$ | Timer fault recovery current | | | 200 | | µA |
| $t_{(TMRRST)}$ | Deglitch time to reset timers when disabling charger | | 250 | 375 | 500 | ms |
| **BATTERY CHARGER ON/OFF COMPARATOR** | | | | | | |
| $V_{(CHGOFF)}$ | Charger off threshold voltage | 2.7 V < $V_{BAT}$ < $V_{O(REG)}$ | $V_{PWR}$ < $V_{BAT}$ + 80 mV | | | V |
| $V_{(CHGON)}$ | Charger on threshold voltage | 2.7 V < $V_{BAT}$ < $V_{O(REG)}$ | $V_{PWR}$ > $V_{BAT}$ + 110 mV | | | V |
| **ISET2** | | | | | | |
| $R_{ON(ISET2)}$ | N-channel MOSFET on-resistance between ISET2 and GND | $V_{AC}$ = 4.75 V | | 4 | | Ω |
| **4.25-V BOOST AND LDO ($C_{OUT}$ = 22 µF, L = 6.8 µH, $C_{IN}$ = 22 µF)** | | | | | | |
| $V_{(VLED4P25)}$ | VLED4P25 output voltage | 3.2 V < $V_{BAT}$ < 4.3 V for boost or 4.6 V < PWR < 5.75 V for LDO | 4.165 | 4.25 | 4.335 | V |
| $I_{(VLED4P25)}$ | VLED4P25 output current | | 1 | | 140 | mA |
| **4.25-V LDO** | | | | | | |
| $I_{(VLED4P25\_ILMT)}$ | 4.25-V LDO output current limit | 4.6 V < PWR < 5.75 V | | 250 | | mA |
| $V_{DO(VLED4P25)}$ | 4.25-V LDO dropout voltage | $I_O$ = 140 mA | | | 0.35 | V |
| $PSRR_{(VLED4P25)}$ | Power supply rejection ratio | | | -60 | | dB |
| **4.25-V BOOST** | | | | | | |
| $f_{OSC\_VLED4P25}$ | 4.25-V boost switching frequency | | | 555 | | kHz |
| $I_{(VLED4P25\_Boost\_ILMT)}$ | 4.25-V boost output current limit | 3.2 V < $V_{BAT}$ < 4.3 V | | 800 | | mA |
| $R_{ON(ISO)}$ | Isolation MOSFET on-resistance between VIN and L | $V_{BAT}$ = 3.2 V | | 300 | | mΩ |
| **R, G, B OUTPUTS** | | | | | | |
| $R_{ON(R)}$ | N-channel MOSFET on-resistance between R and LEDGND | | | 1 | | Ω |
| $R_{ON(G)}$ | N-channel MOSFET on-resistance between G and LEDGND | | | 1 | | Ω |
| $R_{ON(B)}$ | N-channel MOSFET on-resistance between B and LEDGND | | | 1 | | Ω |
| **MTRIN OUTPUT** | | | | | | |
| $R_{ON(MTR)}$ | N-channel MOSFET on-resistance between MTRIN and MTRGND | | | 1 | | Ω |
| **CTR_R, CTL_G, CTL_B, CTL_MTR, EN_VLDO, EN_VLDO3, USB_SUSPEND AND nCHEN INPUTS** | | | | | | |
| $V_{IL}$ | Low level input voltage | VLDO1 = 3.2 V | 0.3 x VLDO1 | | | V |
| $V_{IH}$ | High level input voltage | VLDO1 = 3.2 V | | | 0.7 x VLDO1 | V |
| $R_{PD(CTL\_R)}$ | Pull-down resistor (CTL_R) | | | 1000 | | kΩ |
| $R_{PD(CTL\_G)}$ | Pull-down resistor (CTL_G) | | | 1000 | | kΩ |
| $R_{PD(CTL\_B)}$ | Pull-down resistor (CTL_B) | | | 1000 | | kΩ |
| $R_{PD(CTL\_MTR)}$ | Pull-down resistor (CTL_MTR) | | | 100 | | kΩ |
| $R_{PD(EN\_VLDO)}$ | Pull-down resistor (EN_VLDO) | | | 100 | | kΩ |
| $R_{PD(EN\_VLDO3)}$ | Pull-down resistor (EN_VLDO3) | | | 100 | | kΩ |
| $R_{PD(USB\_SUSPEND)}$ | Pull-down resistor (USB_SUSPEND) | | | 100 | | kΩ |
| $R_{PU(nCHEN)}$ | Pull-up resistor (nCHEN) to VLDO1 | | | 100 | | kΩ |

## Electrical Characteristics (continued)

over –10°C < $T_J$ < 125°C and recommended supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VBUS_PG, VAC_PG OUTPUTS** | | | | | | |
| $V_{OH(PG)}$ | High-level output saturation voltage | 3.4 V < PWR < 5.75 V, $I_O$ = -500 µA, VDD = VLDO1 | VDD - 0.25 | | | V |
| $V_{OL(PG)}$ | Low-level output saturation voltage | 3.4 V < PWR < 5.75 V, $I_O$ = 500 µA, VDD = VLDO1 | | | 0.25 | V |
| **STAT1, STAT2 OUTPUTS** | | | | | | |
| $V_{OL(STAT)}$ | Low-level output saturation voltage | $I_O$ = 2.5 mA | | | 0.25 | V |
| **nRST_OUT OUTPUT** | | | | | | |
| $V_{OL(nRST)}$ | Low-level output saturation voltage | $I_O$ = 2.5 mA | | | 0.25 | V |
| $R_{PU(nRST)}$ | Pull-up resistor (nRST_OUT) to VLDO1 | | | 100 | | kΩ |
| $t_{dly(nRST)}$ | Deglitch time on nRST_OUT | | 95 | 125 | 160 | ms |
| **THERMAL SHUTDOWN THRESHOLD** | | | | | | |
| $T_{(SHTDWN)}$ | Thermal trip threshold | $T_J$ increasing | | 150 | | °C |
| $hys_{(SHTDWN)}$ | Thermal hysteresis | $T_J$ increasing | | 15 | | °C |

## 6.5 Dissipation Ratings[1]

| PACKAGE | $T_A$ < 40°C POWER RATING (W) | DERATING FACTOR ABOVE $T_A$ = 40°C (mW/°C) |
|---|---|---|
| RHA | 2.82 | 33.2 |

(1) This data is based on using the JEDEC High-K board and exposed die pad is connected to a Cu pad on the board.

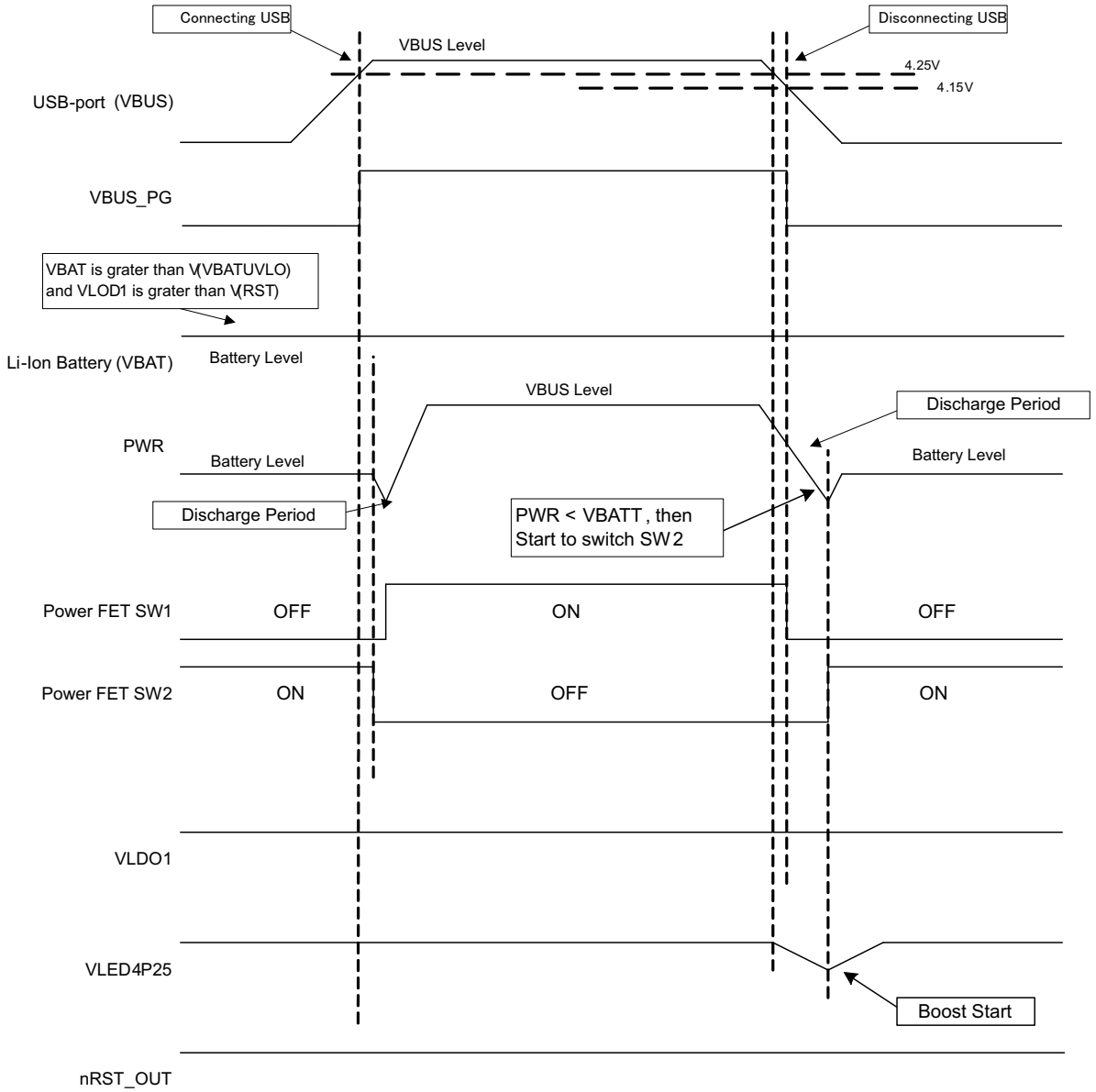



**Figure 1. USB-Port Hot-Plug During Battery Operation (#5# → #7# → #5#, Charge Off, EN_VLDO = H)**

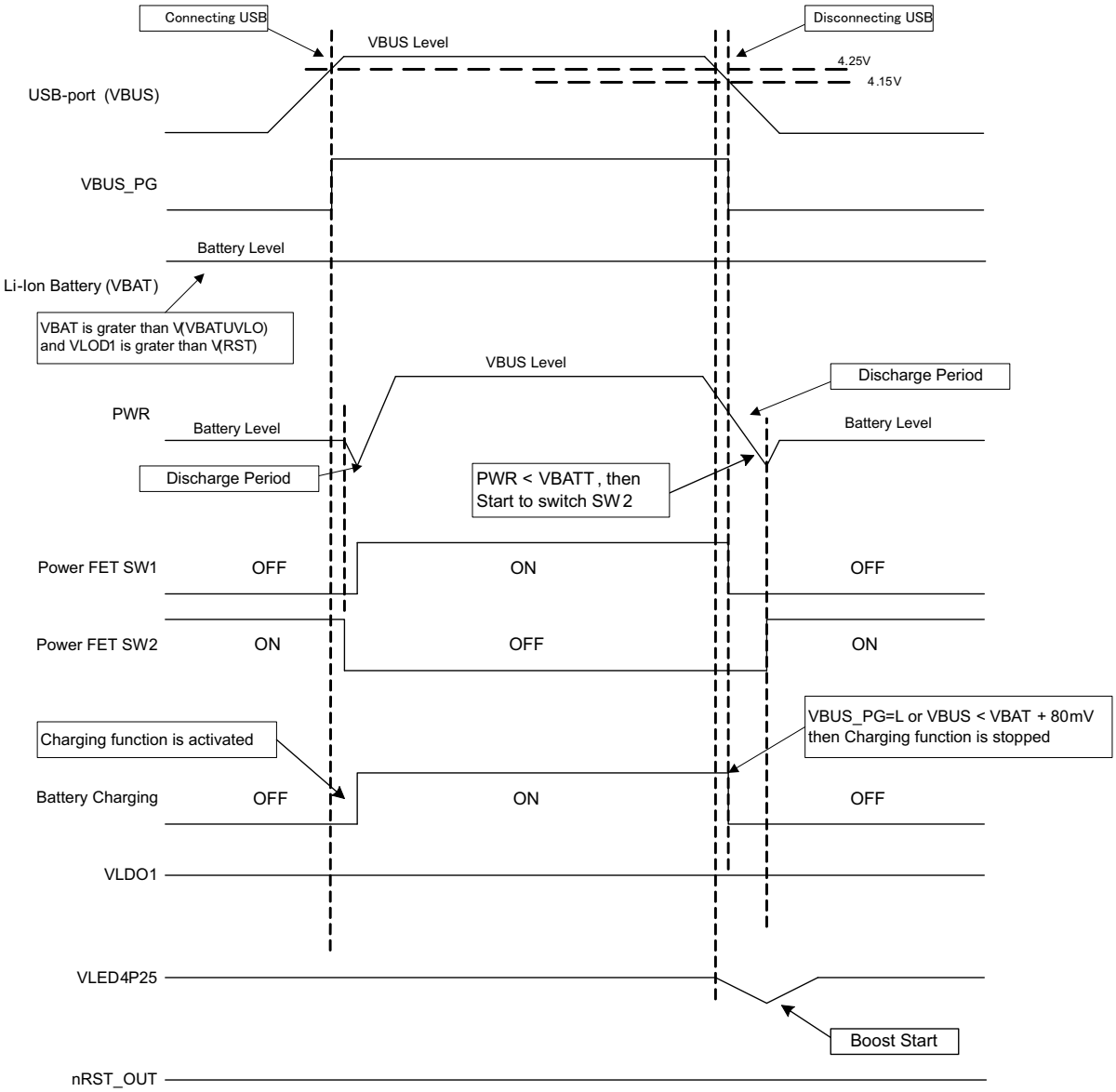



**Figure 2. USB-Port Hot-Plug During Battery Operation (#5# → #7# → #5#, Charge On, EN_VLDO = H)**

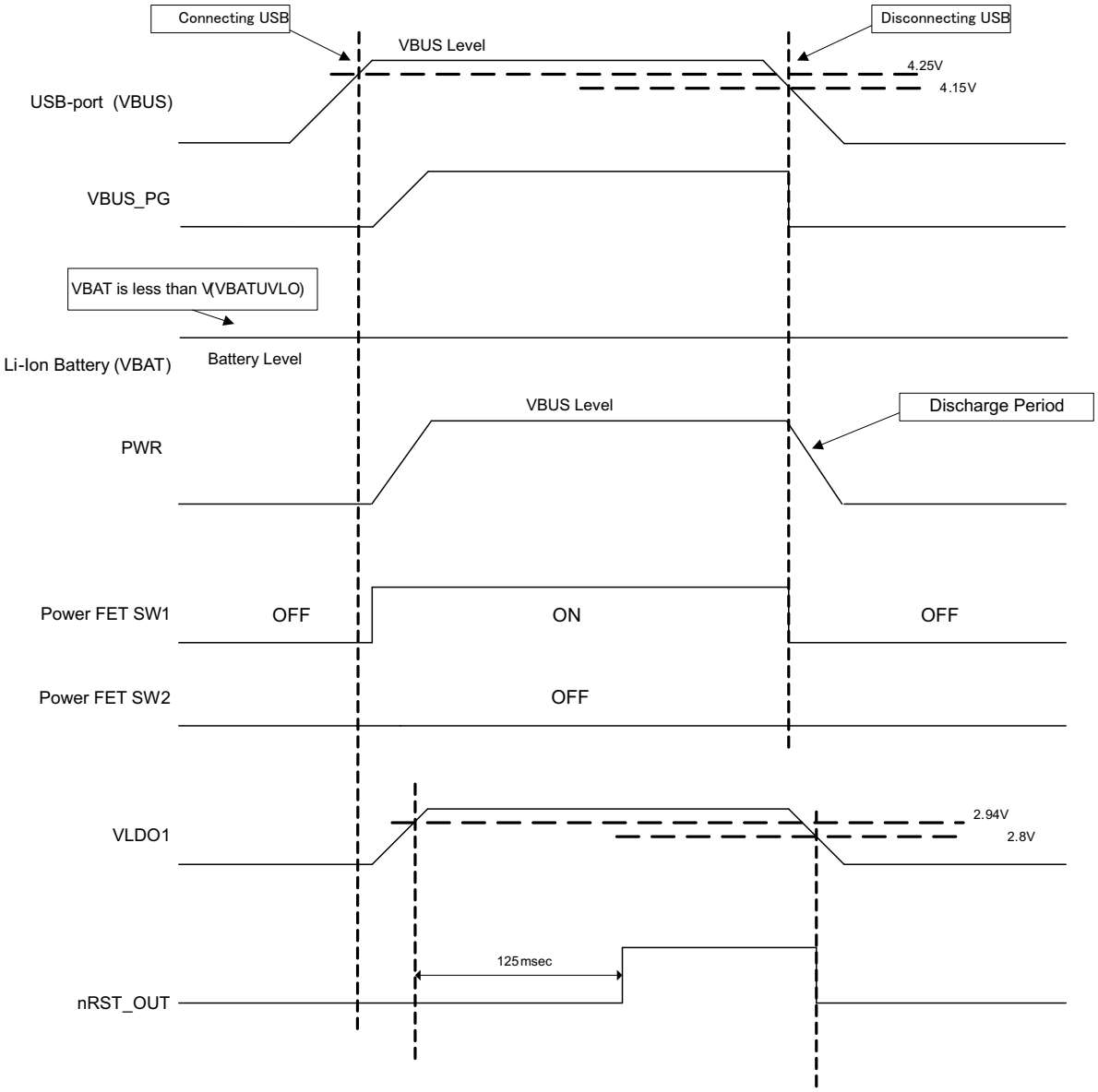



**Figure 3. USB-Port Hot-Plug (Absent Battery and VAC, #1# → #3# → #1#)**

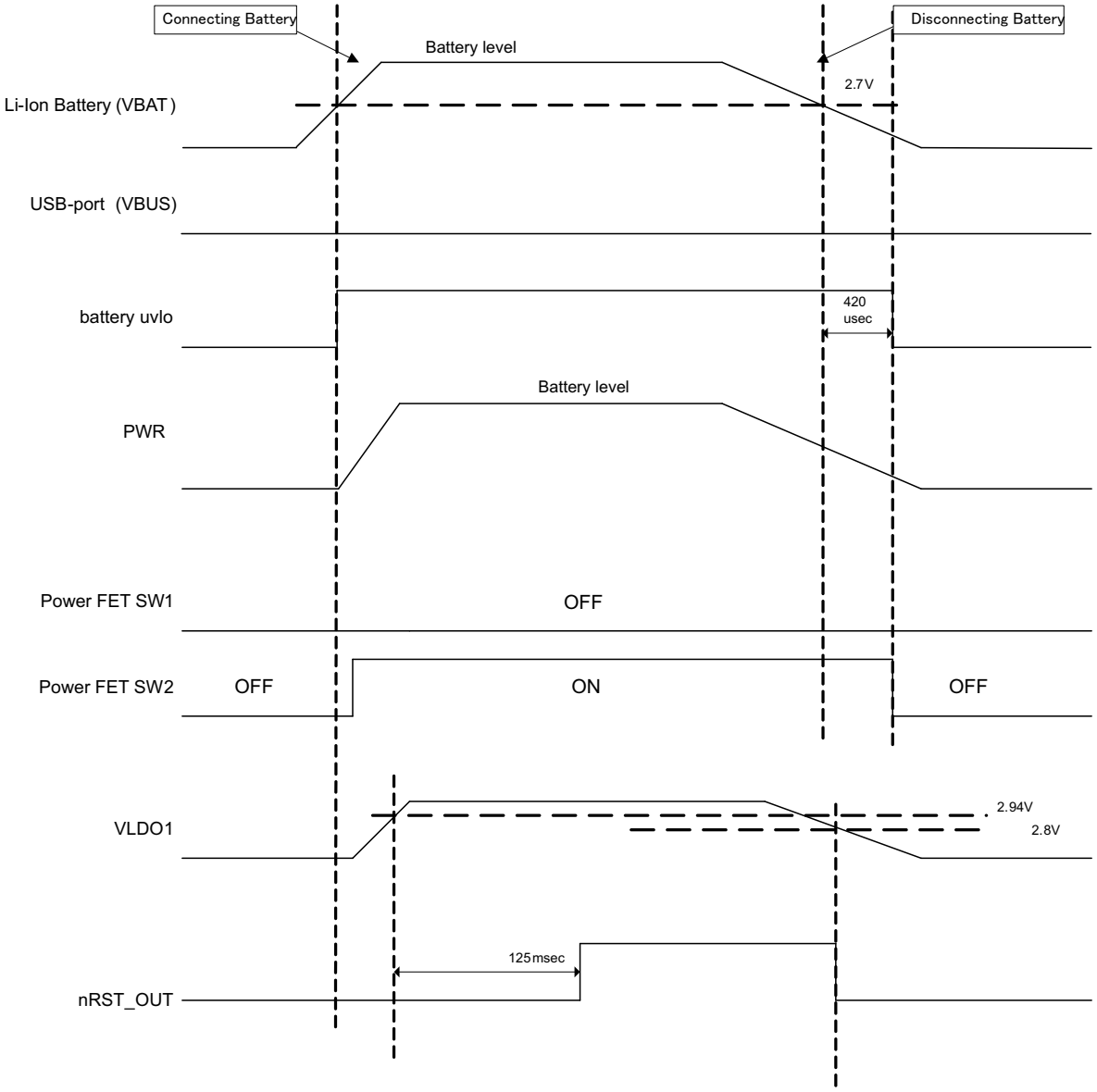



**Figure 4. Battery Hot-Plug (Absent VBUS and VAC, #1# → #5# → #1#)**

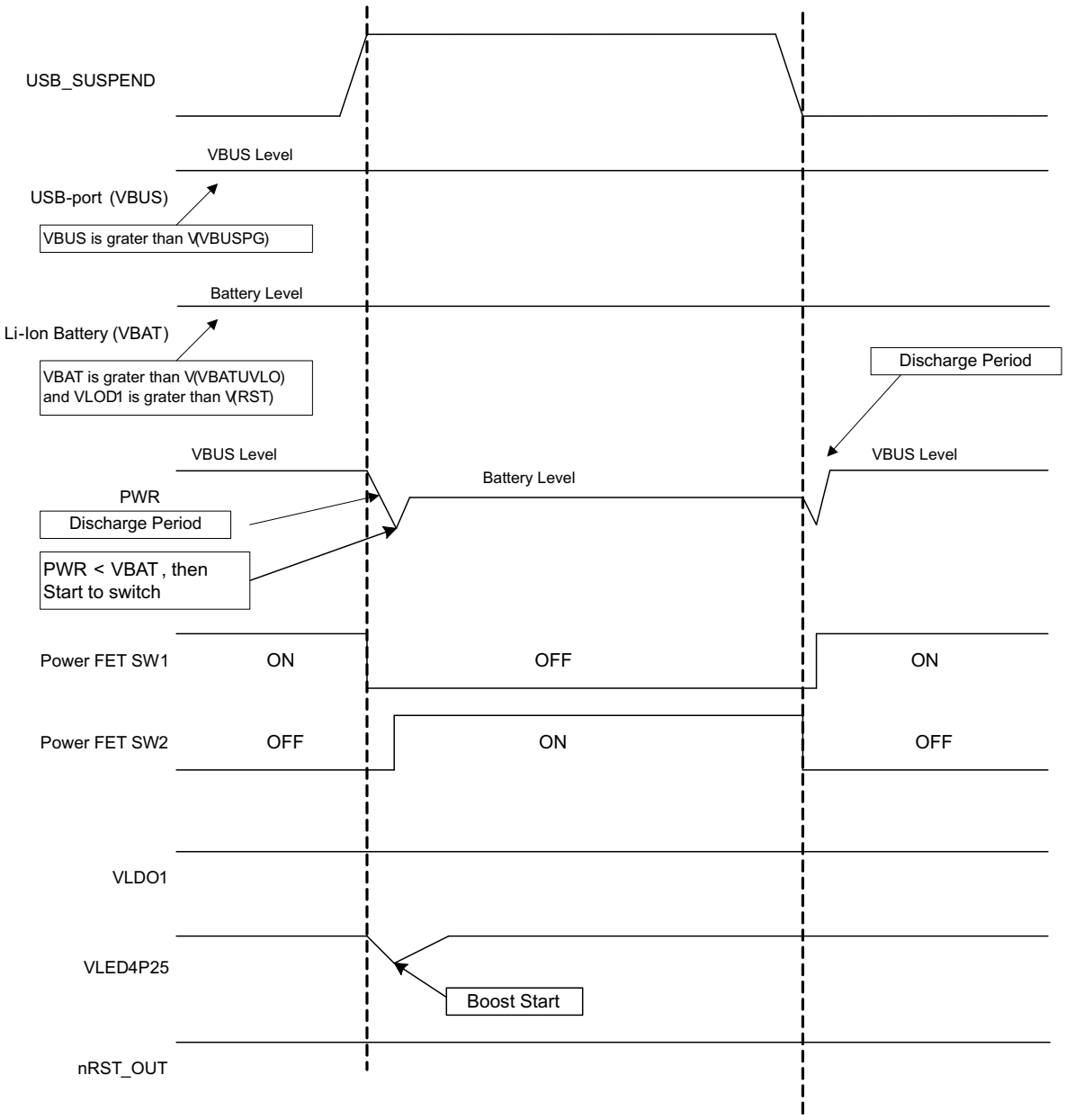
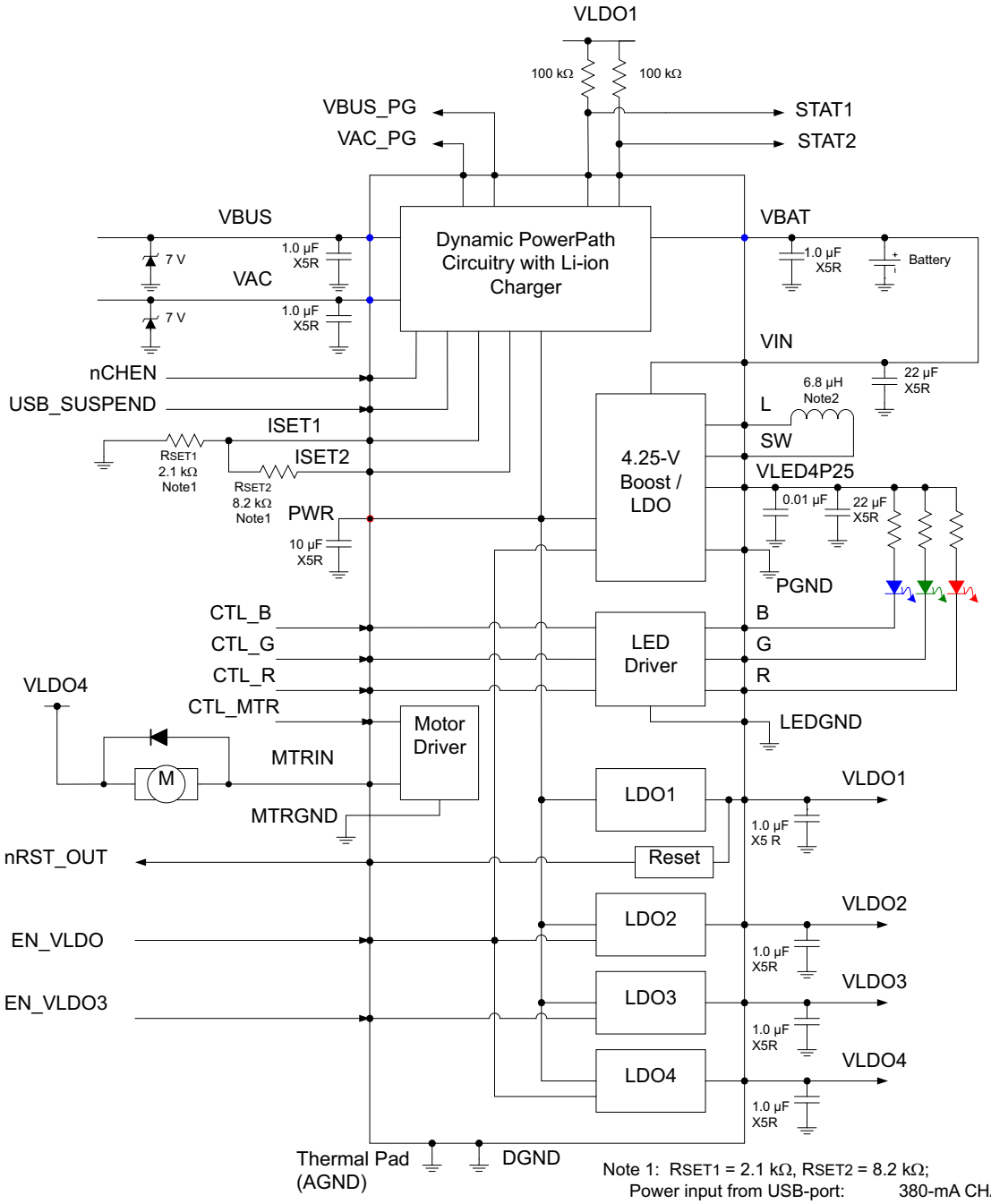



**Figure 5. USB Suspend Mode (#7# → #6# → #7#, EN_VLDO = H)**

# 7 Detailed Description

## 7.1 Functional Block Diagram




Note 1: $R_{SET1}$ = 2.1 kΩ, $R_{SET2}$ = 8.2 kΩ;
Power input from USB-port: 380-mA CHARGE CURRENT
38-mA PRE-CHARGE CURRENT
Power input from AC-DC adaptor: 480-mA CHARGE CURRENT
48-mA PRE-CHARGE CURRENT
Note 2: TAIYO YUDEN NR4018T6R8M or equivalent
These logic inputs and outputs interface are based on 3.2-V system.

## 7.2 Feature Description

### 7.2.1 Power Path Function

TPS65471 has a power-path circuitry to choose automatically any one of USB-port (VBUS), AC-DC adapter (VAC) and Li-ion battery (VBAT) as power source for LDOs.

The priority of power selection is VBUS, VAC, then VBAT. When both VBUS and VAC are available, VBUS is used as the power source of the charger and LDOs.

The exception is USB suspend mode, in this cases, power source of charger and LDOs are provided to PWR from VAC.

The VBAT (Li-ion battery) is chosen as a power source when both VBUS (USB-port) and VAC (AC-DC adapter) are not available. In this case, the linear charger function does not operate.

Figure 6 shows an equivalent circuit of the power path. Power FETs SW1, SW2 and SW3 are turned on/off per Table 1 and provide appropriate power sources to each power output.

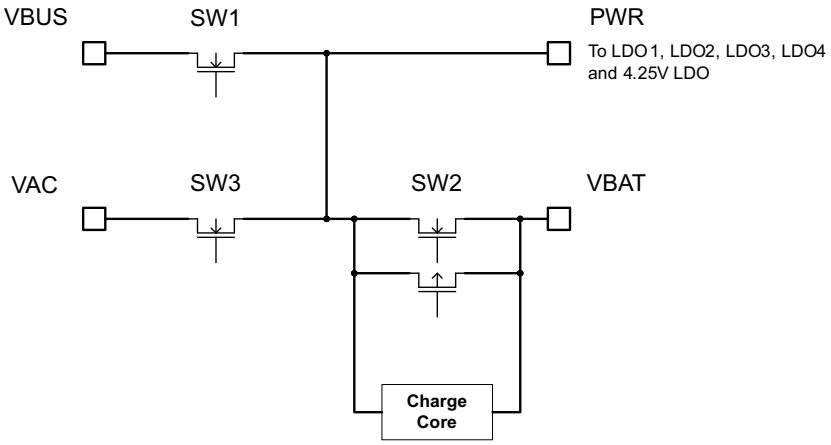



**Figure 6. Power Path Circuitry**

As Table 1 shows, the state of the linear charger circuitry depends on the state of the power path circuitry. If the power path circuitry is not ready for charging, regardless of nCHEN = L, the charger function is not turned on.

**Table 1. Power Path Circuitry Truth Table**

| AC-DC ADAPTER (VAC) | USB-PORT (VBUS) | LI-ION BATTERY (VBAT) | USB_SUSPEND | POWER SOURCE | STATE | CHARGE STATUS(1) |
|---|---|---|---|---|---|---|
| Absent | Absent | Absent | X | Non | #01# | |
| Absent | Present | Absent | H | Non | #02#(2) | |
| Absent | Present | Absent | L | VBUS | #03# | nCHEN = L: Recovery - Charge |
| Present | Absent | Absent | X | VAC | #04# | nCHEN = L: Recovery - Charge |
| Absent | Absent | Present | X | VBAT | #05# | |
| Absent | Present | Present | H | VBAT | #06# | |
| Absent | Present | Present | L | VBUS | #07# | nCHEN = L: Charge |
| Present | Absent | Present | X | VAC | #08# | nCHEN = L: Charge |
| Present | Present | Absent | H | VAC | #09# | nCHEN = L: Recovery - Charge |
| Present | Present | Absent | L | VBUS | #10# | nCHEN = L: Recovery - Charge |
| Present | Present | Present | H | VAC | #11# | nCHEN = L: Charge |
| Present | Present | Present | L | VBUS | #12# | nCHEN = L: Charge |

(1) For recovery charge, the voltage of VBAT shows the charge state below $V_{(BATUVLO)}$.
(2) At state #2#, while USB_SUSPEND = H, the 3.2-V LDO (VLDO1) is toggled. The USB_SUSPEND signal is detected after the activation of 3.2-V LDO and turns SW1 off. If the 3.2-V LDO is turned off and TPS65471 cannot detect USB_SUSPEND = H, SW1 will turn on and 3.2-V LDO is then deactivated.

### 7.2.2 USB Suspend Function

TPS65471 has USB suspend function. USB_SUSPEND = H sends TPS65471 into USB suspend mode. While in USB suspend mode, current from the USB host to the VBUS pin is reduced under the USB suspended current.

USB suspend mode does not depend on Li-ion battery status. Even if the Li-ion battery on the VBAT pin is removed or NG. VBUS, which is in USB suspend mode, does not provide electrical power for 3.2-V, 3-V and 4.25-V outputs and these outputs should be disabled.

Even in USB suspend mode, when VAC exists, source power is provided to the 3.2-V, 3-V and 4.25-V outputs from VAC.

This function complies with Table 1.

### 7.2.3 Standby Function

TPS65471 enters standby mode when the power source Li-ion battery (states #05# and #06#) and both logic inputs of EN_VLDO and EN_VLDO3 are at L level. While in standby mode, current from the Li-ion battery to the VBAT pin is reduced under $V_{VBAT(STBY)}$. The low resistance PMOS FET and NMOS FET are connected to SW2 between the PWR pin and VBAT pin in parallel. In order for the TPS65471 to decrease the power supply current, the PMOS FET operates in standby mode. In standby mode, the PMOS FET turns on corresponding to the output current of the VLDO1 voltage drop of PWR.

To recover from standby mode, the logic input of EN_VLDO or EN_VLDO3 is set to H level, then the low resistance NMOS FET connected between PWR and VBAT turns on. The startup time of the LDOs controlled by these logic input signals is approximately 1 ms.

### 7.2.4 LDO1

The TPS65471 has a 3.2-V regulator as the LDO1 power and it provides a stable and accurate voltage of 3.2 V (±64 mV). Complying with Table 1, LDO1 keeps its operation during PWR on. This LDO provides the power supply to the circuit of logic I/O. If PWR power decreases, discharge resistors at VLOD1 will be turned on and discharge power to the remaining electrode.

### 7.2.5 LDO2

The TPS65471 has a 3.2-V regulator as the LDO2 power and it provides a stable and accurate voltage of 3.2 V (±32 mV). LDO2 is controlled by logic input EN_VLDO and source of supply is PWR. This output is turned off when the EN_VLDO is L.

**Table 2. Output Control Truth Tables**

| EN_VLDO | LDO2 | LDO4 | 4.25-V BOOST/LD |
|---|---|---|---|
| H | 3.2 V (On) | 3 V (On) | 4.25 V (On) |
| L | 0 V (Off) | 0 V (Off) | 0 V (Off) |

| EN_VLDO3 | LDO3 |
|---|---|
| H | 3.2 V (On) |
| L | 0 V (Off) |

### 7.2.6 LDO3

The TPS65471 has a 3.2-V regulator as the LDO3 power and it provides a stable and accurate voltage of 3.2 V (±64 mV). LDO3 is controlled by logic input EN_VLDO3 and source of supply is PWR. This output is turned off when the EN_VLDO3 is L.

### 7.2.7 LDO4

The TPS65471 has a 3-V regulator as the LDO4 power and it provides a stable and accurate voltage of 3 V (±0.1 V). LDO4 is controlled by logic input EN_VLDO. This ouput is turned off when the EN_VLDO is L.

### 7.2.8 4.25-V Boost/LDO

The TPS65471 has a 4.25-V regulator and synchronous boost converter as the LED power. It provides a stable and accurate voltage of 4.25 V (±85 mV) connected to the VLED4P25. The boost converter is based on a fixed frequency pulse-width-modulation (PWM) controller. This output is controlled by logic input EN_VLDO. If USB-port (VBUS pin) or AC-DC adapter (VAC pin) powers are detected, the 4.25-V LDO operates (PWR supply source), and the 4.25V synchronous boost converter stops operation. If the voltage on both VBUS pin and VAC pin are less than the Power Good voltage, the power is provided to VBAT pin from the Li-ion battery, then the 4.25-V synchronous boost converter operates and the 4.25-V LDO stops operation. Complying with Table 1, in USB suspend mode (even if the voltage of VBUS pin is greater than $V_{(VBUSPG)}$) the source of supply is the battery.

### 7.2.9 R, G and B

The TPS65471 has three open-drain outputs for LED drivers. The R output is controlled by logic input CTL_R, the G output is controlled by CTL_G and the B output is controlled by CTL_B. For example, the open-drain output of R pulls low (On) when the CTL_R pin goes to H level. The open-drain output turns off when the CTL_R is L. These functions can operate when the EN_VLDO is H.

### 7.2.10 MTRIN

The TPS65471 has one open-drain output for the motor driver. The MTRIN output is controlled by logic input CTL_MTR. The open-drain output of MTRIN pulls low (On) when the CTL_MTR pin goes to H level. The open-drain output is turned off when the CTL_MTR is L.

### 7.2.11 Reset Generator

The TPS65471 monitors the status of VLDO1 (LDO1) and has reset generator circuitry to indicate a reset signal to the system.

The reset signal output is L level when the voltage of VLDO1 is less than $V_{(RST)}$, and H level when the voltage of VLDO1 is greater than $V_{(RST)}$ + 0.14 V. The Reset pin goes to H level $t_{dly(RESET)}$ after internal signal goes to H. The Reset terminal has a 100-kΩ pull-up resistor to VLDO1. Also the outputs of VLDO2, VLDO3, VDDO4 and VLED4P25 turn Off when the voltage of VLDO1 is less than $V_{(RST)}$. If VLDO1 becomes greater than $V_{(RST)}$ + 0.14 V, these outputs are turned On at the input level of each control signal.

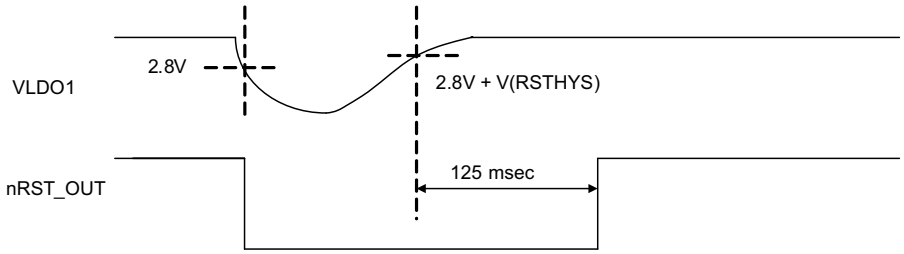



**Figure 7. Timing of nRST_OUT Signal When a Voltage Drop Occurs on VLDO1**

### 7.2.12 Charge Control

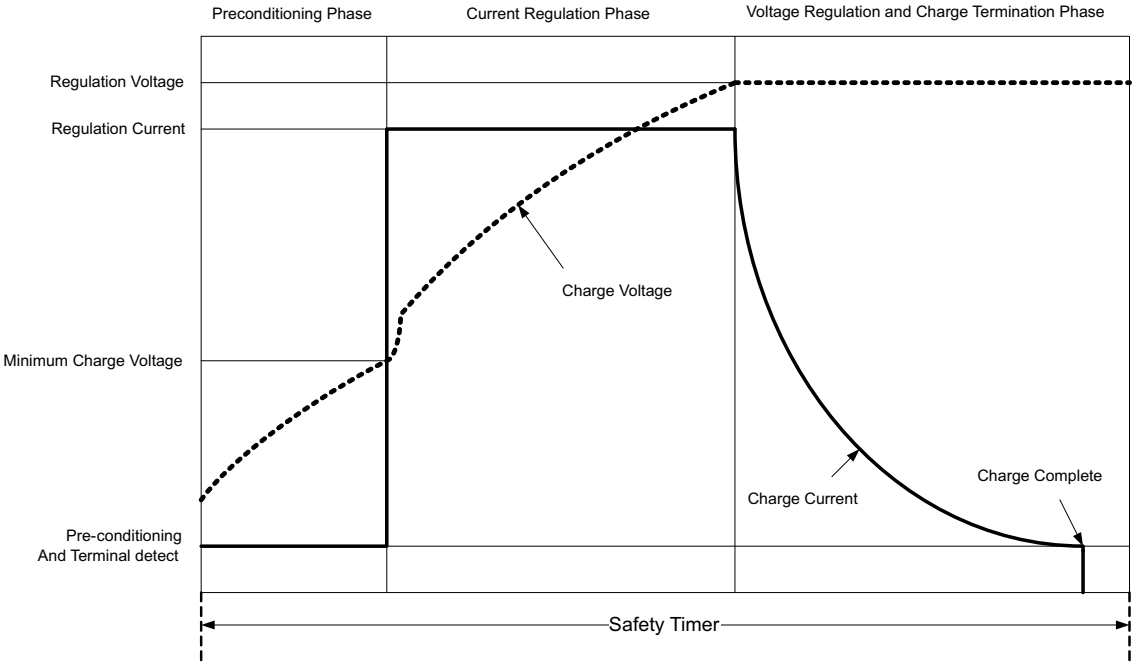



**Figure 8. Charging Profile**

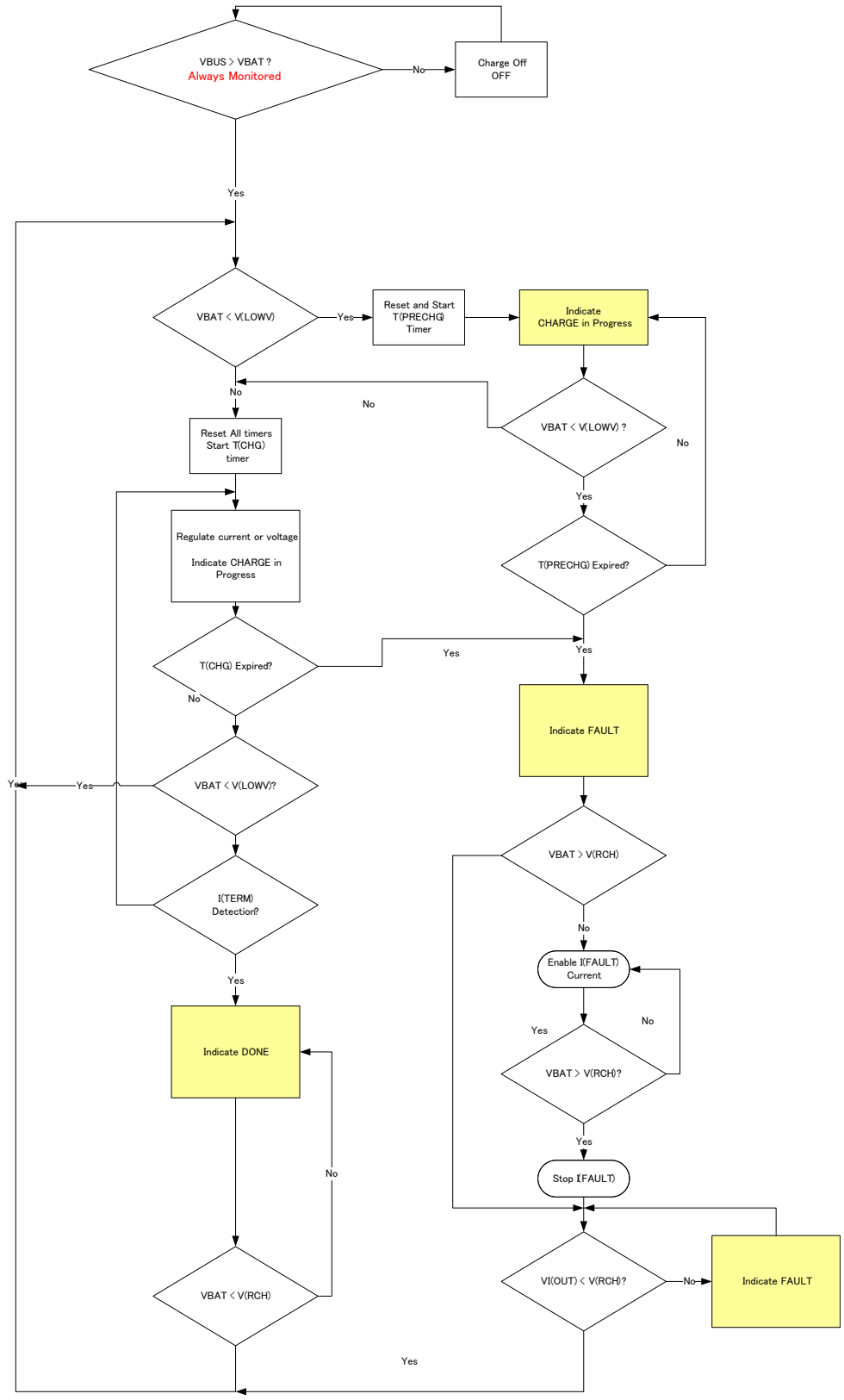



**Figure 9. Charging Flow Chart**

### 7.2.13 Battery Pre-Conditioning

During a charge cycle, if the battery voltage is below the $V_{(LOWV)}$ threshold, the device applies a pre-charge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. Resistor RSETn, connected between ISET1 and AGND an also between ISET1 and ISET2, determines the pre-charge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the Electrical Characteristics table.

$$I_{O(PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}} \quad (1)$$

TPS65471 activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If the $V_{(LOWV)}$ threshold is not reached within the timer period, the device turns off the charger and enunciates FAULT on the STATx pins. See the Timer Fault Recovery section for additional details.

### 7.2.14 Battery Fast-Charge Constant Current

The TPS65471 offers on-chip current regulation with programmable set point. Resistor, RSETn, connected between the ISET1 and AGND and also connected between ISET1 and ISET2, determines the charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the Electrical Characteristics table.

$$I_{O(OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}} \quad (2)$$

If USB-port (VBUS pin) is detected, MOS-FET of N channels connected to ISET2 turns off. The charge current is determined by the resistance of RSET1 connected between ISET1 and GND. If AC-DC adapter (VAC pin) is detected, MOS-FET of N channel connected to ISET2 turns on. The charge current is determined by the resistance of RSET1 and RSET2. When both VBUS and VAC are present, the charge current is determined by the resistance of RSET1 connected between ISET1 and AGND.

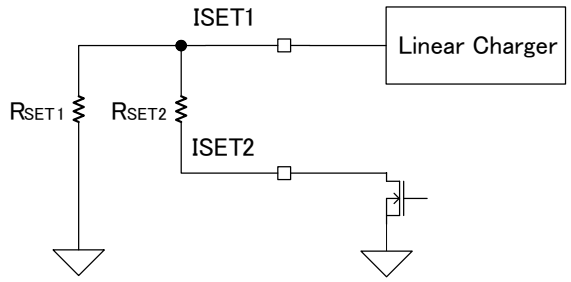



**Figure 10. Equivalent Circuit ISET1 and ISET2 Terminals**

### 7.2.15 Battery Fast-Charge Voltage Regulation

The voltage regulation feedback is through the VBAT pin. This input is tied directly to the positive side of the battery pack. The device monitors the battery-pack voltage between the VBAT and AGND pins. When the battery voltage rises to the $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to decrease.

As a safety backup, the device also monitors the charge time in charge mode. If charge is not terminated within this time period, $t_{(CHG)}$, the charger is turned off and FAULT is set on the STATx pins. See the Timer Fault and Recovery section for additional details.

### 7.2.16 Charge Termination Detection and Recharge

The TPS65471 monitors the charging current during the voltage regulation phase. Once the termination threshold, $I_{(TERM)}$, is detected, charge is terminated. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications.

$$I_{O(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}} \quad (3)$$

After charge termination, the device restarts the charge once the voltage on the VBAT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

The device monitors the charging current during the voltage regulation phase. Once the termination threshold, $I_{(TERM)}$, is detected, the charger is terminated immediately.

Resistors RSETn, connected between the ISET1 and AGND and also connected between ISET1 and ISET2, determine the current level at the termination threshold.

### 7.2.17 Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in Table 3.

These status pins can be used to communicate to the host processor. Note that this open-drain output is powered by VLDO1 and an external pull-up resistor should be applied. lso, note that OFF indicates the open-drain transistor is turns off.

**Table 3. State of STAT1/STAT2 Pins**

| CHARGE STATE | STAT1 | STAT2 |
|---|---|---|
| Pre-charge in progress | ON | ON |
| Fast charge in progress | ON | OFF |
| Charge done | OFF | ON |
| Charge suspend, Timer Fault<br>Any device state except #07#, #08#, #11#, #12# of charging | OFF | OFF |

### 7.2.18 Charge Enable Signal

The nCHEN digital input can control a state of the charger function. If nCHEN is H level, TPS65471 stops all charge functions and turns the charger off.

### 7.2.19 Timer Fault Recovery

As shown in Figure 9, the device provides a recovery method to deal with timer fault conditions. The following summarizes this method:

**Condition Number 1:** Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

**Recovery Method:** The device waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge, or battery removal. Once the battery voltage falls below the recharge threshold, the device clears the fault and starts a new charge cycle. A POR or nCHEN toggle also clears the fault.

**Condition Number 2:** Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

**Recovery Method:** Under this scenario, the device applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the device disables the $I_{(FAULT)}$ current and executes the recovery method described for Condition Number 1. Once the battery falls below the recharge threshold, the device clears the fault and starts a new charge cycle. A POR or nCHEN toggle also clears the fault.

### 7.2.20 Over Discharge Protection

TPS65471 monitors the voltage of Li-ion battery and protects it from over discharge.

If the voltage on VBAT pin is under $V_{(BATUVLO)}$, the current path from VBAT to the device is cut off and the current from the Li-ion battery will be minimized (< $I_{BAT(ODP)}$) as much as possible. This can prevent early battery degradation.

In this case, if the USB-port power source condition or AC-DC adaptor power source is good (state #03#, #04#, #09#, #10#), charge function can be enabled by nCHEN = L. Charge operation must be started from the pre-conditioning phase. When the pre-conditioning phase exceeds $V_{(BATUVLO)}$, the state of TPS65471 changes to (#07#, #08#, #11#, #12#).

### 7.2.21 Thermal Shut Down Function

When the junction temperature of TPS65471 increases higher than $T_{(SHTDWN)}$, the thermal shut down function is activated.

During a state of thermal shut down, all functions (for the charge, power paths LDO1, LDO2, LDO3, LDO4 and 4.25-V Boost/LDO) are turned off and any current is shut off. If the junction temperature decreases less than $T_{(SHTDWN)}$, (Note: -15°C (typical) hysteresis) TPS65471 goes back to normal operation. In this case, timers in the charger are not cleared. The charger timer maintains operation.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Typical Application

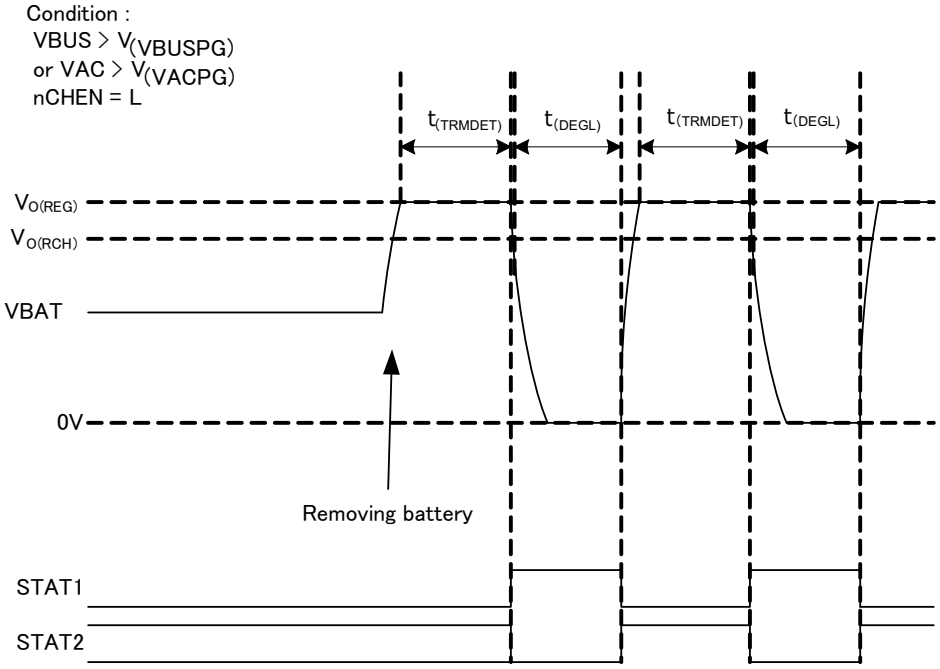



**Figure 11. VBAT Waveform When Charging Without Battery Connection**

### 8.1.1 Design Requirements

**Table 4. Recommended Inductors and Capacitors**

| PIN | PARTS | VALUE | CHARACTERISTIC | NOTE |
|---|---|---|---|---|
| VBUS | Ceramic capacitor | 1.0 µF | X5R/X7R | |
| VAC | Ceramic capacitor | 1.0 µF | X5R/X7R | |
| VBAT | Ceramic capacitor | 1.0 µF | X5R/X7R | |
| PWR | Ceramic capacitor | 10 µF | X5R/X7R | Regarding an effect of DC bias on the capacitor, select a capacitor that can secure at least 4.7 µF in worst case. |
| VLDO1 | Ceramic capacitor | 1.0 µF | X5R/X7R | |
| VLDO2 | Ceramic capacitor | 1.0 µF | X5R/X7R | |
| VLDO3 | Ceramic capacitor | 1.0 µF | X5R/X7R | |
| VLDO4 | Ceramic capacitor | 1.0 µF | X5R/X7R | |
| VLED4P25 | Ceramic capacitor | 22 µF | X5R/X7R | |
| VIN | Ceramic capacitor | 22 µF | X5R/X7R | |
| Between SW and L | Inductor | 6.8 µH | ±20% | NR4018T6R8M : TAIYO YUDEN or equivalent |

### 8.1.2 Detailed Design Procedure

#### *8.1.2.1 Behavior of the Charger Without Li-Ion Battery on VBAT Pin*

If charger function is activated without the Li-ion battery on the VBAT pin, the charger shows the below phenomenon.

1. Voltage level of VBAT pin goes to 4.2 V.
2. After $t_{(TRMDET)}$ has passed, the charger function is turned off. Then the voltage level on the VBAT pin goes to GND.
3. Since the voltage level on the VBAT pin become less than $V_{O(RCH)}$, after $t_{(DEGL)}$ turns off, the charger function is activated again.
4. Return to 1.

#### *8.1.2.2 Short Behaviors*

##### 8.1.2.2.1 VLDO1 Output Shorted to GND

If a short-circuit occurs between the 3.2-V LDO output (VLDO1) and GND, the current is limited by the LDO's current limit. If LDO is heated by the current and voltage, thermal shut down is activated (depending on ambient temperature and PCB structure).

##### 8.1.2.2.2 VLDO2, VLDO4 or VLED4P25 Output Shorted to GND

If a short-circuit occurs between the output and GND, the current is limited by the LDO's current limit. If these output terminals decrease below LVP (low voltage protection), these power outputs will be turned off and this state will be held. In addition, if any output of VLDO2 or VLDO4 or VLED4P25 is connected to GND, all the outputs controlled by the signal of EN_VLDO are turned off. Recovery method, EN_VLDO pin goes to L level at once, then goes to H level.

##### 8.1.2.2.3 VLDO3 Output Shorted to GND

If a short-circuit occurs between the 3.2-V LDO output (VLDO3) and GND, the current is limited by the LDO current limit. If this output terminal decreases below LVP, the power output will be turned off and this state will be held. Recovery method, EN_VLDO3 pin goes to L level at once, then goes to H level.

##### 8.1.2.2.4 PWR Shorted to GND

(VBAT pin) Li-ion battery provides power to PWR. If a short-circuit is detected on the PWR pin, power-path SW2 goes to high-resistance mode immediately and limits this current. If the SW2 is heated by the current and voltage, thermal shut down is activated (depending on ambient temperature and PCB structure).

(VBUS pin or VAC pin) USB-port or AC-DC adaptor power provide power to PWR. If a short-circuit is detected on the PWR pin, current flows through power-path SW1 from VBUS to PWR. This current is limited by internal current limit on SW1. Short current flow through power-path SW3 from VAC to PWR is limited by internal current limit on SW3. If SW2 or SW3 is heated by the current and voltage, thermal shut down is activated (depending on ambient temperature and PCB structure).

##### 8.1.2.2.5 VBAT Shorted to GND

If VBAT is shorted to GND, a protection IC in the battery pack will protect the battery.

# 9 Layout

## 9.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems.

1. Use wide and short traces for the main current path and for the power ground tracks without using vias if possible. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2. The input capacitor, output capacitor and the inductor should be placed as close as possible to the IC. These components should be placed on the same side of the printed circuit board. The order of placement for these components is output capacitor (VLED4P25 pin and PGND pin), inductor (L pin and SW pin), then input capacitor (VIN pin and ground plane).
3. Use of a ground plane is recommended.

Since TPS65471 provides charging current and system power with internal linear regulators, users need to consider thermal condition.

1. PowerPAD should be soldered to a thermal land on the PCB.
2. Vias on the thermal land of the PCB are necessary. This is a thermal path through the other side of the PCB.
3. A thermal pad of the same size is required on the other side of the PCB. All thermal pads should be connected by vias.
4. A metal layer should cover all of the PCB if possible.
5. Place vias to connect other sides to create thermal paths.

With these steps, the thermal resistance of TPS65471 can be lowered.

# 10 Device and Documentation Support

## 10.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 10.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 10.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 10.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65471RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-3-260C-168 HR | -10 to 125 | TPS 65471 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

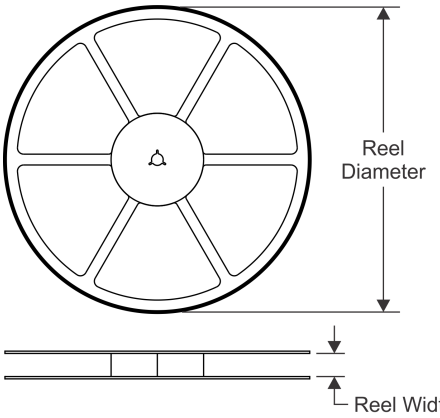
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE MATERIALS INFORMATION

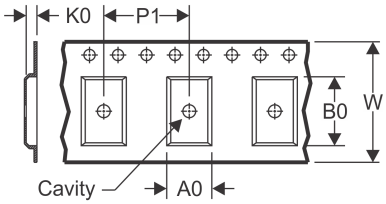


## TAPE AND REEL INFORMATION

REEL DIMENSIONS

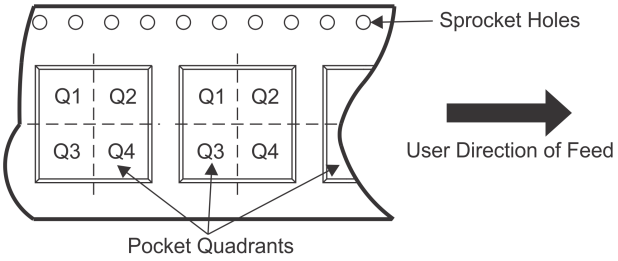



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



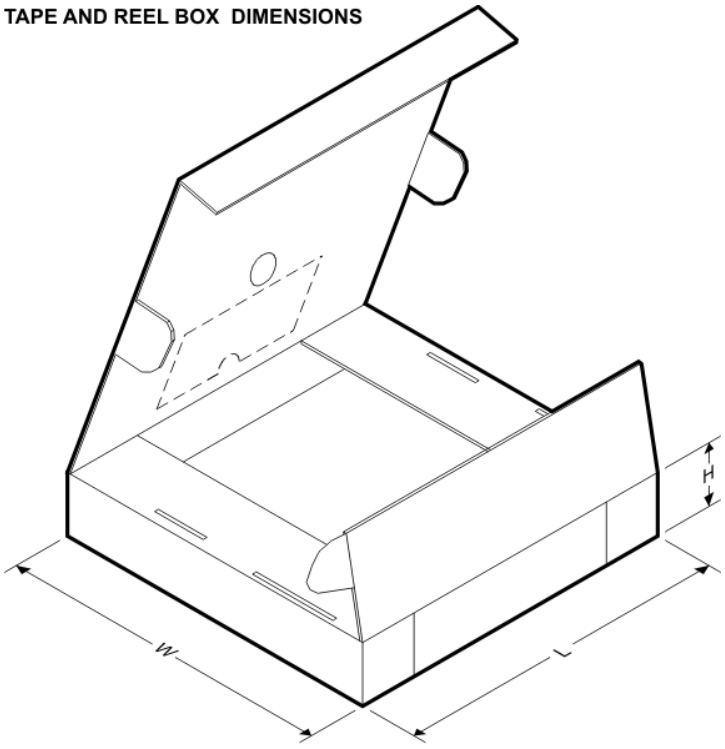

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65471RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

# PACKAGE MATERIALS INFORMATION



**TAPE AND REEL BOX DIMENSIONS**

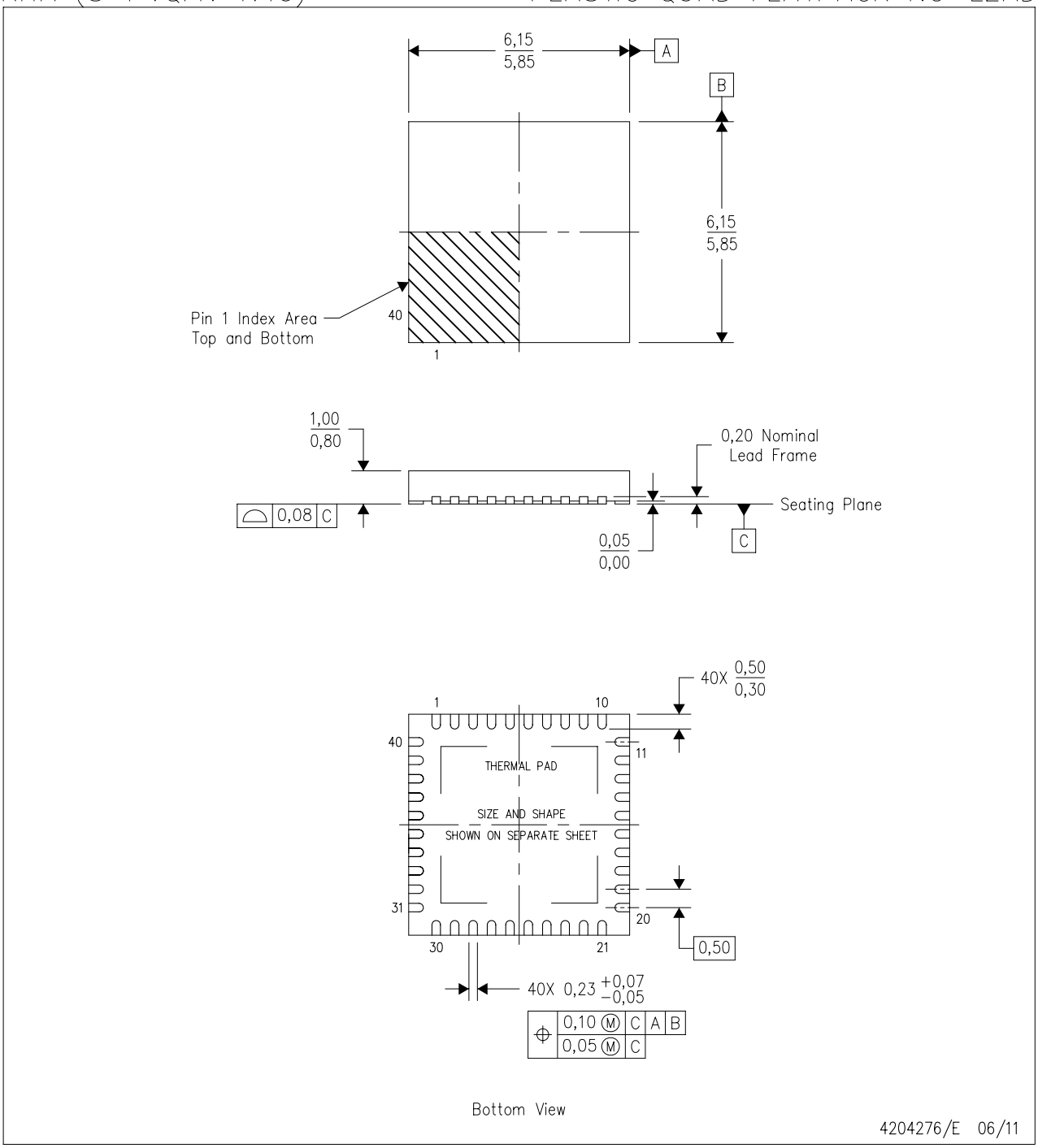



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65471RHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 38.0 |

## MECHANICAL DATA

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

# THERMAL PAD MECHANICAL DATA

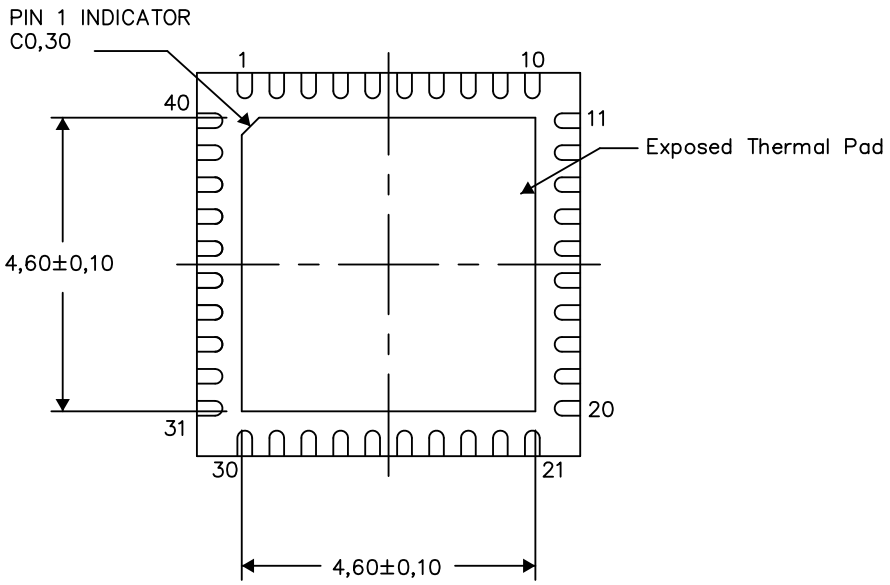
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Bottom View

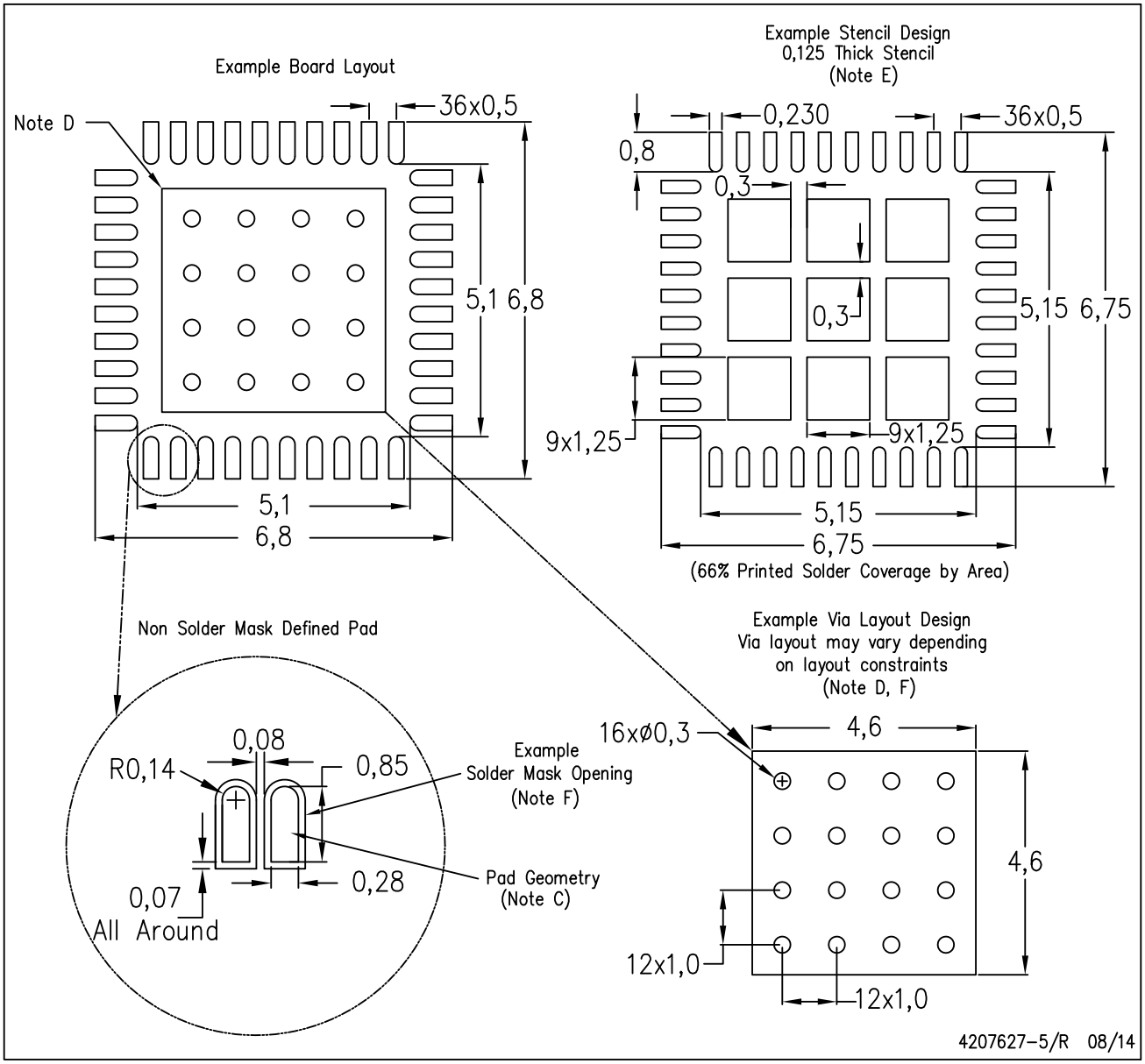
Exposed Thermal Pad Dimensions

4206355–5/X 08/14

NOTES: A. All linear dimensions are in millimeters

## LAND PATTERN DATA

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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