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**Burr-Brown Products
from Texas Instruments**

REG104



SBVS025G – SEPTEMBER 2001 – REVISED SEPTEMBER 2005

DMOS 1A Low-Dropout Regulator

FEATURES

- **NEW DMOS TOPOLOGY:**
 - Ultra Low Dropout Voltage:
230mV typ at 1A and 3.3V Output
 - Output Capacitor NOT Required for Stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE:** 33 μ V_{RMS}
- **HIGH ACCURACY:** $\pm 2\%$ max
- **HIGH EFFICIENCY:**
 - $I_{GND} = 1.7\text{mA}$ at $I_{OUT} = 1\text{A}$
 - Not Enabled: $I_{GND} = 0.5\mu\text{A}$
- **2.5V, 2.7V, 3.0V, 3.3V, 5.0V AND
ADJUSTABLE OUTPUT VERSIONS**
- **THERMAL PROTECTION**
- **SMALL SURFACE-MOUNT PACKAGES:**
SOT223-5, DDPAK-5

APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

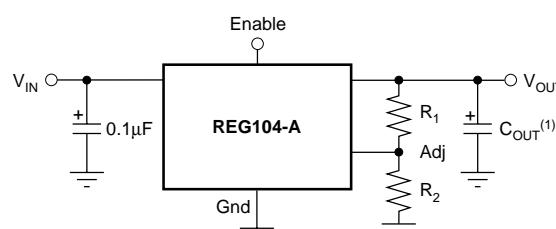
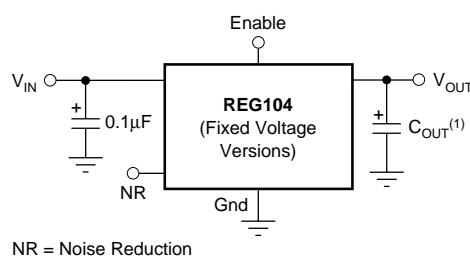
DESCRIPTION

The REG104 is a family of low-noise, low-dropout linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low dropout voltage (only 230mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1 μF .

Typical ground pin current is only 1.7mA (at $I_{OUT} = 1\text{A}$) and drops to 0.5 μA in *not enabled* mode. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG104 has very low output noise (typically 33 μ V_{RMS} for $V_{OUT} = 3.3\text{V}$ with $C_{NR} = 0.01\mu\text{F}$), making it ideal for use in portable communications equipment. On-chip trimming results in high output voltage accuracy. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (-40°C to $+85^\circ\text{C}$).

The REG104 is well protected—internal circuitry provides a current limit which protects the load from damage. Thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG104 is available in the DDPAK-5 and the SOT223-5.



NOTE: (1) Optional.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Input Voltage, V_{IN}	-0.3V to 16V
Enable Input Voltage, V_{EN}	-0.3V to V_{IN}
Feedback Voltage, V_{FB}	-0.3V to 6.0V
NR Pin Voltage, V_{NR}	-0.3V to 6.0V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	-55°C to +150°C
Lead Temperature (soldering, 3s, SOT, and DDPAK)	+240°C
ESD Rating: HBM (V_{OUT} to GND)	1.5kV
HBM (All other pins)	2kV
CDM	500V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

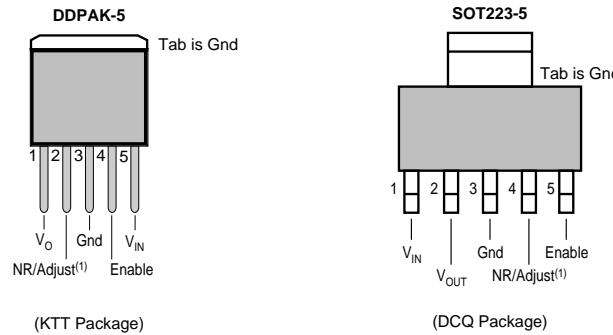
PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT}
REG104xx- <i>yyyy</i> /zzz	XX is package designator. YYYY is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable). ZZZ is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATIONS

Top View



NOTE: (1) For REG104A-A: voltage setting resistor pin.
All other models: noise reduction capacitor pin.

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REG104
SBVS025G

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$

At $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$ ($V_{OUT} = 3.0\text{V}$ for REG104-A), $V_{ENABLE} = 2\text{V}$, $I_{OUT} = 10\text{mA}$, $C_{NR} = 0.01\mu\text{F}$, and $C_{OUT} = 0.1\mu\text{F}^{(1)}$, unless otherwise noted.

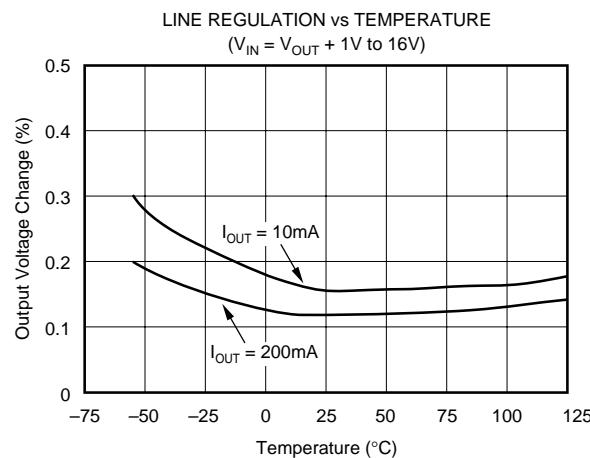
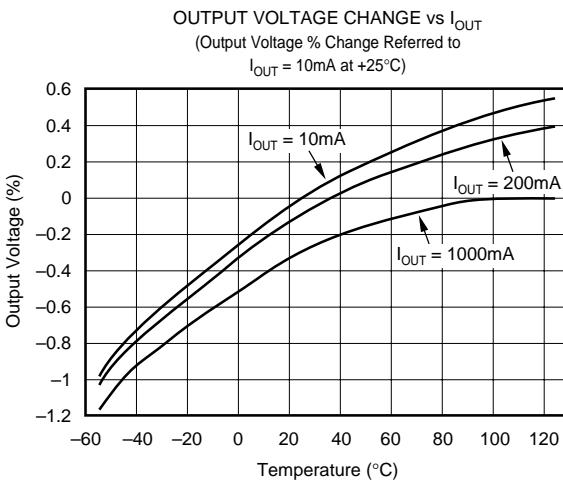
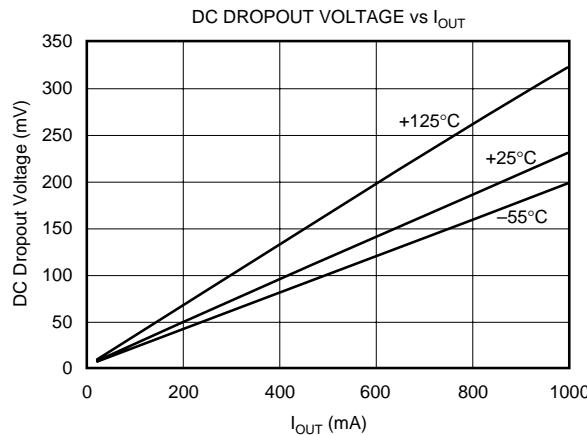
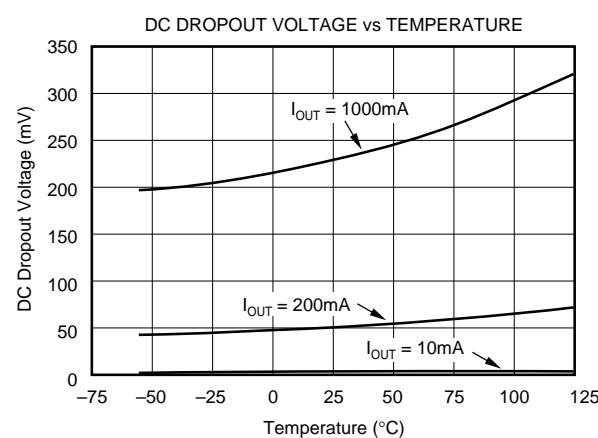
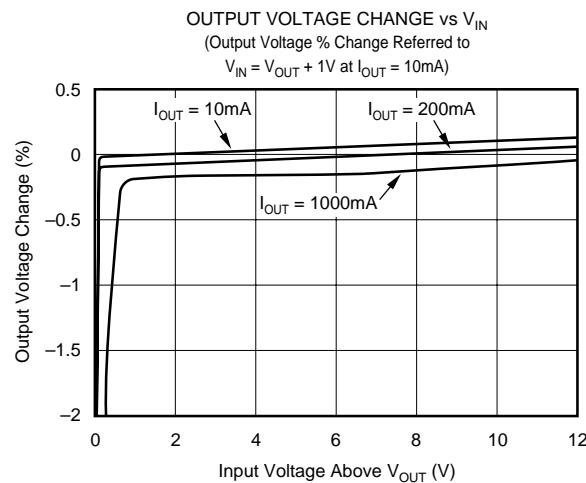
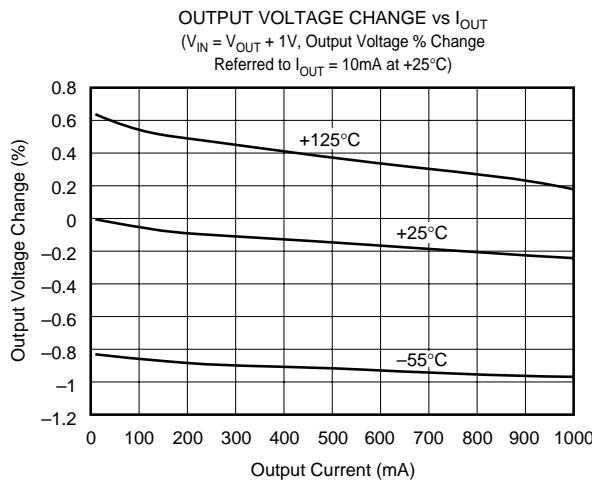
PARAMETER	CONDITION	REG104GA REG104FA			UNITS
		MIN	TYP	MAX	
OUTPUT VOLTAGE Output Voltage Range REG104-2.5 REG104-2.7 REG104-3.0 REG104-3.3 REG104-5 REG104-A Reference Voltage Adjust Pin Current Accuracy $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ vs Temperature vs Line and Load $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$	V_{OUT} V_{REF} I_{ADJ} dV_{OUT}/dT		2.5 2.7 3.0 3.3 5 1.295 0.2 ± 0.5 70 ± 0.5	5.5 1 ± 2 ± 3.0 ± 2.5 ± 3.5	V V V V V V μA %
DC DROPOUT VOLTAGE^(2, 3) For all models except 5V For 5V model For all models except 5V $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ For 5V models $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$	V_{DROP}	$I_{OUT} = 10\text{mA}$ $I_{OUT} = 1\text{A}$ $I_{OUT} = 1\text{A}$ $I_{OUT} = 1\text{A}$ $I_{OUT} = 1\text{A}$		3 230 320 480 580	mV mV mV mV
VOLTAGE NOISE $f = 10\text{Hz}$ to 100kHz Without C_{NR} (all models) With C_{NR} (all fixed voltage models)	V_n	$C_{NR} = 0, C_{OUT} = 0$ $C_{NR} = 0.01\mu\text{F}, C_{OUT} = 10\mu\text{F}$		$35\mu\text{V}_{\text{RMS}}/\text{V} \cdot V_{OUT}$ $10\mu\text{V}_{\text{RMS}}/\text{V} \cdot V_{OUT}$	μV_{RMS} μV_{RMS}
OUTPUT CURRENT Current Limit ⁽⁴⁾ $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{CL}		1.2 1.0	1.7 2.1 2.2	A A
RIPPLE REJECTION $f = 120\text{Hz}$				65	dB
ENABLE CONTROL V_{ENABLE} High (output enabled) V_{ENABLE} Low (output disabled) I_{ENABLE} High (output enabled) I_{ENABLE} Low (output disabled) Output Disable Time Output Enable Softstart Time	V_{ENABLE} I_{ENABLE}	$V_{ENABLE} = 2\text{V}$ to V_{IN} , $V_{IN} = 2.1\text{V}$ to $6.5^{(5)}$ $V_{ENABLE} = 0\text{V}$ to 0.5V	2 -0.2	0.5 1 2 50 1.5	V_{IN} 0.5 100 100 μA μs
THERMAL SHUTDOWN Junction Temperature Shutdown Reset from Shutdown				150 130	°C °C
GROUND PIN CURRENT Ground Pin Current Enable Pin Low	I_{GND}	$I_{OUT} = 10\text{mA}$ $I_{OUT} = 1\text{A}$ $V_{ENABLE} \leq 0.5\text{V}$		0.5 1.7 0.5	mA mA μA
INPUT VOLTAGE Operating Input Voltage Range ⁽⁶⁾ Specified Input Voltage Range $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$	V_{IN}	$V_{IN} > 2.7\text{V}$ $V_{IN} > 2.9\text{V}$	2.1 $V_{OUT} + 0.7$ $V_{OUT} + 0.9$	15 15 15	V V V
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance DDPAK-5 Surface Mount SOT223-5 Surface Mount	T_J θ_{JC} θ_{JC}	Junction-to-Case Junction-to-Case	-40 -55 -65	4 15	°C °C °C °C/W °C/W

NOTES: (1) The REG104 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection.

- (2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at $V_{IN} = V_{OUT} + 1\text{V}$ at fixed load.
- (3) Not applicable for V_{OUT} less than 2.7V .
- (4) Current limit is the output current that produces a 15% change in output voltage from $V_{IN} = V_{OUT} + 1\text{V}$ and $I_{OUT} = 10\text{mA}$.
- (5) For $V_{IN} > 6.5\text{V}$, see typical characteristic V_{ENABLE} vs I_{ENABLE} .
- (6) The REG104 no longer regulates when $V_{IN} < V_{OUT} + V_{DROP}(\text{MAX})$. In drop-out or when the input voltage is between 2.7V and 2.1V , the impedance from V_{IN} to V_{OUT} is typically less than 1Ω at $T_J = +25^\circ\text{C}$. See typical characteristic *Output Voltage Change* vs V_{IN} .

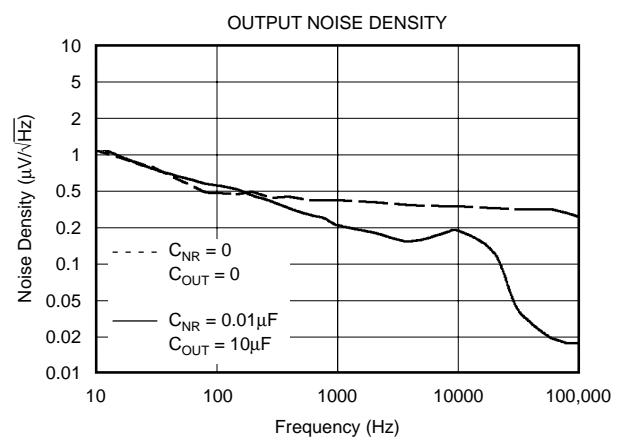
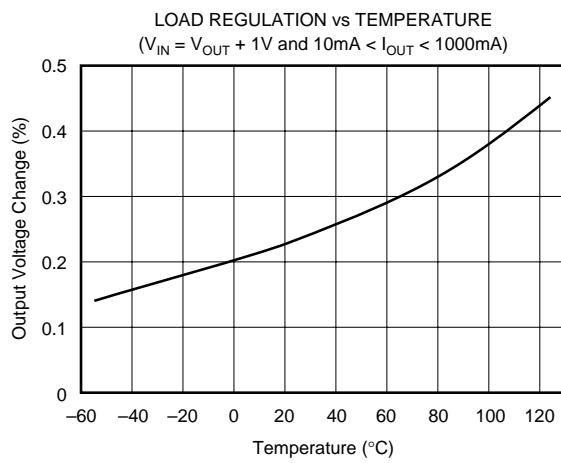
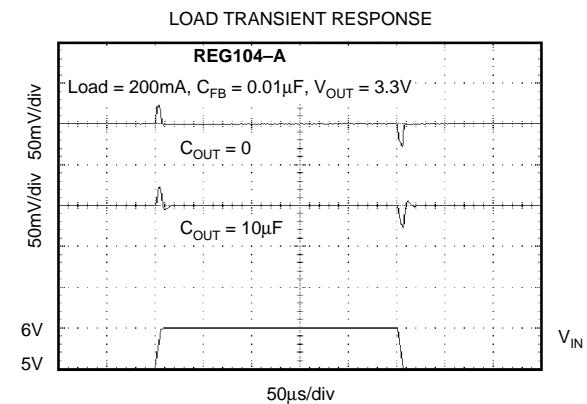
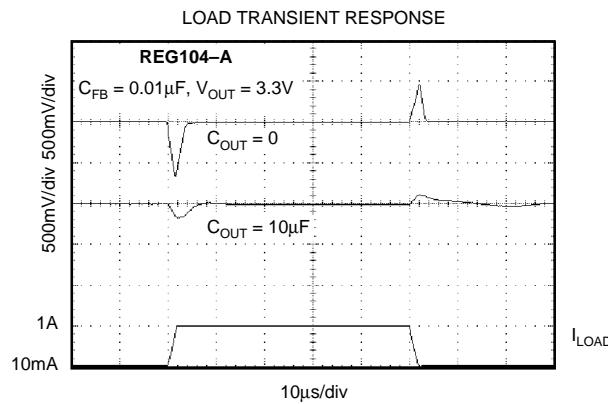
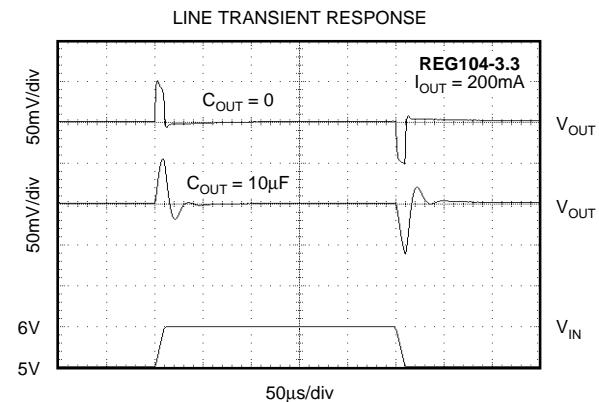
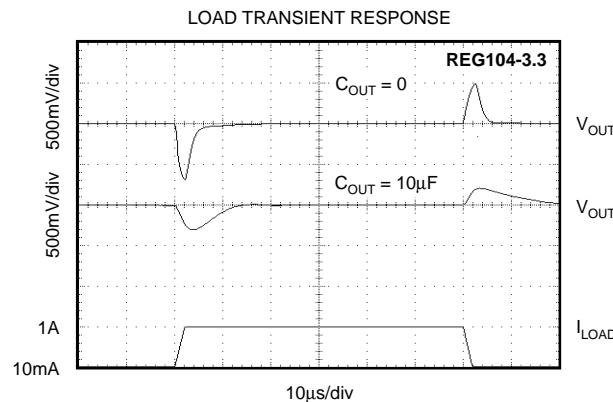
TYPICAL CHARACTERISTICS

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 2\text{V}$, unless otherwise noted.



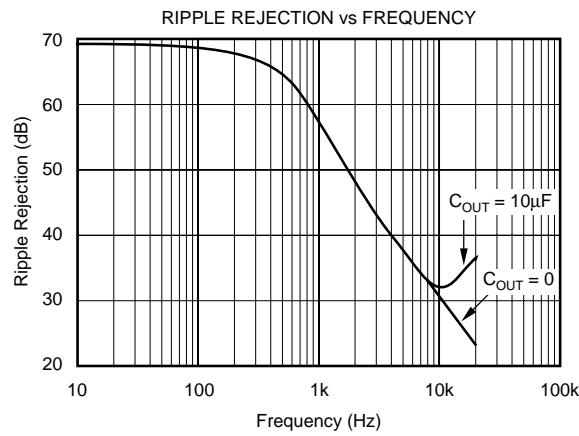
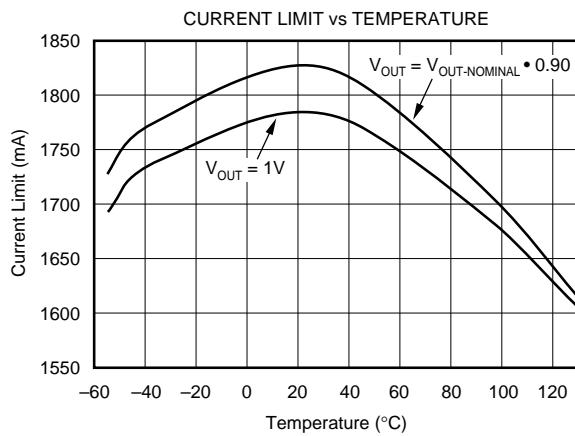
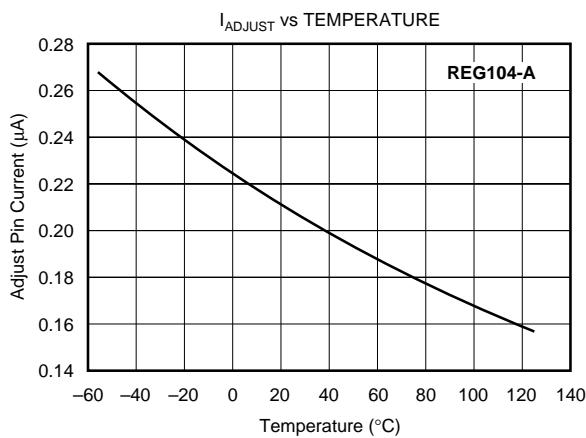
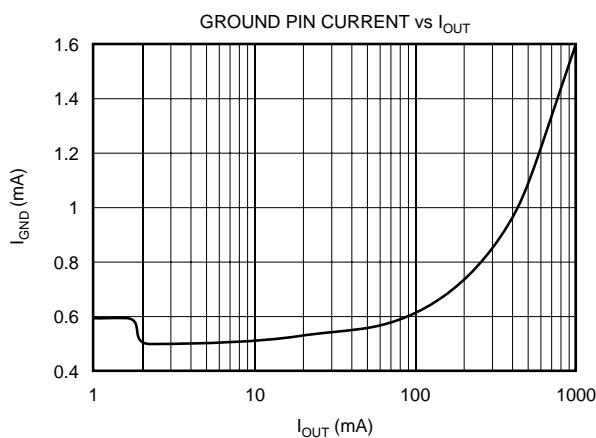
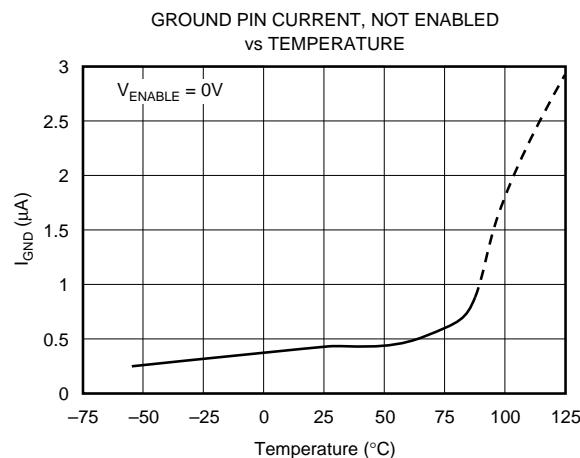
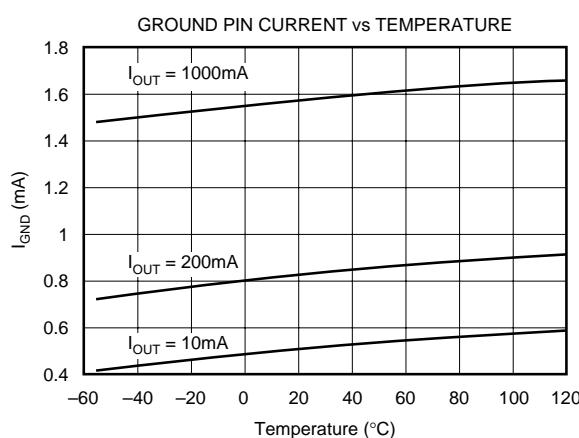
TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 2\text{V}$, unless otherwise noted.



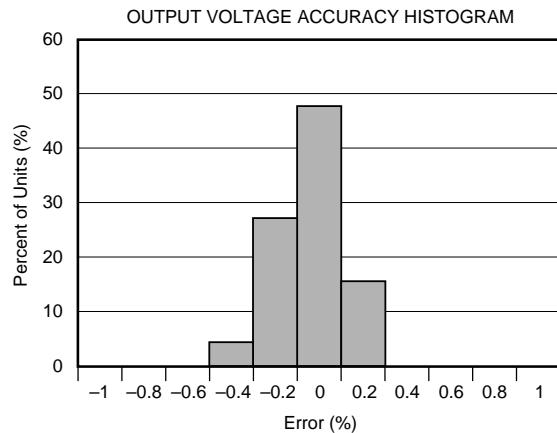
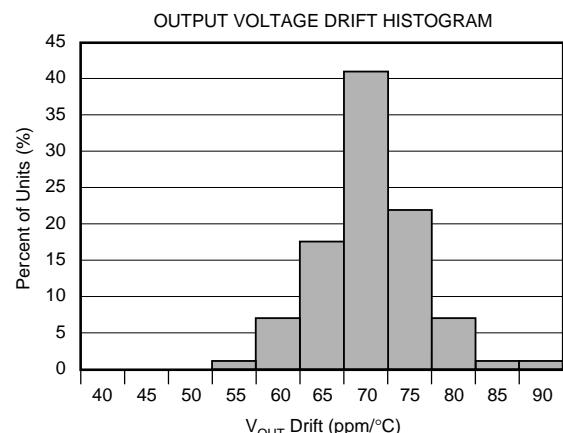
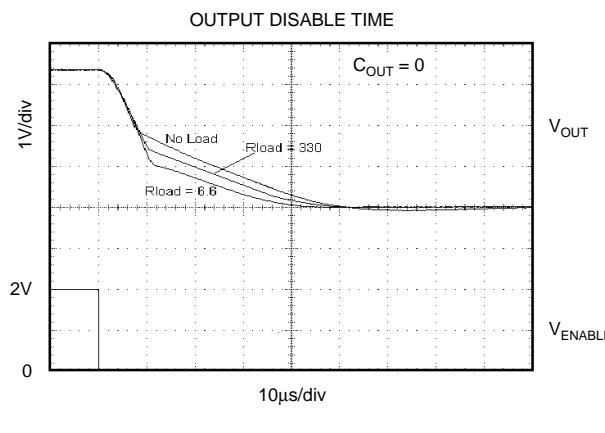
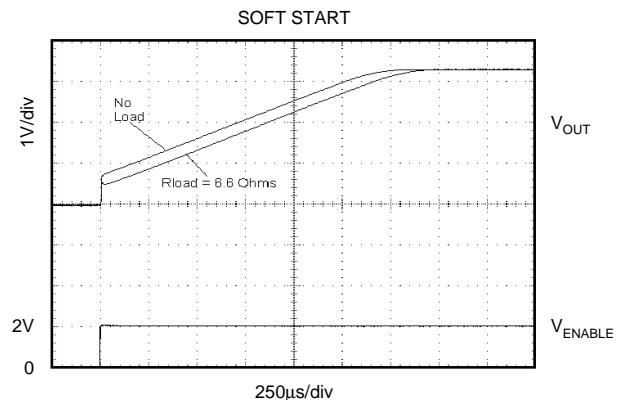
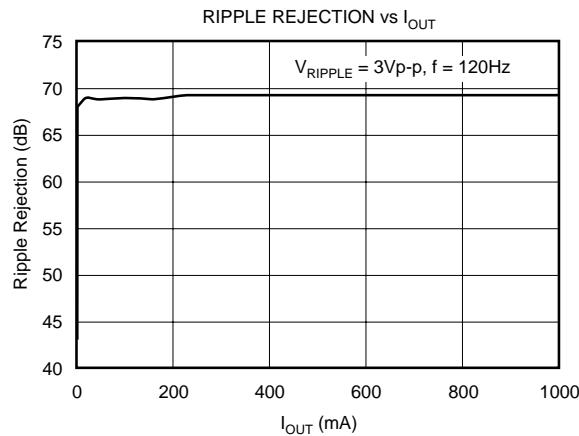
TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 2\text{V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 2\text{V}$, unless otherwise noted.



BASIC OPERATION

The REG104 series is a family of LDO (Low DropOut) linear regulators. The family includes five fixed output versions (2.5V to 5.0V) and an adjustable output version. An internal DMOS power device provides low dropout regulation with near constant ground pin current (largely independent of load and dropout conditions) and very fast line and load transient response. All versions include internal current limit and thermal shutdown circuitry.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG104A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2.

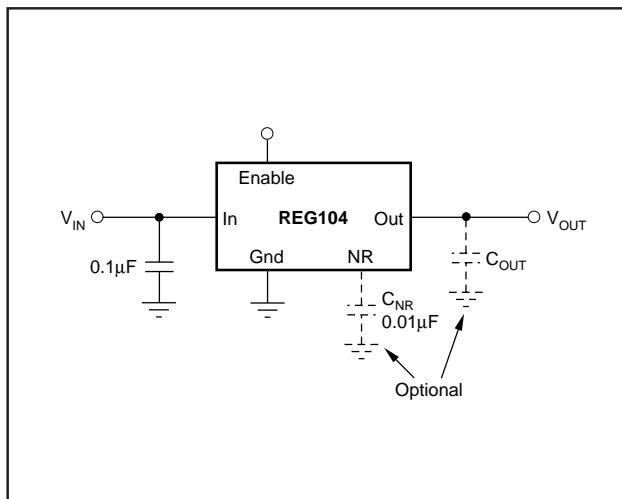


FIGURE 1. Fixed Voltage Nominal Circuit for REG104.

None of the versions require an output capacitor for regulator stability. The REG104 will accept any output capacitor type less than 1μF. For capacitance values larger than 1μF the effective ESR should be greater than 0.1Ω. This minimum ESR value includes parasitics such as printed circuit board traces, solder joints, and sockets. A minimum 0.1μF low ESR capacitor connected to the input supply voltage is recommended.

ENABLE

The Enable pin allows the regulator to be turned on and off. This pin is active HIGH and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition ground-pin current drops to approximately 0.5μA.

When not used, the Enable pin may be connected to V_{IN}. Internal to the part, the Enable pin is connected to an input resistor-zener diode circuit, as shown in Figure 3, creating a nonlinear input impedance.

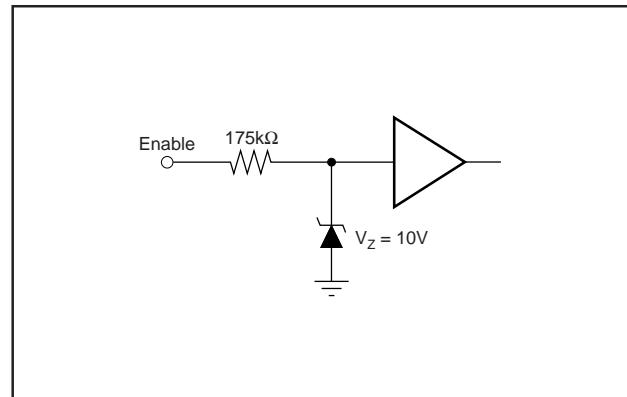


FIGURE 3. Enable Pin Equivalent Input Circuit.

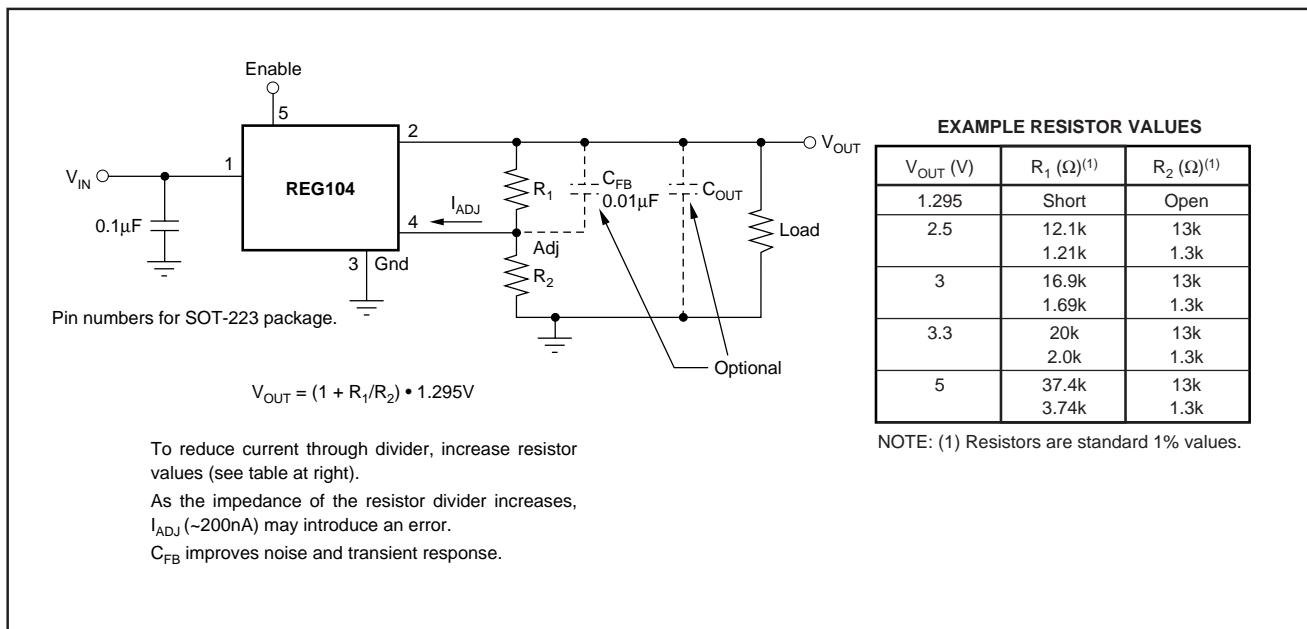


FIGURE 2. Adjustable Voltage Circuit for REG104A.

EXAMPLE RESISTOR VALUES

V _{OUT} (V)	R ₁ (Ω) ⁽¹⁾	R ₂ (Ω) ⁽¹⁾
1.295	Short	Open
2.5	12.1k	13k
	1.21k	1.3k
3	16.9k	13k
	1.69k	1.3k
3.3	20k	13k
	2.0k	1.3k
5	37.4k	13k
	3.74k	1.3k

NOTE: (1) Resistors are standard 1% values.

The Enable Pin Current versus Applied Voltage relationship is shown in Figure 4. When the Enable pin is connected to V_{IN} greater than 10V, a series resistor may be used to limit the current.

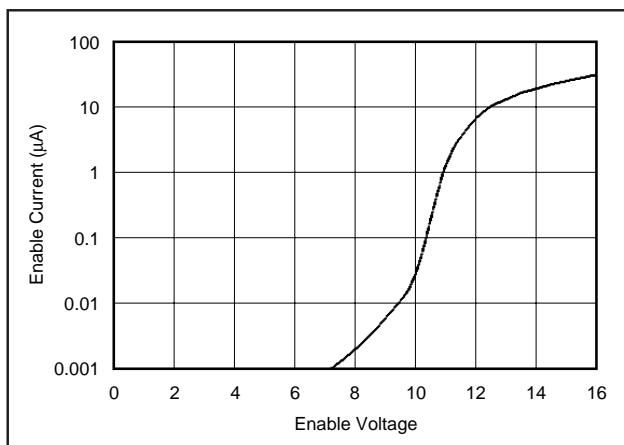


FIGURE 4. Enable Pin Current versus Applied Voltage.

OUTPUT NOISE

A precision band-gap reference is used for the internal reference voltage, V_{REF} , for the REG104. This reference is the dominant noise source within the REG104. It generates approximately $45\mu V_{RMS}$ in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 45\mu V_{RMS} \frac{R_1 + R_2}{R_2} = 45\mu V_{RMS} \cdot \frac{V_{OUT}}{V_{REF}}$$

Since the value of V_{REF} is 1.295V, this relationship reduces to:

$$V_N = 35 \frac{\mu V_{RMS}}{V} \cdot V_{OUT}$$

Connecting a capacitor, C_{NR} , from the Noise-Reduction (NR) pin to ground can reduce the output noise voltage. Adding C_{NR} , as shown in Figure 5, forms a low-pass filter for the voltage reference. For $C_{NR} = 10nF$, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 3.5. This noise reduction effect is shown in Figure 6.

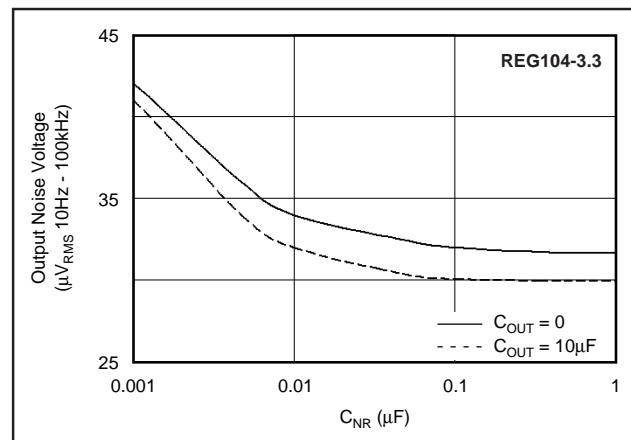


FIGURE 6. Output Noise versus Noise Reduction Capacitor.

The REG104 adjustable version does not have the noise-reduction pin available, however, the adjust pin is the summing junction of the error amplifier. A capacitor, C_{FB} ,

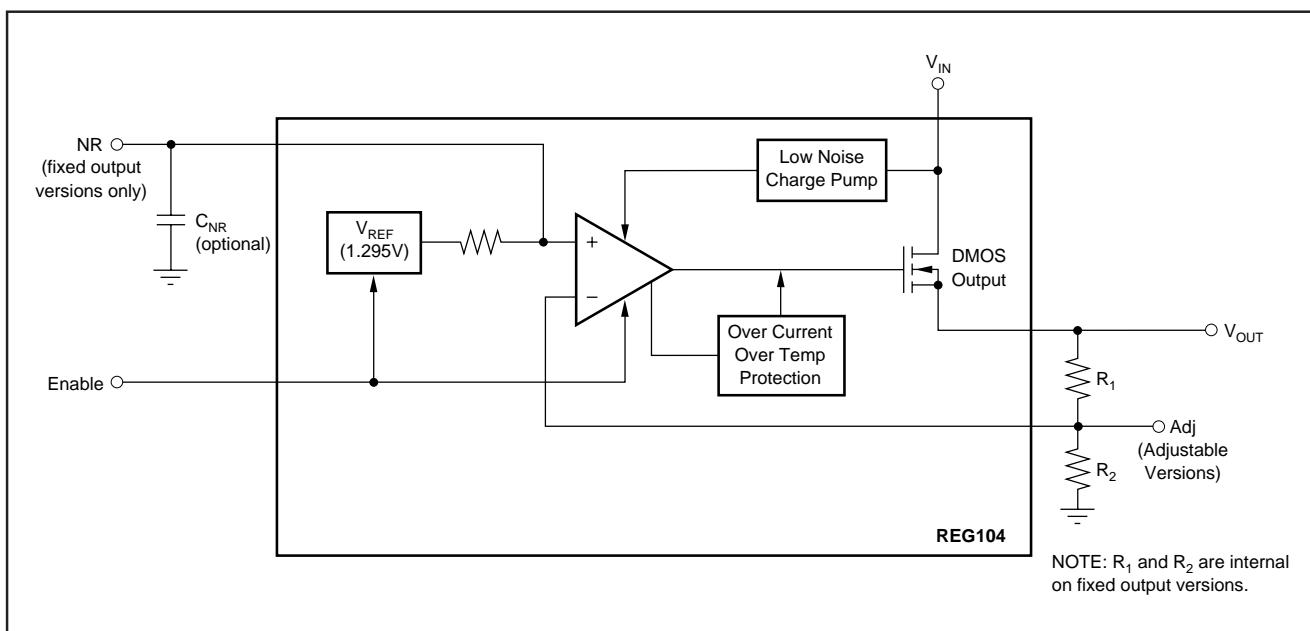


FIGURE 5. Block Diagram.

connected from the output to the adjust pin will reduce both the output noise and the peak error from a load transient. Figure 7 shows improved output noise performance for two capacitor combinations.

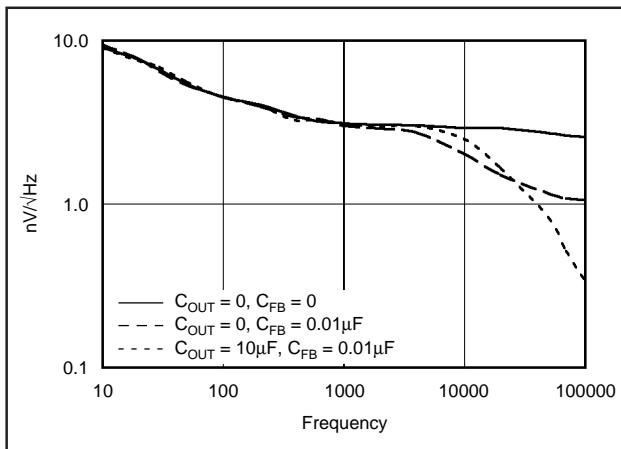


FIGURE 7. Output Noise Density on Adjustable Versions.

The REG104 utilizes an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above V_{IN} . The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator.

DROP-OUT VOLTAGE

The REG104 uses an N-channel DMOS as the pass element. When the input voltage is within a few hundred millivolts of the output voltage, the DMOS device behaves like a resistor. Therefore, for low values of V_{IN} to V_{OUT} , the regulator's input-to-output resistance is the $R_{DS(ON)}$ of the DMOS pass element (typically 230mΩ). For static (DC) loads, the REG104 will typically maintain regulation down to V_{IN} to V_{OUT} voltage drop of 230mV at full rated output current. In Figure 8, the bottom line (DC dropout) shows the minimum V_{IN} to V_{OUT} voltage drop required to prevent dropout under DC load conditions.

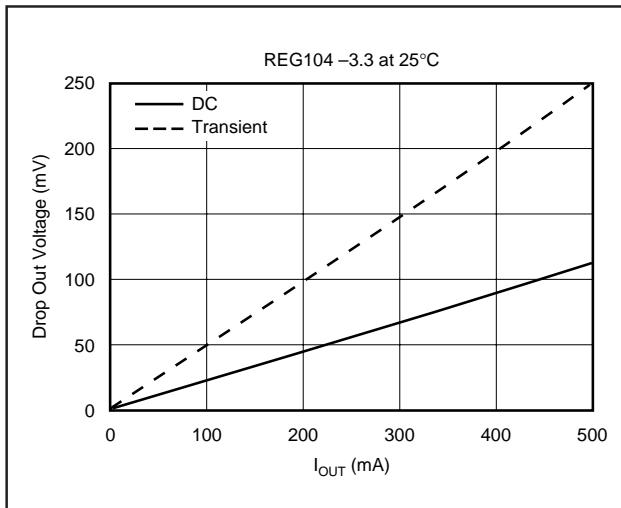


FIGURE 8. Transient and DC Dropout.

For large step changes in load current, the REG104 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this *transient dropout* region is shown as the top line in Figure 8. Values of V_{IN} to V_{OUT} voltage drop above this line insure normal transient response.

In the transient dropout region between *DC* and *Transient*, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available *headroom* V_{IN} to V_{OUT} voltage drop. Under worst-case conditions (full-scale load change with V_{IN} to V_{OUT} voltage drop close to DC dropout levels), the REG104 can take several hundred microseconds to re-enter the specified window of regulation.

TRANSIENT RESPONSE

The REG104 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 10nF) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor, C_{FB} (nominal value 10nF), from the output to the adjust pin will also improve the transient response.

THERMAL PROTECTION

Power dissipated within the REG104 will cause the junction temperature to rise. The REG104 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 150°C, allowing the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG104 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the REG104 into thermal shutdown will degrade reliability.

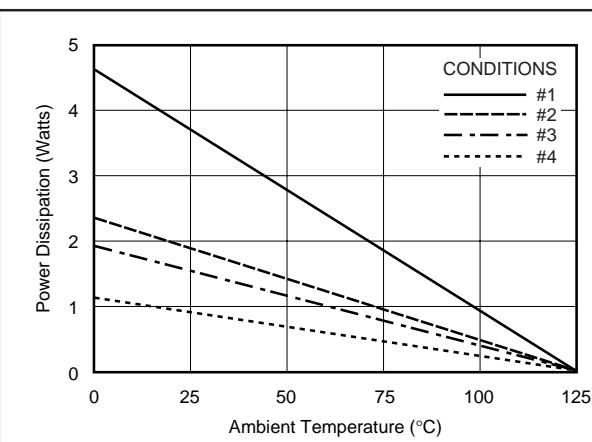
POWER DISSIPATION

The REG104 is available in two different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. While it is difficult to impossible to quantify all of the variables in a thermal design of this type, performance data for several configurations are shown in Figure 9. In all cases the PCB copper area is bare copper, free of solder resist mask, and not solder plated. All examples are for 1-ounce copper. Using heavier copper will increase the effectiveness in moving the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the average output current times the voltage across the output element, V_{IN} to V_{OUT} voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT(AVG)}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.



CONDITION	PACKAGE	PCB AREA	θ_{JA}
1	DDPAK	4in ² Top Side Only	27°C/W
2	SOT-223	4in ² Top Side Only	53°C/W
3	DDPAK	None	65°C/W
4	SOT-223	0.5in ² Top Side Only	110°C/W

FIGURE 9. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

REGULATOR MOUNTING

The tab of both packages is electrically connected to ground. For best thermal performance, the tab of the DDPAK surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation. Figure 10 shows typical thermal resistance from junction to ambient as a function of the copper area for the DDPAK. Figure 11 shows the same relationship for the SOT-223.

Although the tabs of the DDPAK and the SOT-223 are electrically grounded, they are not intended to carry any current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the various REG104 devices are presented in the Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015A), available from the Texas Instruments web site (www.ti.com).

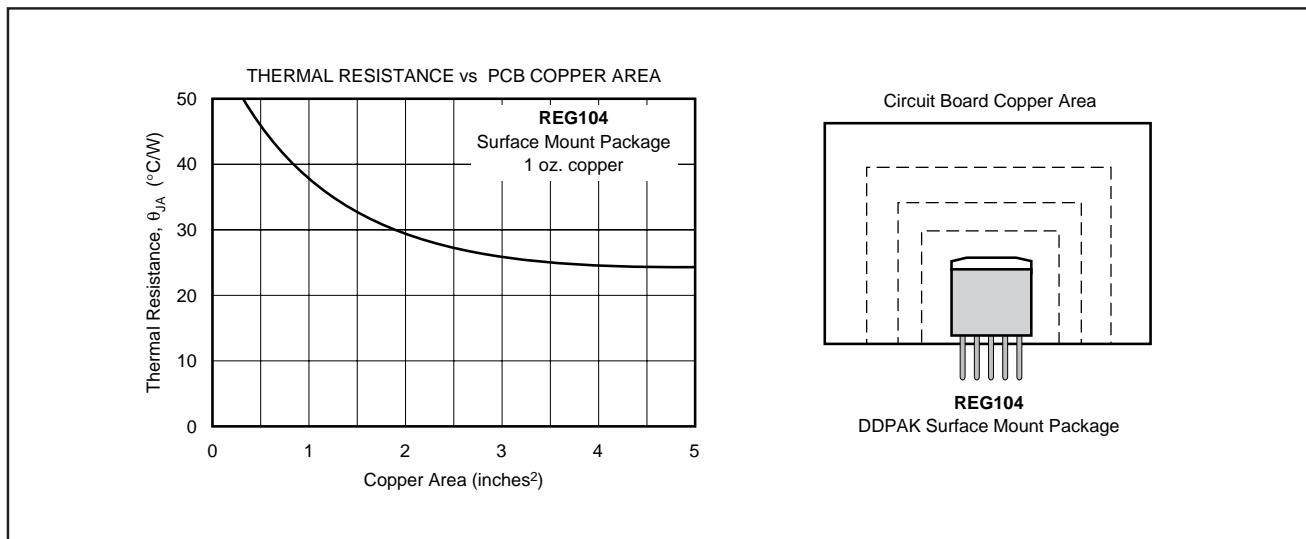


FIGURE 10. Thermal Resistance versus PCB Area for the Five-Lead DDPAK.

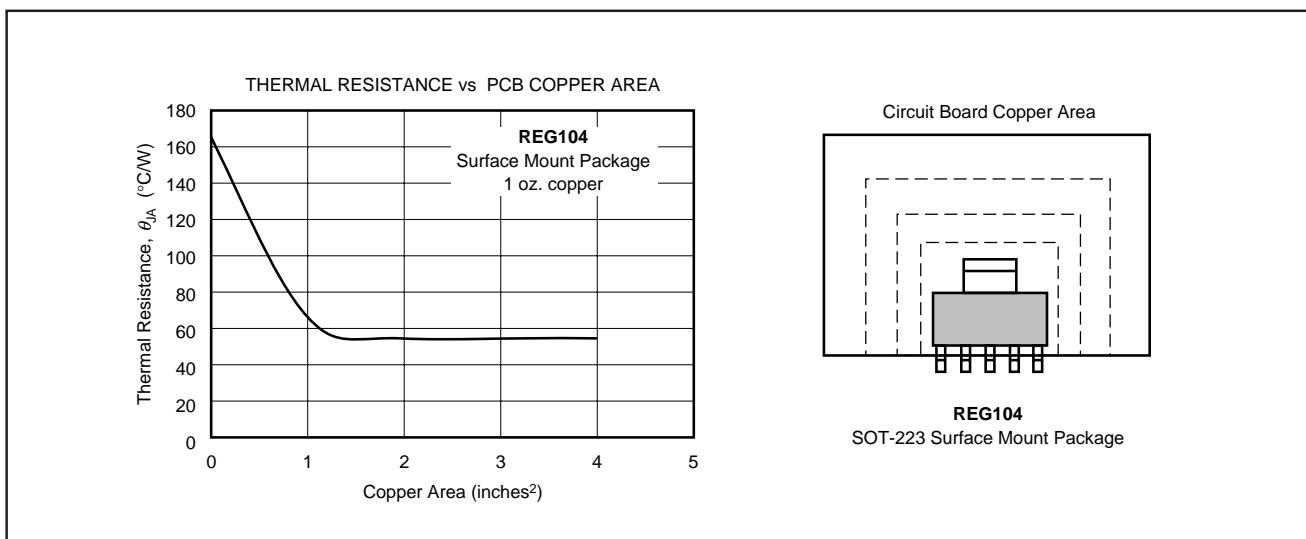


FIGURE 11. Thermal Resistance versus PCB Area for the Five Lead SOT-223.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG104FA-2.5	OBsolete	DDPAK/ TO-263	KT	5		TBD	Call TI	Call TI			
REG104FA-2.5/500	ACTIVE	DDPAK/ TO-263	KT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-2.5	Samples
REG104FA-2.5/500G3	ACTIVE	DDPAK/ TO-263	KT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-2.5	Samples
REG104FA-2.5KTTT	ACTIVE	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-2.5	Samples
REG104FA-2.5KTTTG3	ACTIVE	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-2.5	Samples
REG104FA-2.7	OBsolete	DDPAK/ TO-263	KT	5		TBD	Call TI	Call TI			
REG104FA-3	OBsolete	DDPAK/ TO-263	KT	5		TBD	Call TI	Call TI			
REG104FA-3.3	OBsolete	DDPAK/ TO-263	KT	5		TBD	Call TI	Call TI			
REG104FA-3.3/500	ACTIVE	DDPAK/ TO-263	KT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-3.3	Samples
REG104FA-3.3/500G3	ACTIVE	DDPAK/ TO-263	KT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-3.3	Samples
REG104FA-3.3KTTT	ACTIVE	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-3.3	Samples
REG104FA-3.3KTTTG3	ACTIVE	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-3.3	Samples
REG104FA-3KTTT	NRND	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-3	
REG104FA-3KTTTG3	NRND	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-3	
REG104FA-5	OBsolete	DDPAK/ TO-263	KT	5		TBD	Call TI	Call TI			
REG104FA-5/500	ACTIVE	DDPAK/ TO-263	KT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-5	Samples
REG104FA-5/500G3	ACTIVE	DDPAK/ TO-263	KT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-5	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG104FA-5KTTT	ACTIVE	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-5	Samples
REG104FA-5KTTTG3	ACTIVE	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		REG 104FA-5	Samples
REG104FA-A	OBSOLETE	DDPAK/ TO-263	KT	5		TBD	Call TI	Call TI			
REG104FA-A/500	ACTIVE	DDPAK/ TO-263	KT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	REG 104FA-A	Samples
REG104FA-A/500G3	ACTIVE	DDPAK/ TO-263	KT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	REG 104FA-A	Samples
REG104FA-AKTTT	ACTIVE	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	REG 104FA-A	Samples
REG104FA-AKTTTG3	ACTIVE	DDPAK/ TO-263	KT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	REG 104FA-A	Samples
REG104GA-2.5	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		R104G25	Samples
REG104GA-2.5/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		R104G25	Samples
REG104GA-2.5G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		R104G25	Samples
REG104GA-3	NRND	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		R104G30	
REG104GA-3.3	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		R104G33	Samples
REG104GA-3.3/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R104G33	Samples
REG104GA-3.3/2K5G4	ACTIVE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 85		Samples
REG104GA-3.3G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		R104G33	Samples
REG104GA-3G4	NRND	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		R104G30	
REG104GA-5	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		R104G50	Samples
REG104GA-5/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	R104G50	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG104GA-5/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R104G50	Samples
REG104GA-5G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		R104G50	Samples
REG104GA-A	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	R104GA	Samples
REG104GA-A/2K5	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-2-260C-1 YEAR	-40 to 85	R104GA	Samples
REG104GA-A/2K5G4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	R104GA	Samples
REG104GA-AG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R104GA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

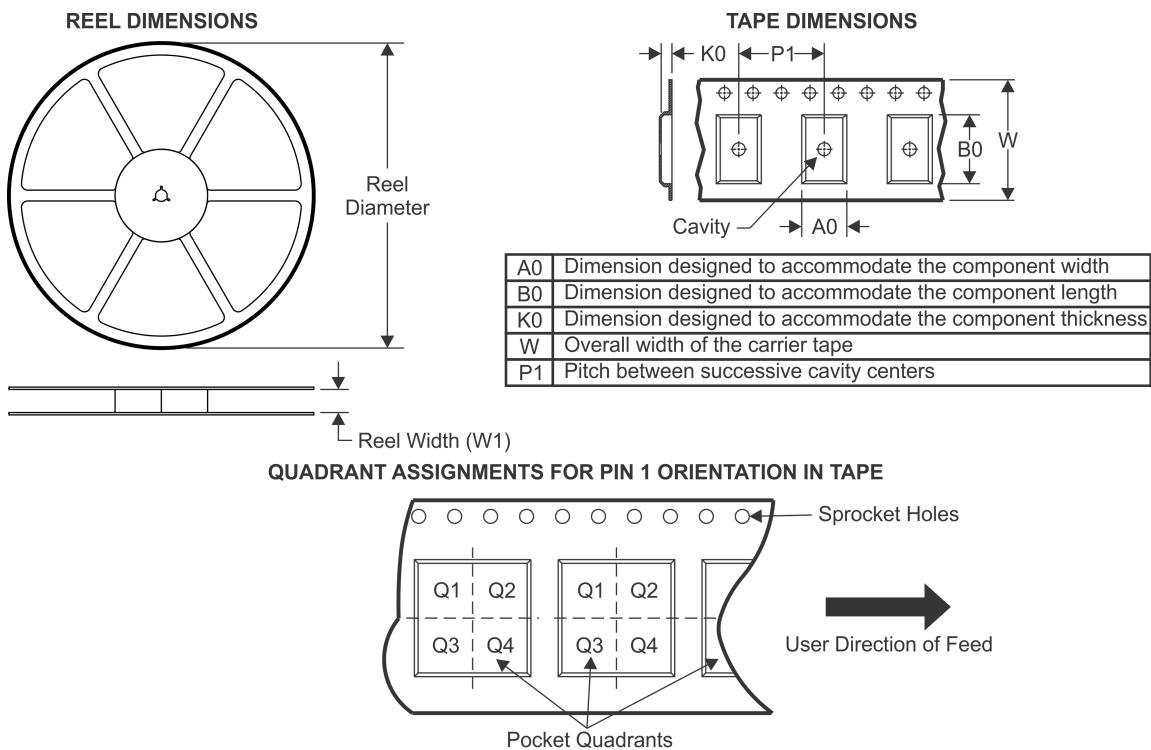
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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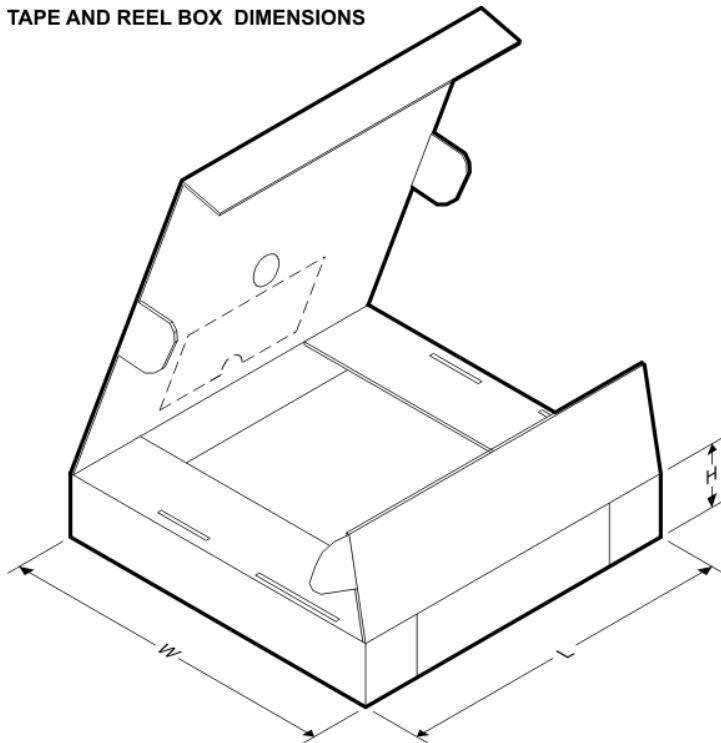


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG104FA-2.5/500	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG104FA-2.5KTTT	DDPAK/TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG104FA-3.3/500	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG104FA-3.3KTTT	DDPAK/TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG104FA-3KTTT	DDPAK/TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG104FA-5/500	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG104FA-5KTTT	DDPAK/TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG104FA-A/500	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG104FA-AKTTT	DDPAK/TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG104GA-2.5/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG104GA-3.3/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG104GA-5/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG104GA-5/2K5G4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG104GA-A/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG104GA-A/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG104FA-2.5/500	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
REG104FA-2.5KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
REG104FA-3.3/500	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
REG104FA-3.3KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
REG104FA-3KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
REG104FA-5/500	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
REG104FA-5KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
REG104FA-A/500	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
REG104FA-AKTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
REG104GA-2.5/2K5	SOT-223	DCQ	6	2500	406.0	348.0	63.0
REG104GA-3.3/2K5	SOT-223	DCQ	6	2500	358.0	335.0	35.0
REG104GA-5/2K5	SOT-223	DCQ	6	2500	367.0	367.0	35.0
REG104GA-5/2K5G4	SOT-223	DCQ	6	2500	358.0	335.0	35.0
REG104GA-A/2K5	SOT-223	DCQ	6	2500	406.0	348.0	63.0

**PACKAGE MATERIALS INFORMATION**

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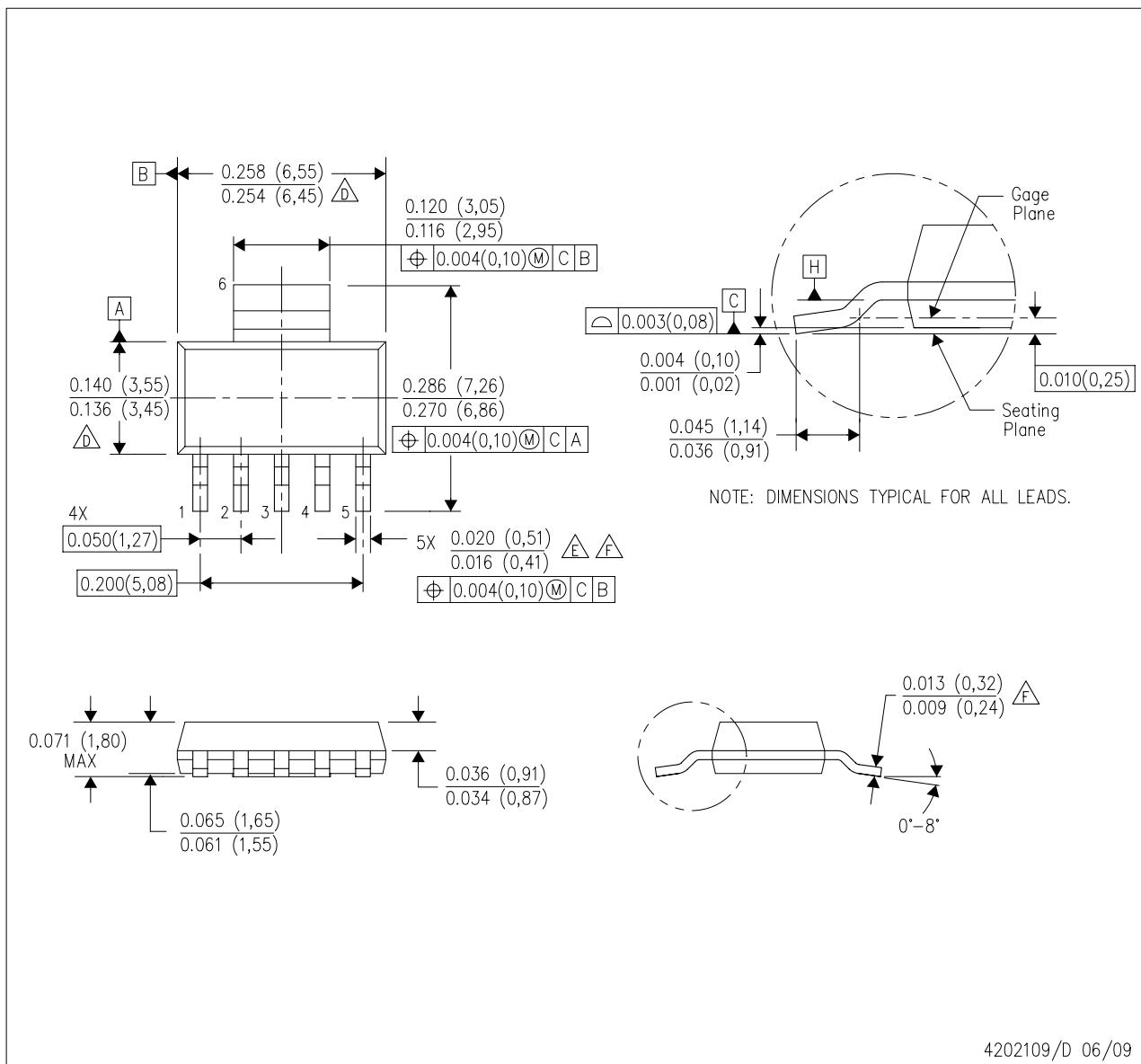
29-Apr-2016

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG104GA-A/2K5	SOT-223	DCQ	6	2500	367.0	367.0	35.0

MECHANICAL DATA

DCQ (R-PDSO-G6)

PLASTIC SMALL-OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Controlling dimension in inches.

Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

Lead width dimension does not include dambar protrusion.

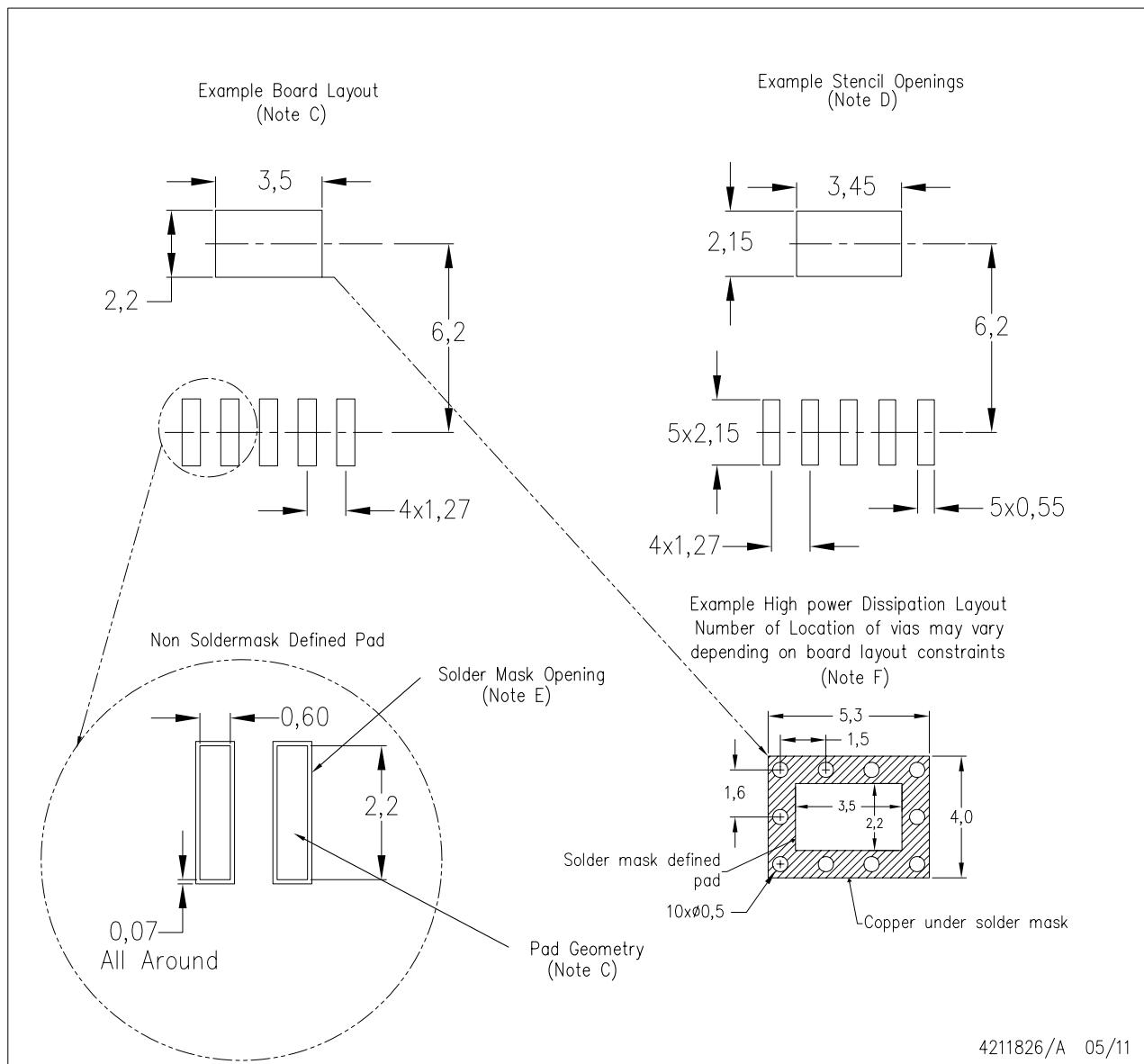
Lead width and thickness dimensions apply to solder plated leads.

- Interlead flash allow 0.008 inch max.
- Gate burr/protrusion max. 0.006 inch.
- Datums A and B are to be determined at Datum H.

LAND PATTERN DATA

DCQ (R-PDSO-G6)

PLASTIC SMALL OUTLINE



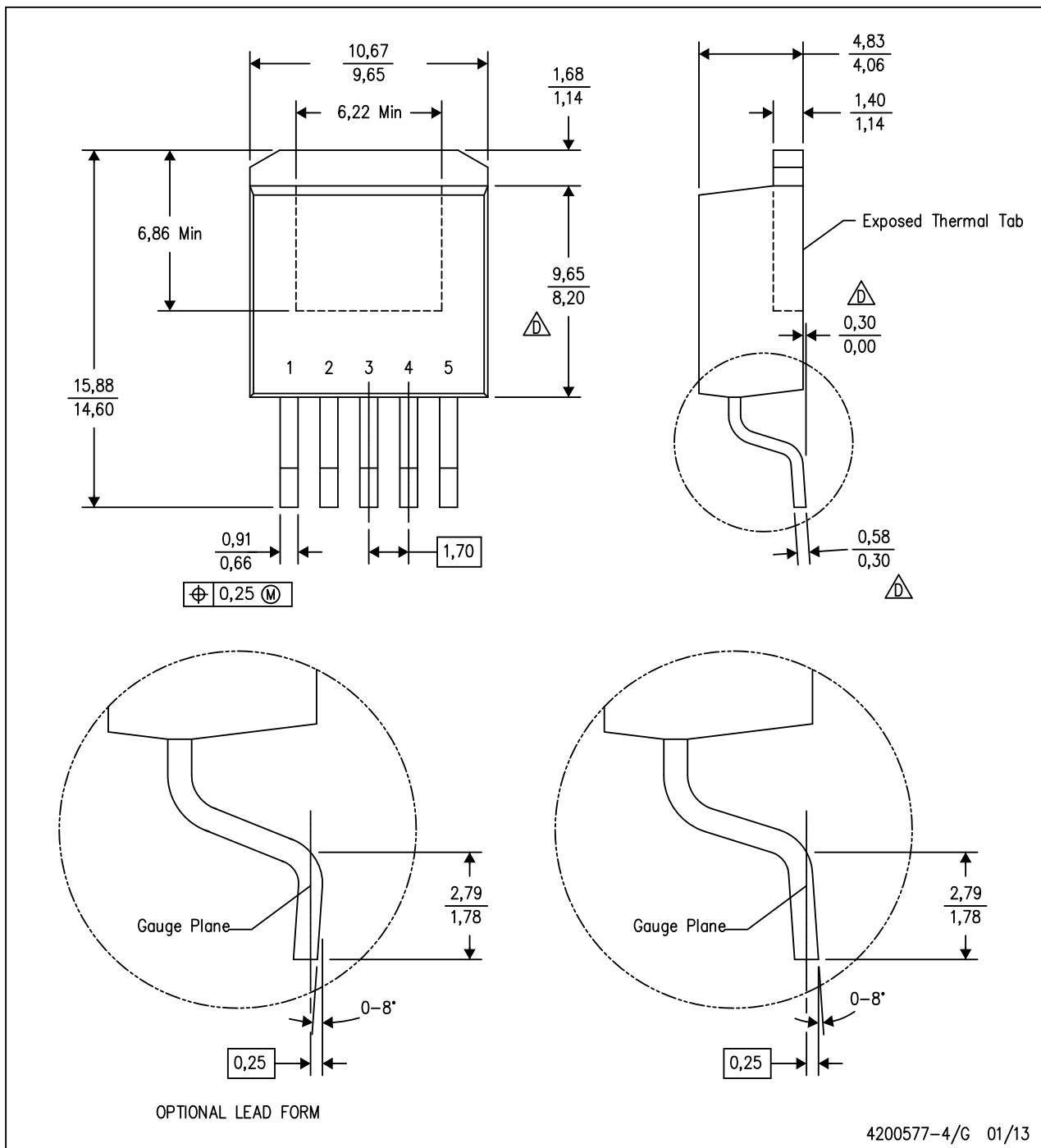
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-SM-782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. Please refer to the product data sheet for specific via and thermal dissipation requirements.

MECHANICAL DATA

KT (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE



NOTES:

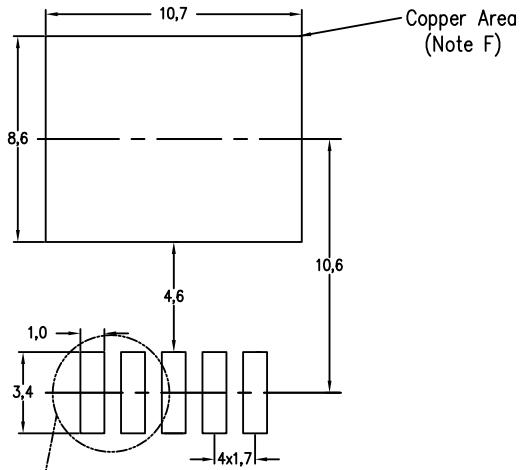
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- Δ Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

LAND PATTERN DATA

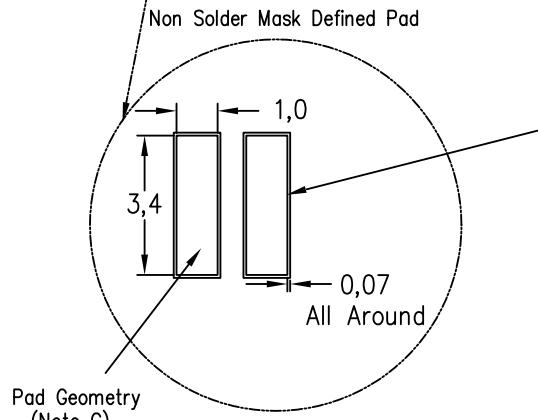
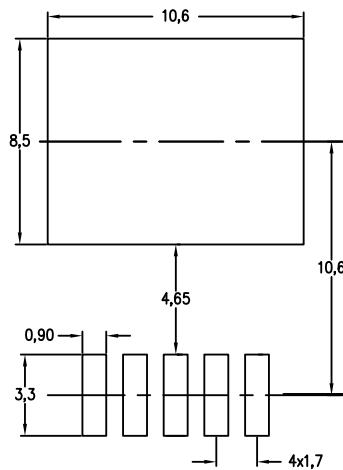
KTT (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE

Example Board Layout
(Note C)



Example Stencil Design
(Note D)



Example
Solder Mask Opening
(Note E)

4208208-3/C 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-SM-782 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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