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LM611CM/NOPB

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LM611 Operational Amplifier and Adjustable Reference

Check for Samples: LM611

FEATURES

OP AMP

- **Low Operating Current: 300 μA (op amp)**
- **Wide Supply Voltage Range: 4V to 36V**
- **Wide Common-Mode Range: V^- to $(V^+-1.8V)$**
- **Wide Differential Input Voltage: ±36V**
- **Available in Low Cost 8-pin DIP**
- **Available in Plastic Package Rated for Military Temperature Range Operation**

REFERENCE

- **Adjustable Output Voltage: 1.2V to 6.3V**
- **Tight Initial Tolerance Available: ±0.6%**
- **Wide Operating Current Range: 17 μA to 20 mA**
- **Reference Floats Above Ground**
- **Tolerant of Load Capacitance**

APPLICATIONS

- **Transducer Bridge Driver**
- **Process and Mass Flow Control Systems**
- **Power Supply Voltage Monitor**
- **Buffered Voltage References for A/D's**

DESCRIPTION

The LM611 consists of a single-supply op-amp and a programmable voltage reference in one space saving 8-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with a wide output swing op-amp makes the LM611 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of TI's Super-Block family, the LM611 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Connection Diagrams

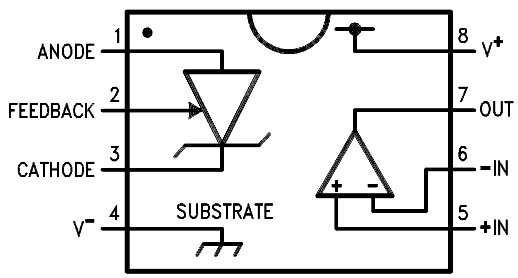


Figure 1. Hermetic Dual-In-Line Package

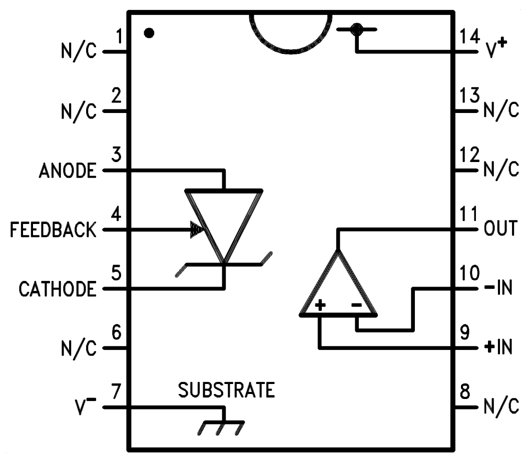


Figure 2. Plastic Surface Mount Narrow Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Voltage on Any Pins Except V_R (referred to V^- pin)	36V (Max)
See[3]	−0.3V (Min)
Current through Any Input Pin and V_R Pin	±20 mA
Differential Input Voltage	
Military and Industrial	±36V
Commercial	±32V
Storage Temperature Range	−65°C≤T_J≤+150°C
Maximum Junction Temperature	150°C
Thermal Resistance, Junction-to-Ambient[4]	
N Package	100°C/W
D Package	150°C/W
Soldering Information Soldering (10 seconds)	
N Package	260°C
D Package	220°C
ESD Tolerance[5]	±1 kV

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.
(4) Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one op amp or reference output transistor, nominal θ_{JA} is 90°C/W for the N package and 135°C/W for the D package.
(5) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Temperature Range

LM611AI, LM611I, LM611BI	−40°C≤T_J≤+85°C
LM611AM, LM611M	−55°C≤T_J≤+125°C
LM611C	0°C≤T_J≤70°C

Electrical Characteristics(1)

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical(2)	LM611AM LM611AI Limits(3)	LM611M LM611BI LM611I LM611C Limits(3)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM611C)	210 **221**	300 **320**	350 **370**	μA max μA max
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V min V min
			46 **43**	36 **36**	32 **32**	V max V max
OPERATIONAL AMPLIFIER						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ for LM611C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV max mV max
V_{OS2}	V_{OS} Over V_{CM}	$V_{CM} = 0V$ through $V_{CM} = (V^+ - 1.8V)$, $V^+ = 30V$, $V^- = 0V$	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV max mV max
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	See(3)	**15**			μV/°C max
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA max nA max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA max nA max
$\frac{I_{OS1}}{\Delta T}$	Average Offset Drift Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1800			MΩ
		Common-Mode	3800			MΩ
C_{IN}	Input Capacitance	Common-Mode	5.7			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			nV/ √Hz
I_n	Current Noise	f = 100 Hz, Input Referred	58			fA/√Hz
CMRR	Common-Mode Rejection-Ratio	$V^+ = 30V$, $0V \le V_{CM} \le (V^+ - 1.8V)$ CMRR = 20 log ($\Delta V_{CM}/\Delta V_{OS}$)	95 **90**	80 **75**	75 **70**	dB min dB min
PSRR	Power Supply Rejection-Ratio	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$, PSRR = 20 log ($\Delta V^+/\Delta V_{OS}$)	110 **100**	80 **75**	75 **70**	dB min dB min
A_V	Open Loop Voltage Gain	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$, $5V \le V_{OUT} \le 25V$	500 **50**	100 **40**	94 **40**	V/mV min
SR	Slew Rate	$V^+ = 30V$(4)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/μs
GBW	Gain Bandwidth	$C_L = 50$ pF	0.80 **0.50**			MHz
V_{O1}	Output Voltage Swing High	$R_L = 10\ k\Omega$ to GND $V^+ = 36V$ (32V for LM611C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V min V min
V_{O2}	Output Voltage Swing Low	$R_L = 10\ k\Omega$ to V^+ $V^+ = 36V$ (32V for LM611C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V max V max
I_{OUT}	Output Source Current	$V_{OUT} = 2.5V$, $V_{+IN} = 0V$, $V_{-IN} = -0.3V$	25 **15**	20 **13**	16 **13**	mA min mA min

(1) Military RETS 611AMX electrical test specification is available on request. The LM611AMJ/883 can also be procured as a Standard Military Drawing.
(2) Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.
(3) All limits are specified at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.
(4) Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and output voltage transition is sampled at 20V and 10V.

Electrical Characteristics(1) (continued)

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical(2)	LM611AM LM611AI Limits(3)	LM611M LM611BI LM611I LM611C Limits(3)	Units
I_{SINK}	Output Sink Current	$V_{OUT} = 1.6V$, $V_{+IN} = 0V$, $V_{-IN} = 0.3V$	17 **9**	14 **8**	13 **8**	mA min mA min
I_{SHORT}	Short Circuit Current	$V_{OUT} = 0V$, $V_{+IN} = 3V$, $V_{-IN} = 2V$, Source	30 **40**	50 **60**	50 **60**	mA max mA max
		$V_{OUT} = 5V$, $V_{+IN} = 2V$, $V_{-IN} = 3V$, Sink	30 **32**	60 **80**	70 **90**	mA max mA max
VOLTAGE REFERENCE						
V_R	Reference Voltage	See(5)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2.0%)	V min V max
$\frac{\Delta V_R}{\Delta T_J}$	Average Temperature Drift	See(6)	**10**	**80**	**150**	PPM/°C max
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	Hyst = (Vro′ − Vro)/ΔT_J(7)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV max mV max
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$(8)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV max mV max
R	Resistance	$\Delta V_{R(10\rightarrow0.1\ mA)}/9.9\ mA$ $\Delta V_{R(100\rightarrow17\ \mu A)}/83\ \mu A$	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω max Ω max
$\frac{\Delta V_R}{V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro = Vr)} - V_{R(Vro = 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V+}$	V_R Change with V^+ Change	$V_{R(V+ = 5V)} - V_{R(V+ = 36V)}$ (V^+ = 32V for LM611C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV max mV max
		$V_{R(V+ = 5V)} - V_{R(V+ = 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV max mV max
$\frac{\Delta V_R}{\Delta V_{ANODE}}$	V_R Change with V_{ANODE} Change	$V^+ = V^+$ max, $\Delta V_R = V_R$ (@ $V_{ANODE} = V^- = GND) - V_R$ (@ $V_{ANODE} = V^+ - 1.0V$)	0.7 **3.3**	1.5 **3.0**	1.6 **3.0**	mV max mV max
I_{FB}	FEEDBACK Bias Current	I_{FB}; $V_{ANODE} \le V_{FB} \le 5.06V$	22 **29**	35 **40**	50 **55**	nA max nA max
e_n	V_R Noise	10 Hz to 10,000 Hz, $V_{RO} = V_R$	30			μV_{RMS}

(5) V_R is the cathode-feedback voltage, nominally 1.244V.
(6) Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/(V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is ensured by design and sample testing.
(7) Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.
(8) Low contact resistance is required for accurate measurement.

Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

Reference Voltage vs Temp on 5 Representative Units

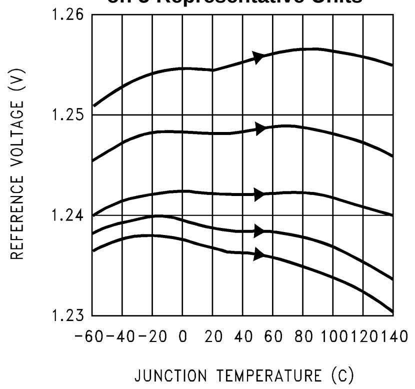


Figure 3.

Reference Voltage Drift

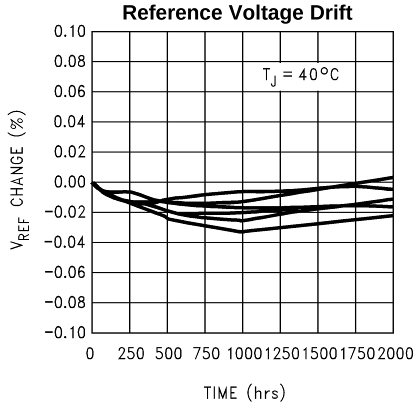


Figure 4.

Accelerated Reference Voltage Drift vs Time

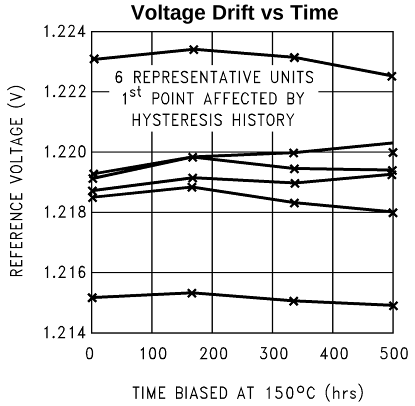


Figure 5.

Reference Voltage vs Current and Temperature

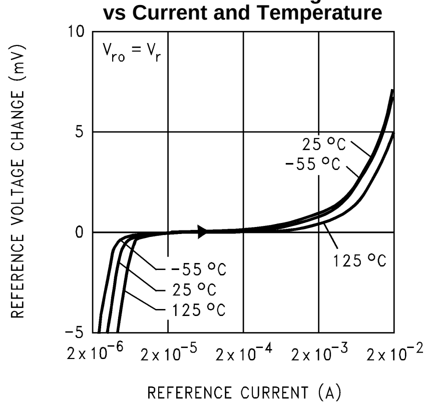


Figure 6.

Reference Voltage vs Current and Temperature

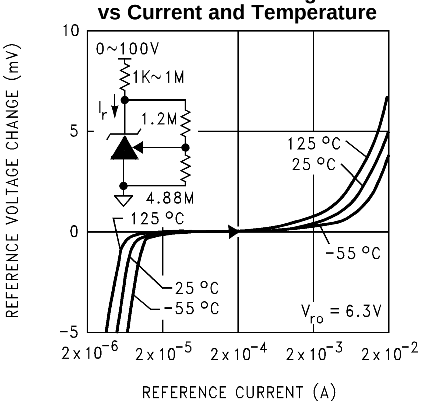


Figure 7.

Reference Voltage vs Reference Current

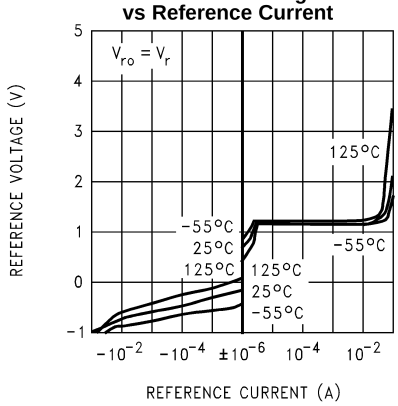


Figure 8.

Typical Performance Characteristics (Reference) (continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

Reference Voltage vs Reference Current

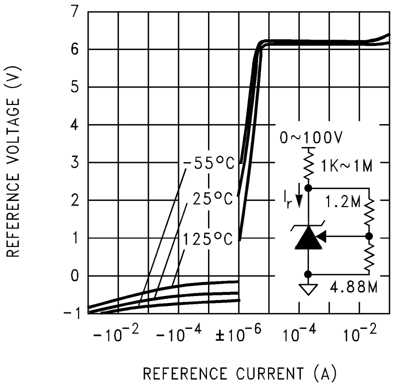


Figure 9.

Reference AC Stability Range

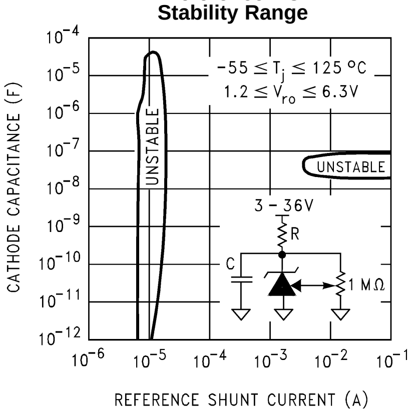


Figure 10.

Feedback Current vs Feedback-to-Anode Voltage

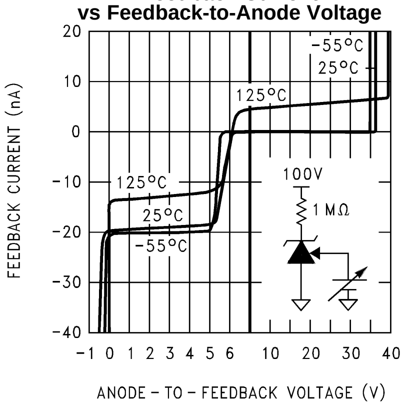


Figure 11.

Feedback Current vs Feedback-to-Anode Voltage

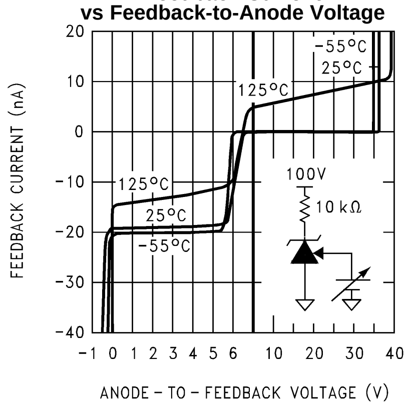


Figure 12.

Reference Noise Voltage vs Frequency

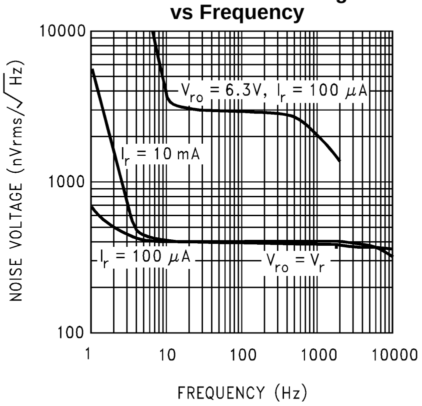


Figure 13.

Reference Small-Signal Resistance vs Frequency

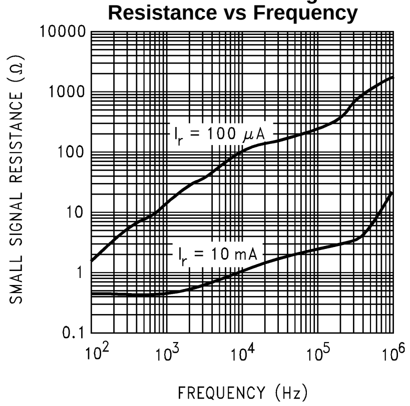


Figure 14.

Typical Performance Characteristics (Reference) (continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

Reference Power-Up Time

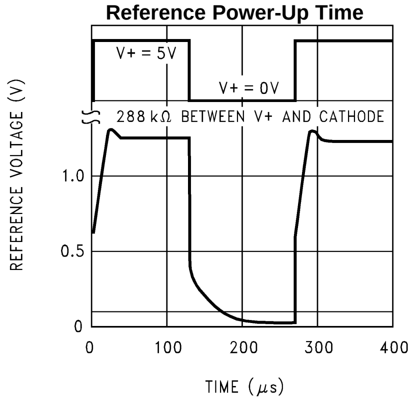


Figure 15.

Reference Voltage with Feedback Voltage Step

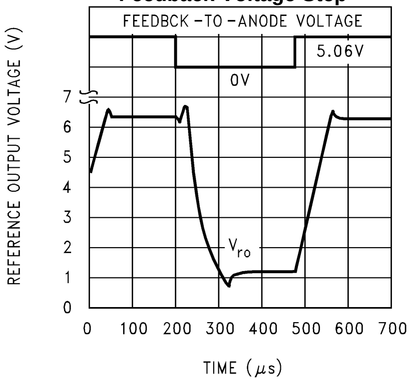


Figure 16.

Reference Voltage with 100~12 μA Current Step

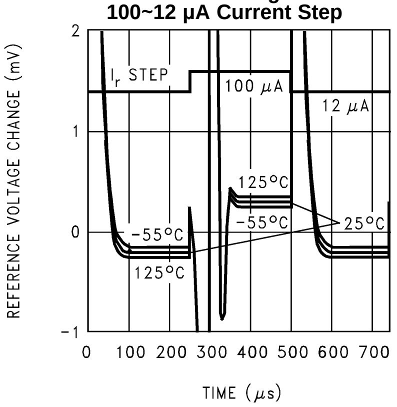


Figure 17.

Reference Step Response for 100 μA ~ 10 mA Current Step

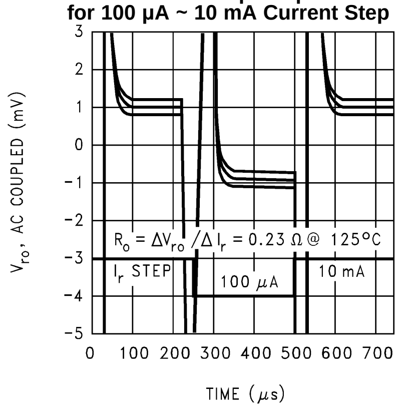


Figure 18.

Reference Voltage Change with Supply Voltage Step

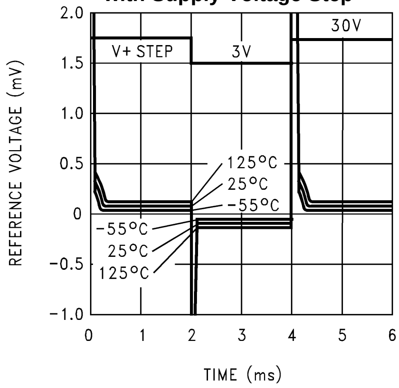


Figure 19.

Typical Performance Characteristics (Op Amps)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

Input Common-Mode Voltage Range vsTemperature

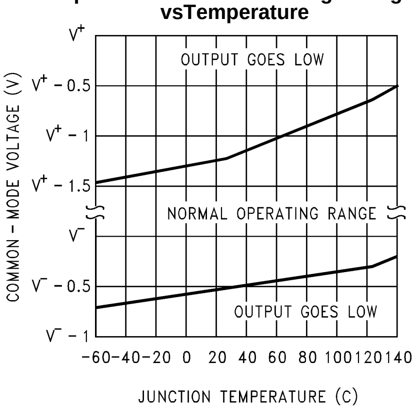


Figure 20.

V_{OS} vs Junction Temperature

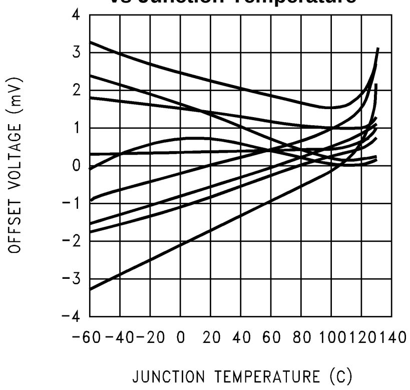


Figure 21.

Input Bias Current vs Common-Mode Voltage

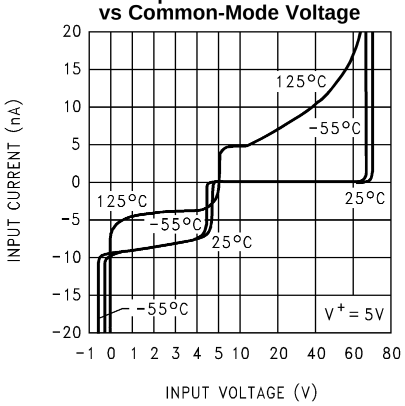


Figure 22.

Reference Change vs Common-Mode Voltage

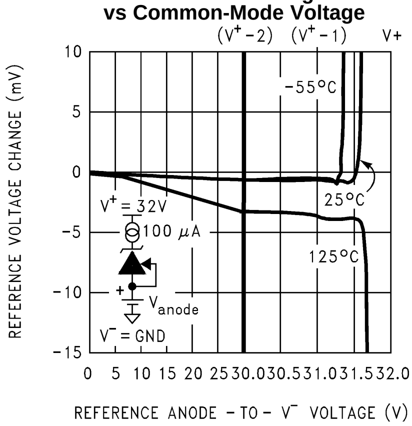


Figure 23.

Large-Signal Step Response

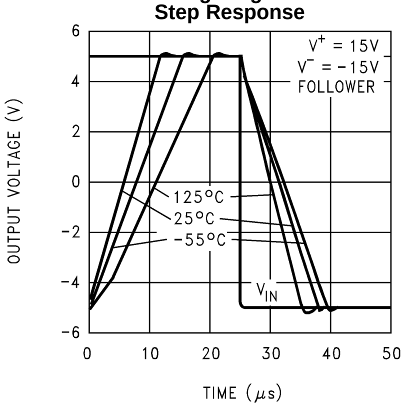


Figure 24.

Output Voltage Swing vs Temp. and Current

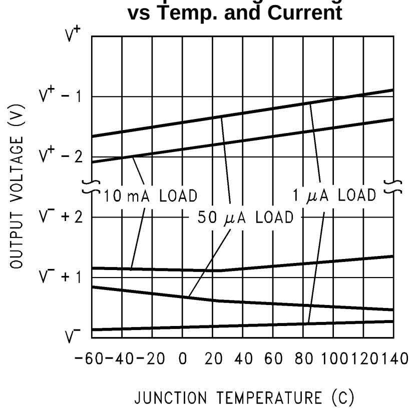


Figure 25.

Typical Performance Characteristics (Op Amps) (continued)

V^+ = 5V, V^- = GND = 0V, V_{CM} = $V^+/2$, V_{OUT} = $V^+/2$, T_J = 25°C, unless otherwise noted

Output Source Current vs Output Voltage and Temp.

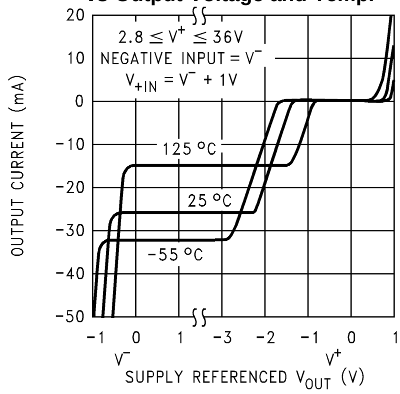


Figure 26.

Output Sink Current vs Output Voltage

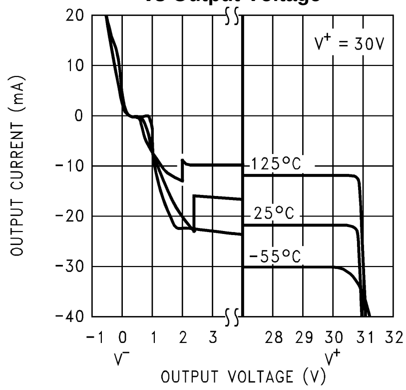


Figure 27.

Output Swing, Large Signal

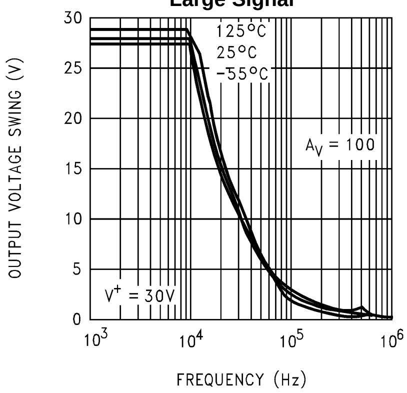


Figure 28.

Output Impedance vs Frequency and Gain

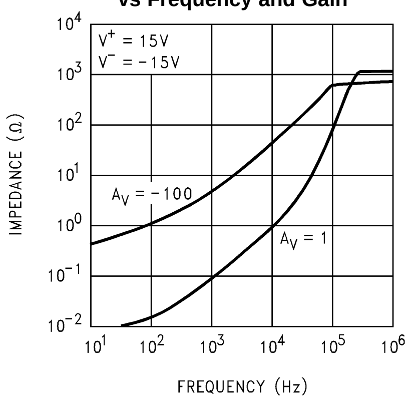


Figure 29.

Small Signal Pulse Response vs Temp.

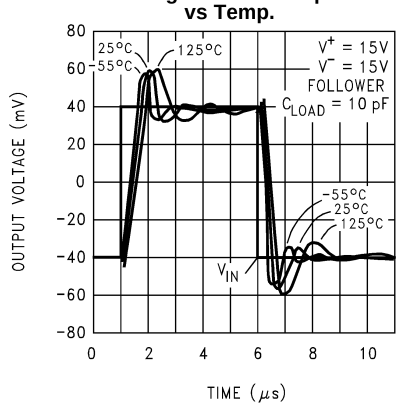


Figure 30.

Small-Signal Pulse Response vs Load

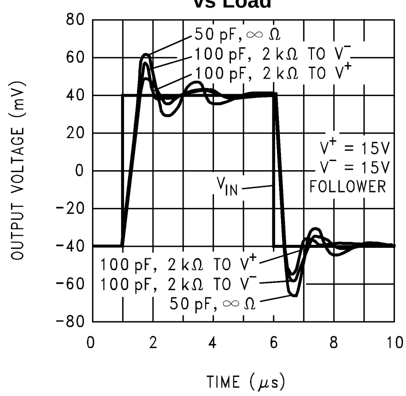


Figure 31.

Typical Performance Characteristics (Op Amps) (continued)

V^+ = 5V, V^- = GND = 0V, V_{CM} = V^+/2, V_{OUT} = V^+/2, T_J = 25°C, unless otherwise noted

Op Amp Voltage Noise vs Frequency

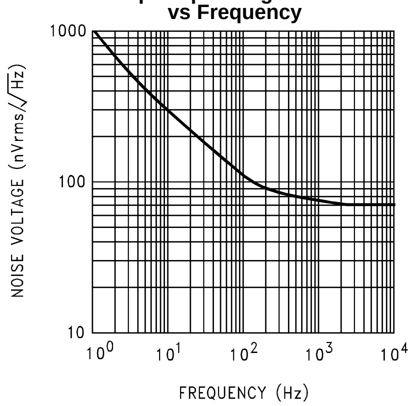


Figure 32.

Op Amp Current Noise vs Frequency

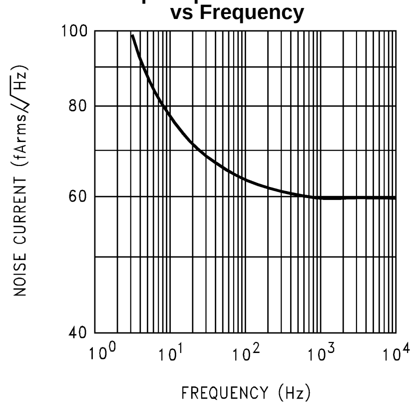


Figure 33.

Small-Signal Voltage Gain vs Frequency and Temperature

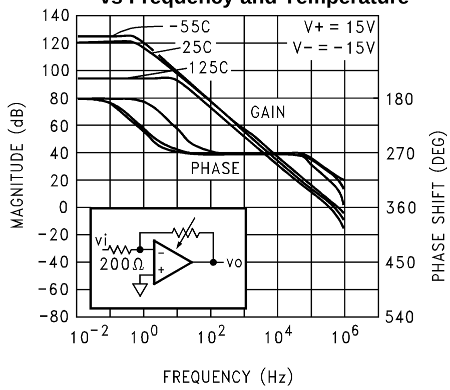


Figure 34.

Small-Signal Voltage Gain vs Frequency and Load

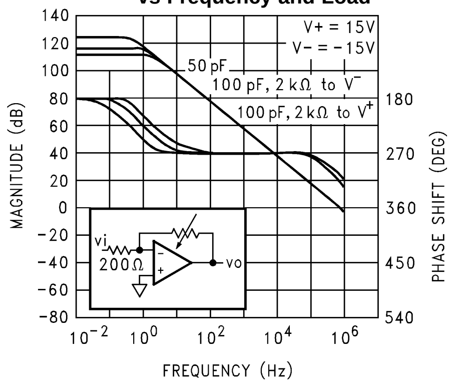


Figure 35.

Follower Small-Signal Frequency Response

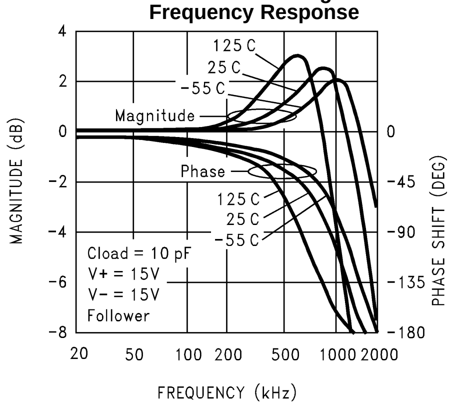


Figure 36.

Common-Mode Input Voltage Rejection Ratio

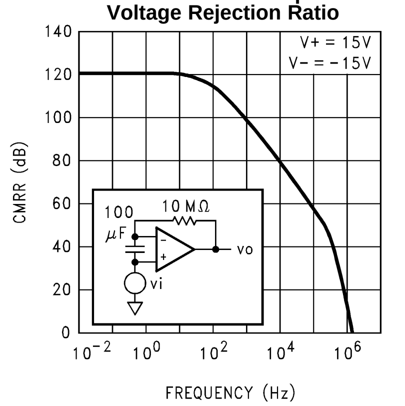


Figure 37.

Typical Performance Characteristics (Op Amps) (continued)

V^+ = 5V, V^- = GND = 0V, V_{CM} = $V^+/2$, V_{OUT} = $V^+/2$, T_J = 25°C, unless otherwise noted

Power Supply Current vs Power Supply Voltage

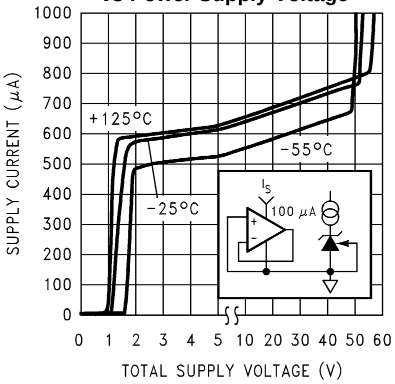


Figure 38.

Positive Power Supply Voltage Rejection Ratio

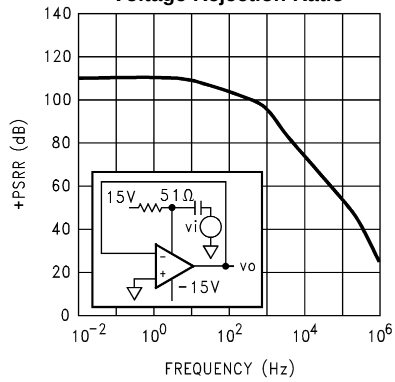


Figure 39.

Negative Power Supply Voltage Rejection Ratio

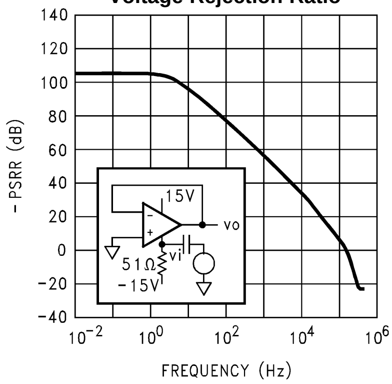


Figure 40.

Slew Rate vs Temperature

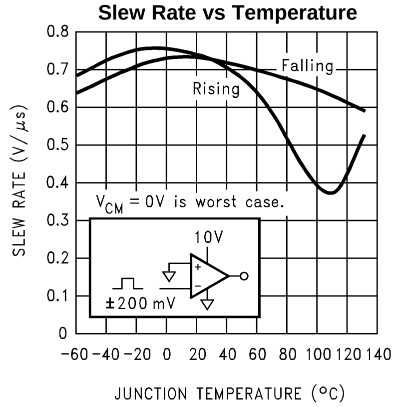


Figure 41.

Input Offset Current vs Junction Temperature

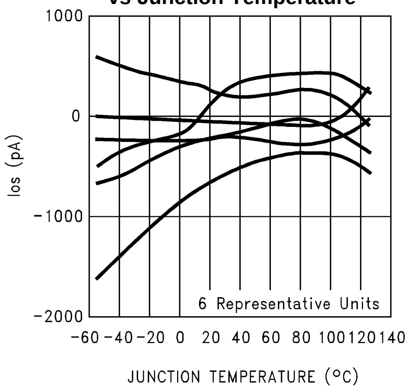


Figure 42.

Input Bias Current vs Junction Temperature

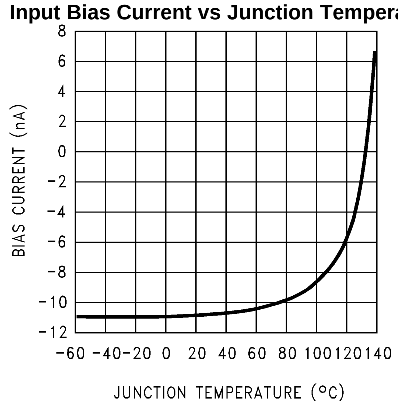


Figure 43.

Typical Performance Distributions

Average V_{OS} Drift
Military Temperature Range

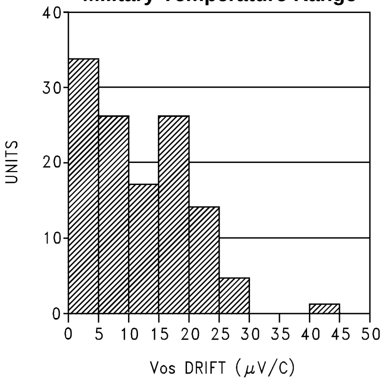


Figure 44.

Average V_{OS} Drift
Industrial Temperature Range

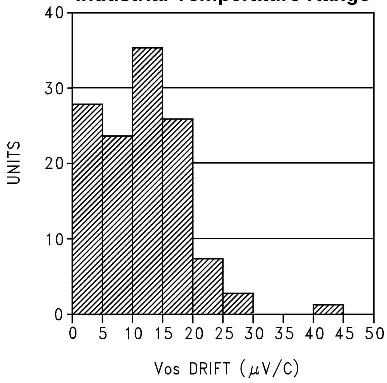


Figure 45.

Average V_{OS} Drift
Commercial Temperature Range

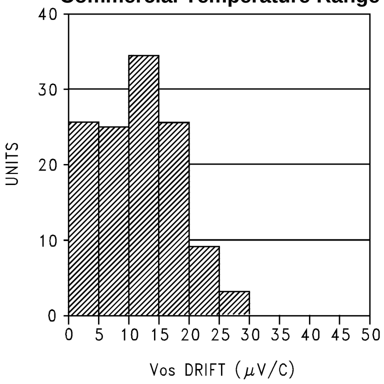


Figure 46.

Average I_{OS} Drift
Military Temperature Range

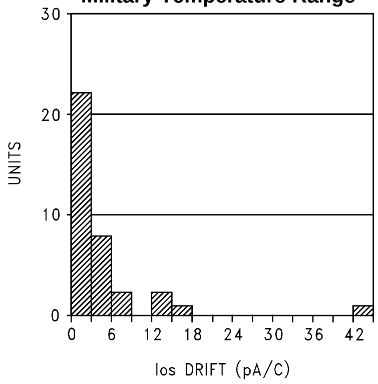


Figure 47.

Average I_{OS} Drift
Industrial Temperature Range

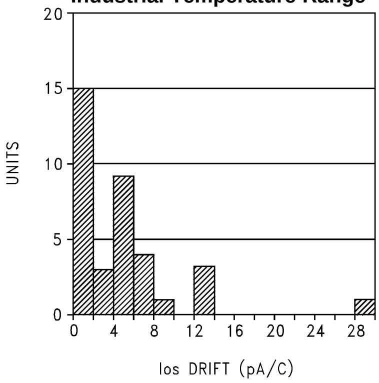


Figure 48.

Average I_{OS} Drift
Commercial Temperature Range

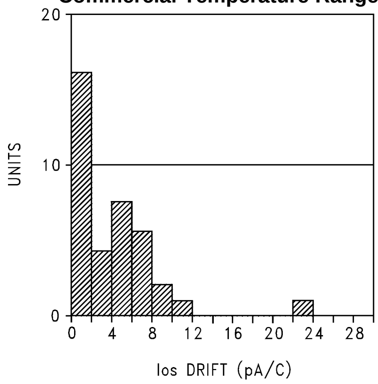


Figure 49.

Typical Performance Distributions (continued)

Voltage Reference Broad-Band Noise Distribution

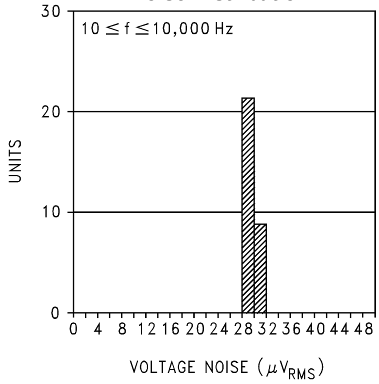


Figure 50.

Op Amp Voltage Noise Distribution

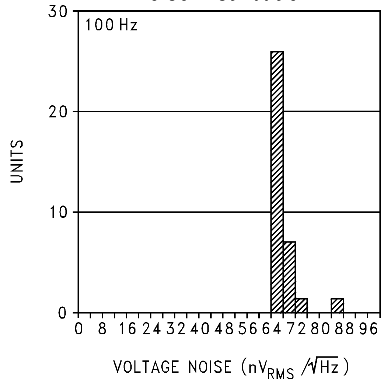


Figure 51.

Op Amp Current Noise Distribution

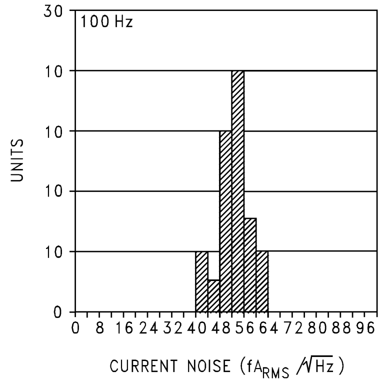


Figure 52.

APPLICATION INFORMATION

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The applied voltage to the cathode may range from a diode drop below V⁻ to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with V+ = 3V is allowed.

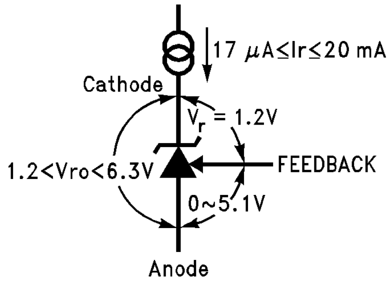


Figure 53. Voltages Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

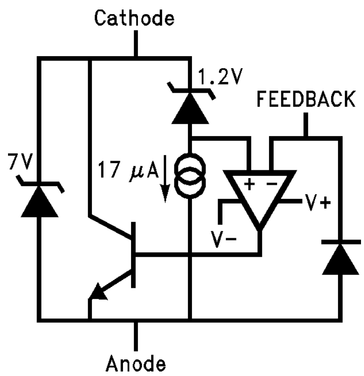


Figure 54. Reference Equivalent Circuit

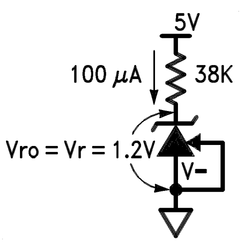


Figure 55. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range curve for capacitance values—from 20 µA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for V_{ro} = 5V. Connecting a resistor across the constant V_r generates a current I=R1/V_r flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with R2=3.76/I. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—I≥32 µA for the military grade over the military temperature range (I≥5.5 µA for a 1% untrimmed error for a commercial part.)

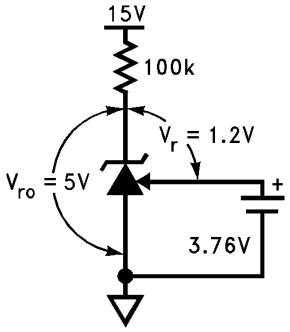
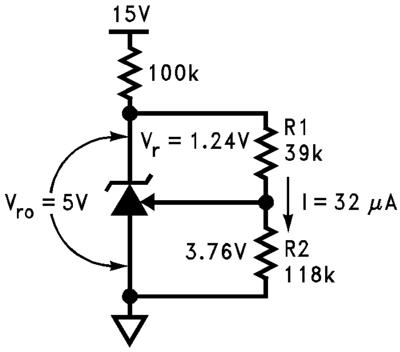


Figure 56. Thevenin Equivalent of Reference with 5V Output



R1 = Vr/I = 1.24/32µ = 39k

R2 = R1 {(Vro/Vr) − 1} = 39k {(5/1.24) − 1)} = 118k

Figure 57. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.

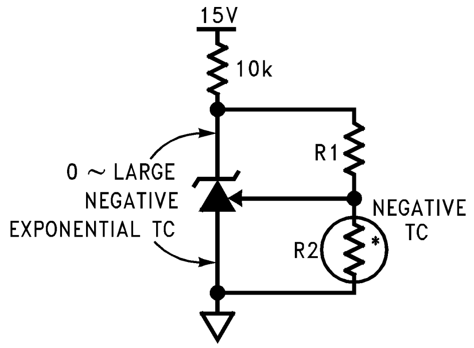


Figure 58. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

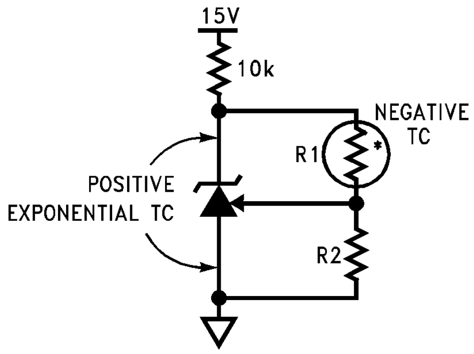


Figure 59. Output Voltage has Positive TC if R1 has Negative TC

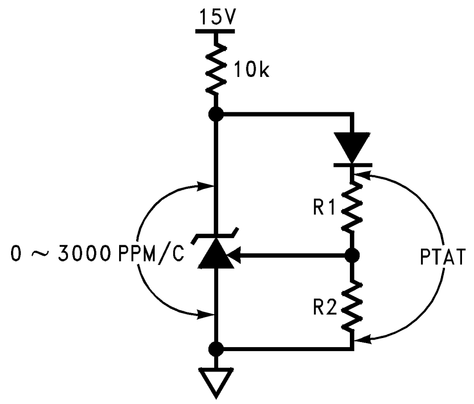
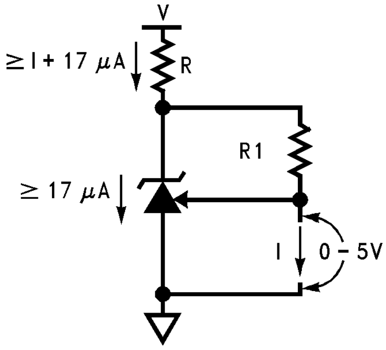


Figure 60. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



I = Vr/R1 = 1.24/R1

Figure 61. Current Source is Programmed by R1

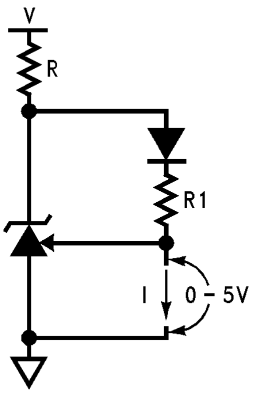


Figure 62. Proportional-to-Absolute-Temperature Current Source

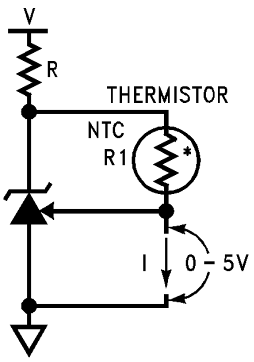


Figure 63. Negative −TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIER

The amp or the reference may be biased in any way with no effect on the other, except when a substrate diode conducts (see [1] under Electrical Characteristics). The amp may have inputs outside the common-mode range, may be operated as a comparator, or have all terminals floating with no effect on the reference (tying inverting input to output and non-inverting input to V^- on unused amp is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

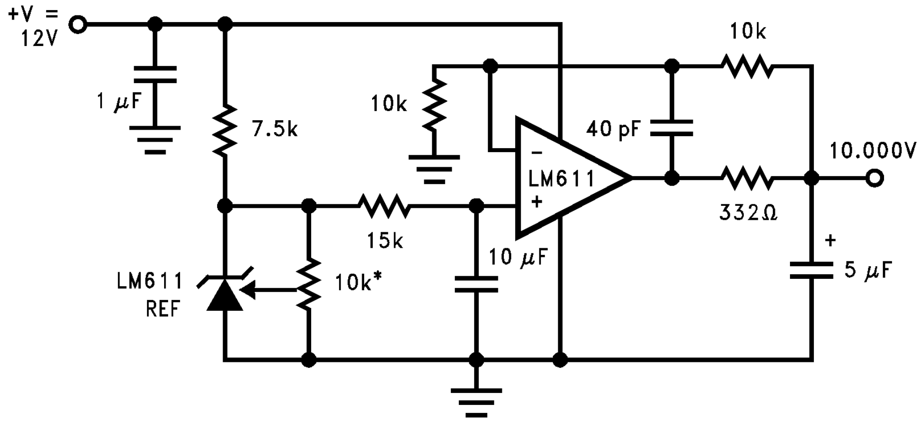
The op amp, like the LM124 series, has a flexible and relatively wide-swing output stage. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1. Output Swing: Unloaded, the 42 µA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 µA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.
2. Cross-over Distortion: The LM611 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the Typical Performance Charactersitics curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3. Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Op Amp Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications



*10k must be low t.c. trim pot.

Figure 64. Ultra Low Noise 10.00V Reference. Total Output Noise is Typically 14 μV_{RMS}. Adjust the 10k pot for 10.000V.

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

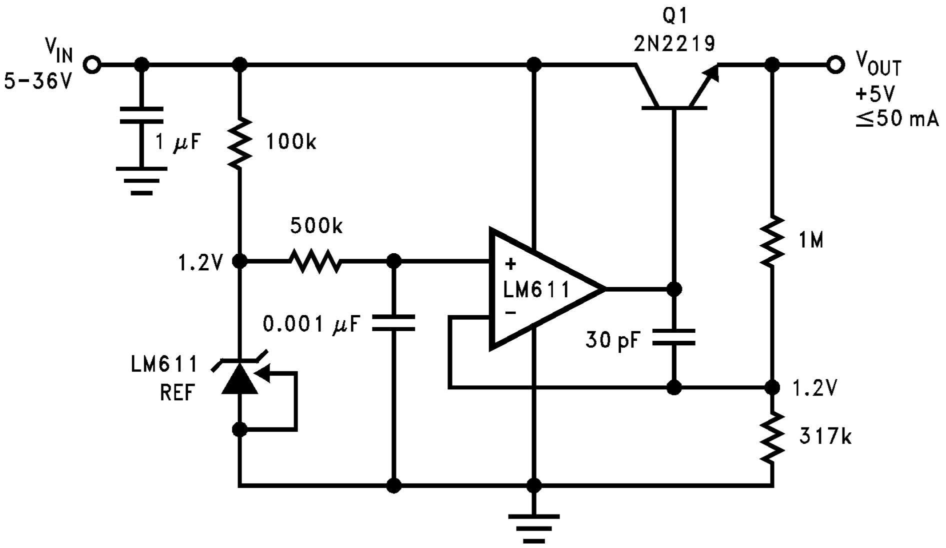
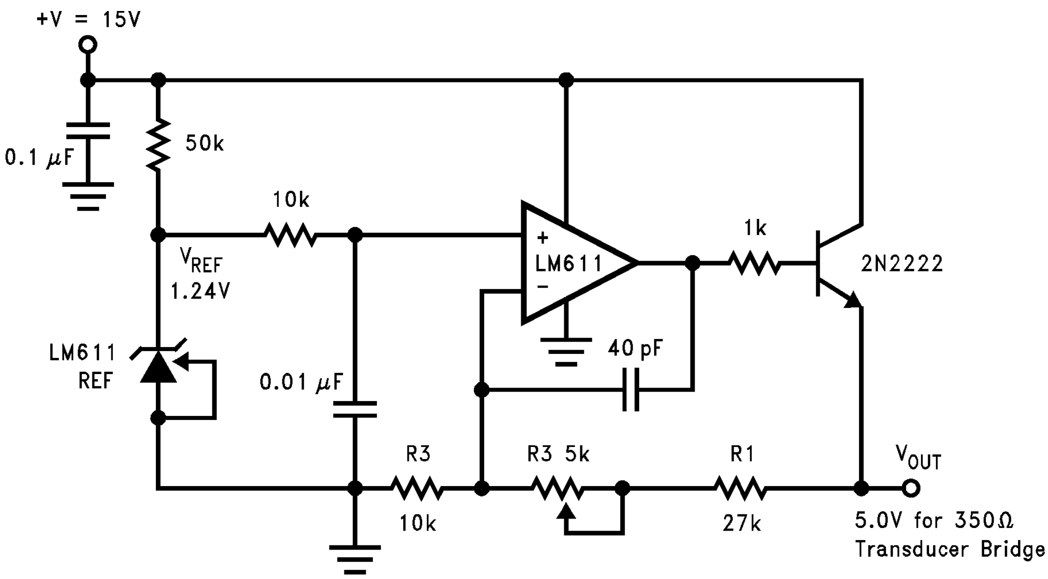


Figure 65. Simple Low Quiescent Drain Voltage Regulator. Total Supply Current is approximately 320 µA when V_{IN} = 5V, and output has no load.



V_{OUT} = (R1/R2 + 1) V_{REF}.
R1, R2 should be 1% metal film.
R3 should be low t.c. trim pot.

Figure 66. Slow Rise-Time Upon Power-Up, Adjustable Transducer Bridge Driver. Rise-time is approximately 0.5 ms.

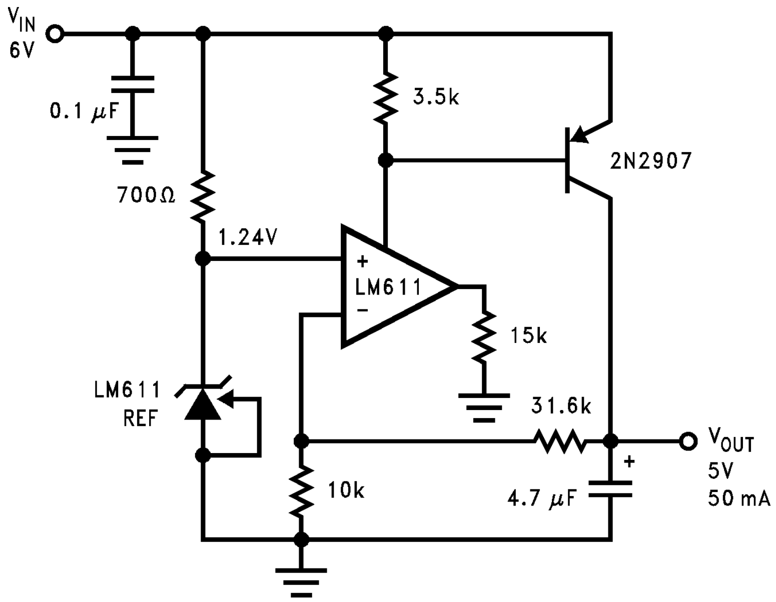


Figure 67. Low Drop-Out Voltage Regulator Circuit. Drop out voltage is typically 0.2V.

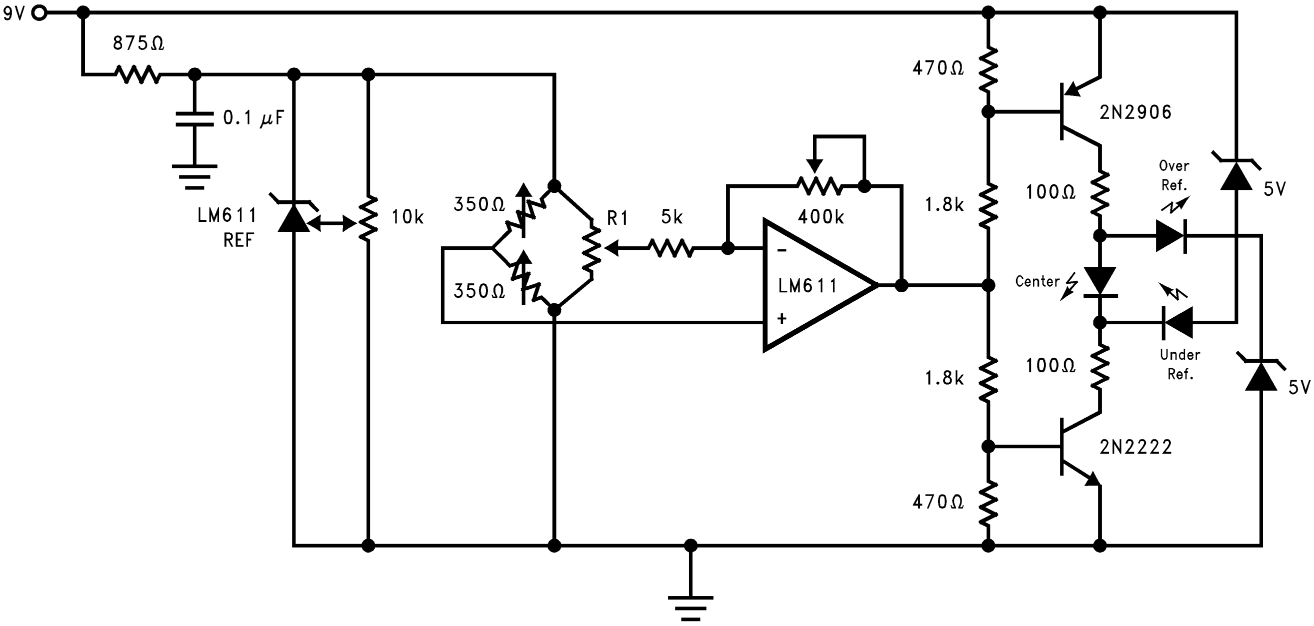


Figure 68. Nulling Bridge Detection System. Adjust sensitivity via 400 kΩ pot. Null offset with R1, and bridge drive with the 10k pot.

Simplified Schematic Diagrams

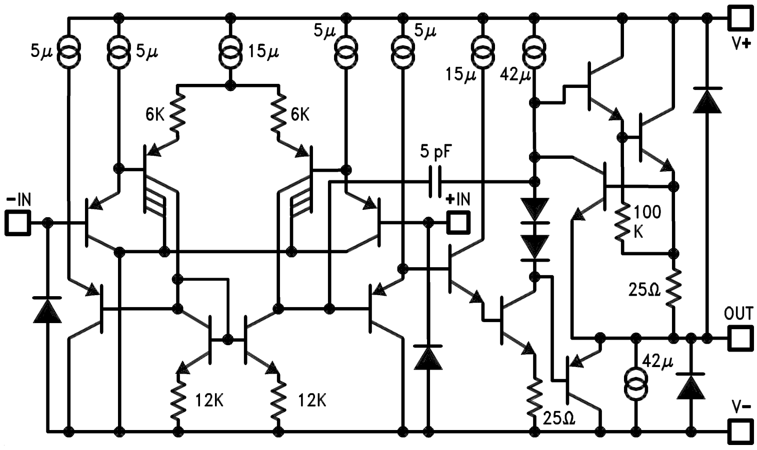


Figure 69. Op Amp

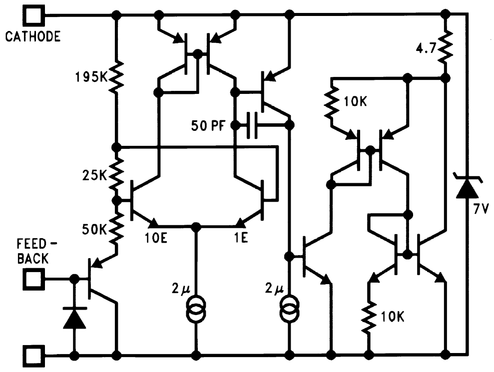


Figure 70. Reference

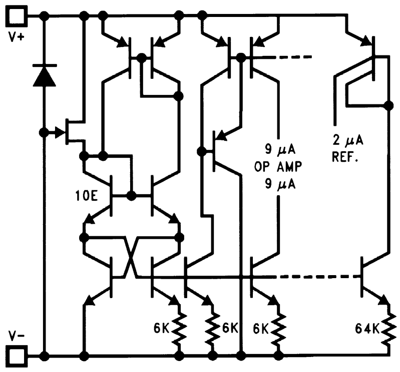


Figure 71. Bias

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM611CM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM611CM	Samples
LM611CMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM611CM	Samples
LM611IM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM611IM	Samples
LM611IMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM611IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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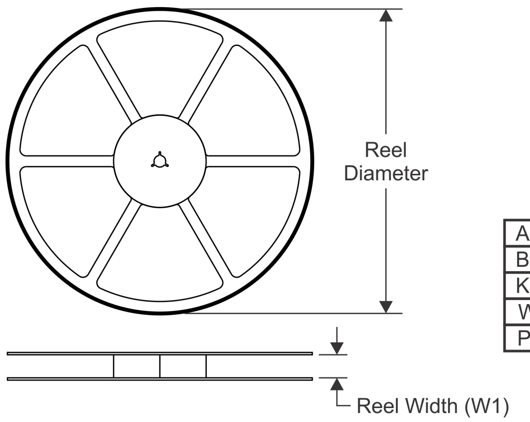
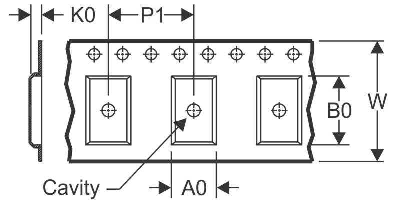
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

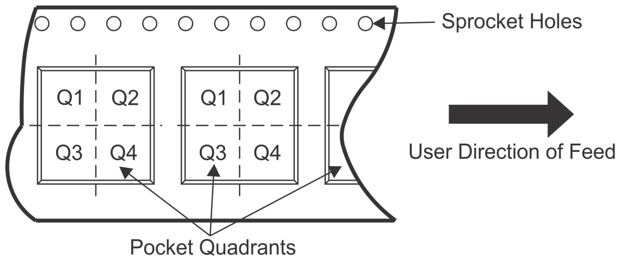


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

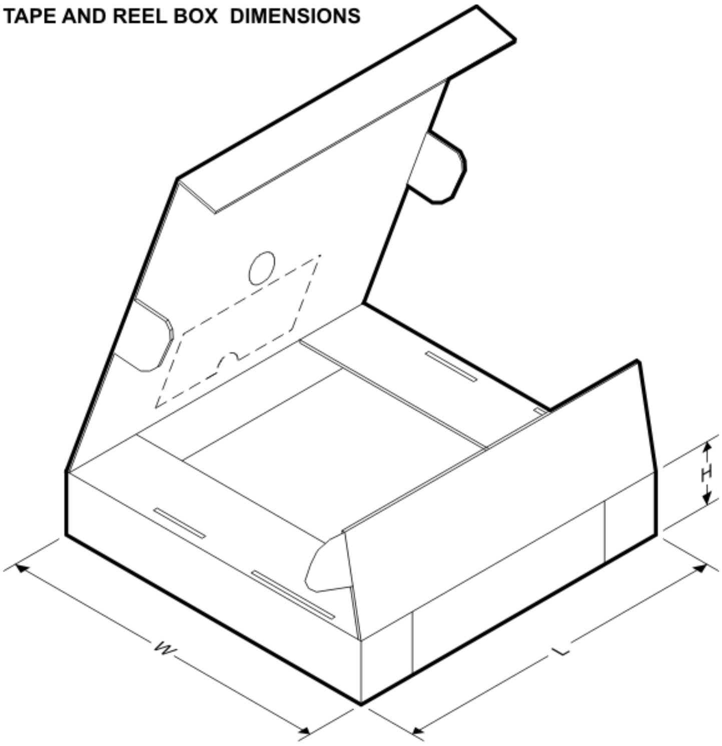
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM611CMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM611IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

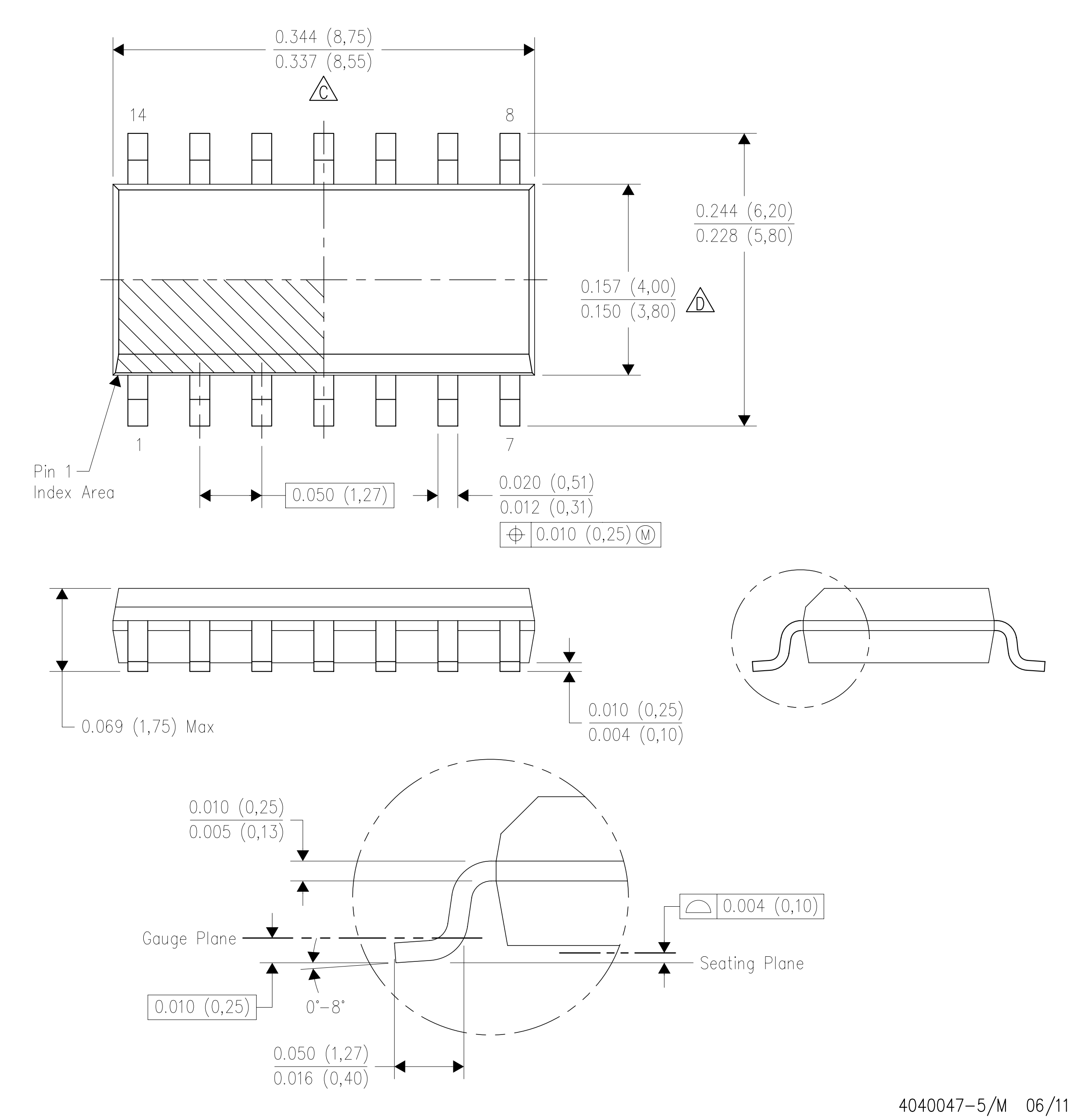
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM611CMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM611IMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

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