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SN75123N

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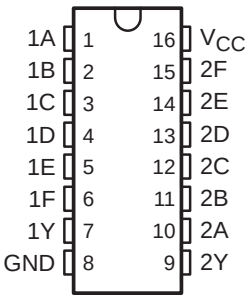
SN75123
DUAL LINE DRIVER

SLLS086C – SEPTEMBER 1973 – REVISED APRIL 1998

- **Meets or Exceeds the Requirements of IBM™ System 360 Input/Output Interface Specification**
- **Operate From Single 5-V Supply**
- **TTL Compatible**
- **3.11-V Output at I_{OH} = –59.3 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **Designed for Use With Triple Line Receiver SN75124**
- **Designed to Be Interchangeable With N8T13 and N8T23**

D OR N PACKAGE
(TOP VIEW)



THE SN751730 IS RECOMMENDED FOR NEW IBM 360/370 INTERFACE DESIGNS.

description

The SN75123 is a dual line driver specifically designed to meet the input/output interface specifications for IBM System 360. It also is compatible with standard-TTL logic and supply-voltage levels.

The SN75123 low-impedance emitter-follower outputs drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All the inputs are in conventional TTL configuration, and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

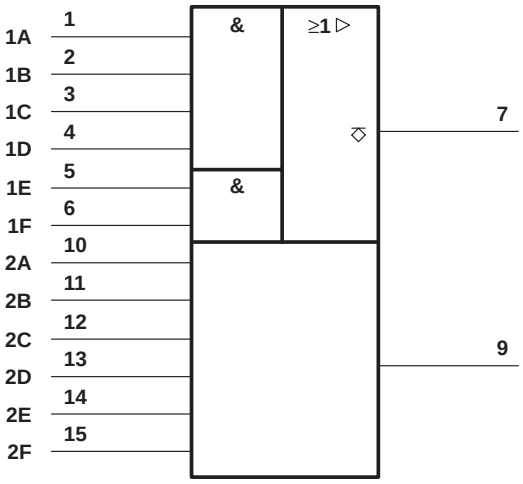
The SN75123 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

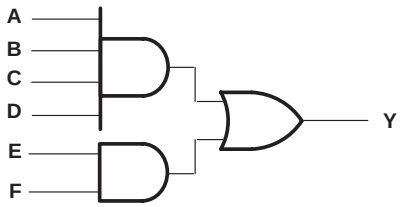
H = high level, L = low level, X = irrelevant

logic symbol†

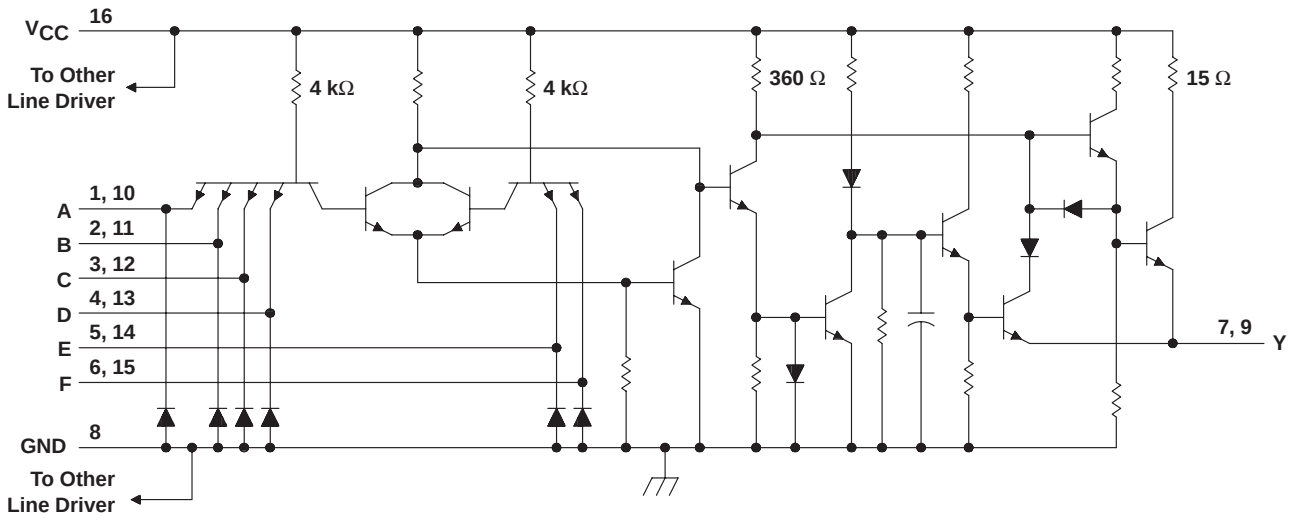


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Output voltage, V_O . . . . . 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): D package . . . . . 950 mW
N package . . . . 1150 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–100	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = –12 mA			–1.5	V
$V_{I(BR)}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5		V
V_{OH}	High-level output voltage	V_{CC} = 5 V, V_{IH} = 2 V, I_{OH} = –59.3 mA, See Note 3	T_A = 25°C		3.11		V
			T_A = 0°C to 70°C		2.9		
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OL} = –240 µA,	See Note 3		0.15	V
I_{OH}	High-level output current	V_{CC} = 5 V, V_{IH} = 4.5 V, V_{OH} = 2 V, T_A = 25°C, See Note 3			–100	–250	mA
$I_{O(off)}$	Off-state output current	V_{CC} = 0,	V_O = 3 V			40	µA
I_{IH}	High-level input current	V_I = 4.5 V				40	µA
I_{IL}	Low-level input current	V_I = 0.4 V			–0.1	–1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = 5 V,	T_A = 25°C			–30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	Outputs open		28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	Outputs open		60	mA

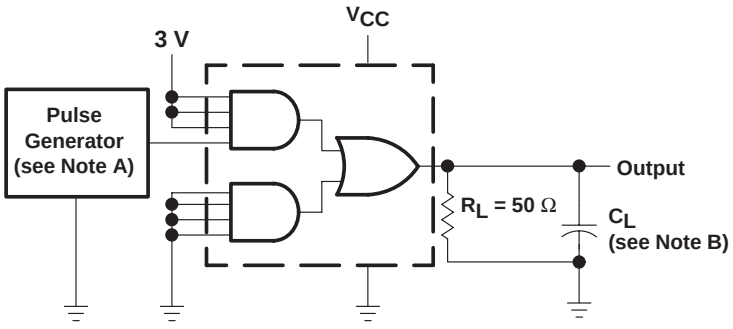
† Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

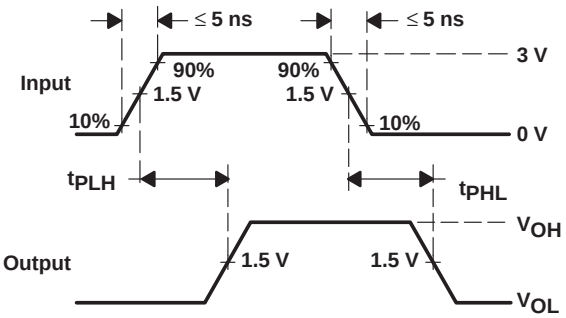
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 50 Ω,	C_L = 15 pF,	See Figure 1		12	20	ns
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 50 Ω,	C_L = 15 pF,	See Figure 1		12	20	ns
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 50 Ω,	C_L = 100 pF,	See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 50 Ω,	C_L = 100 pF,	See Figure 1		15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 200 ns, duty cycle = 50%.
B. C_L Includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

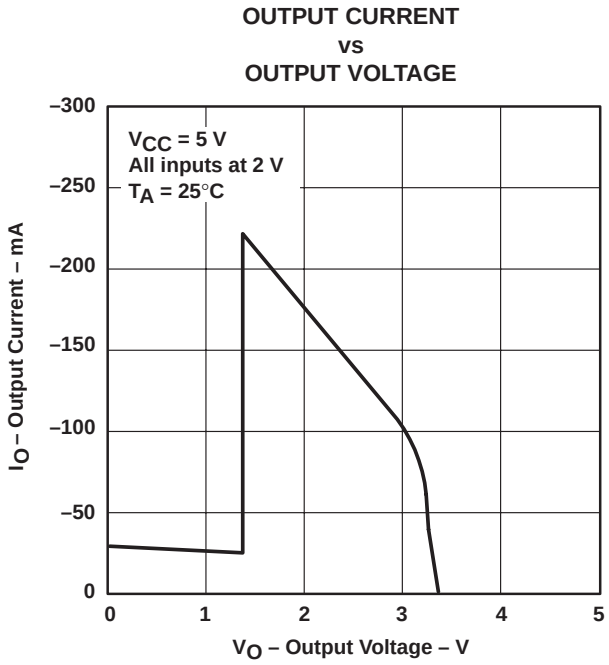


Figure 2

APPLICATION INFORMATION

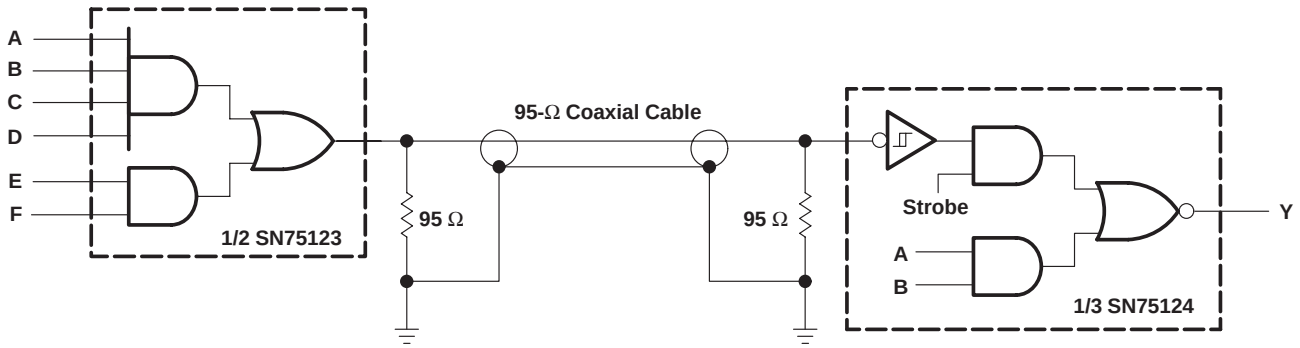


Figure 3. Unbalanced Line Communication Using SN75123 and SN75124

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75123D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN75123DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN75123N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75123N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

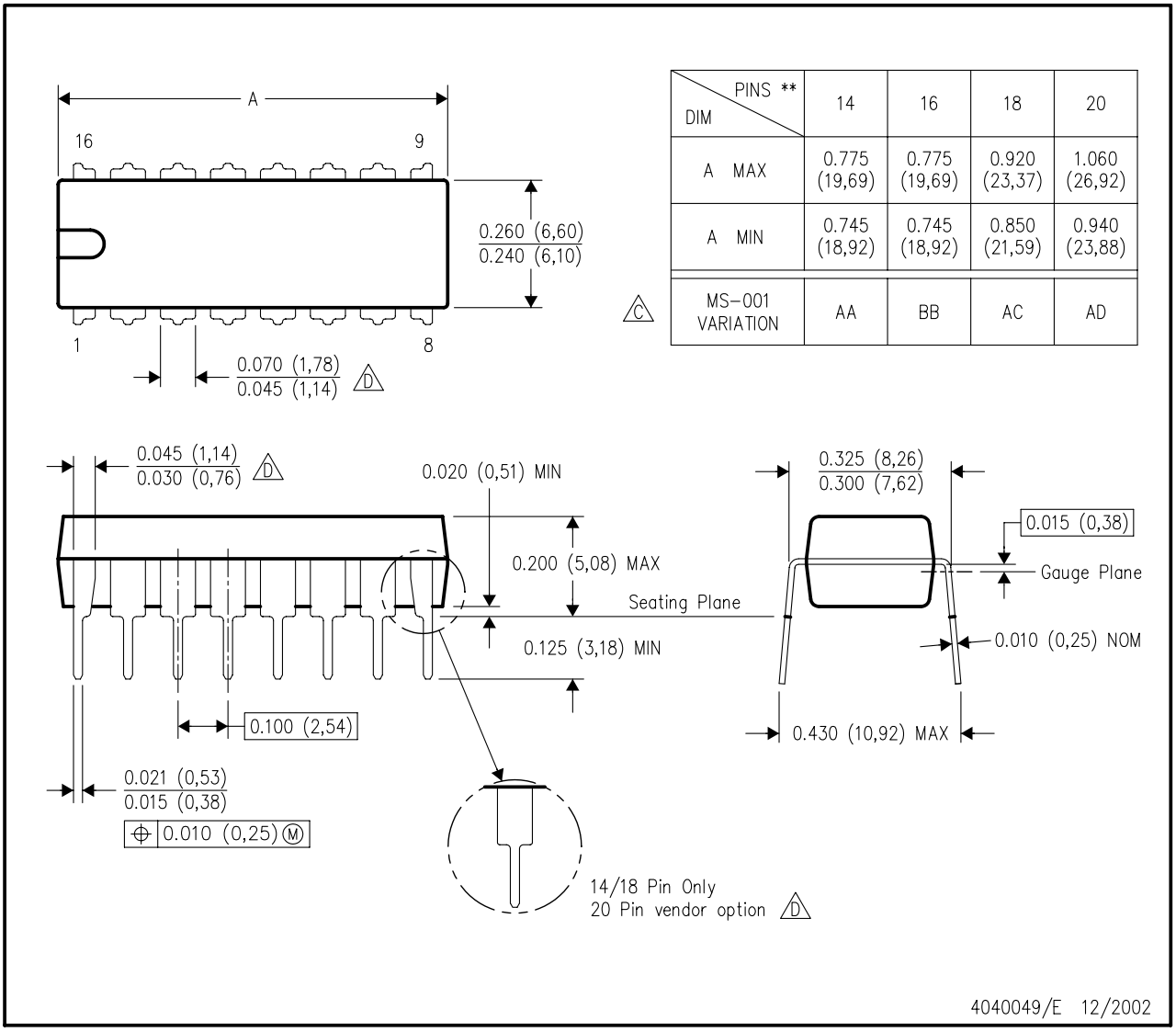
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



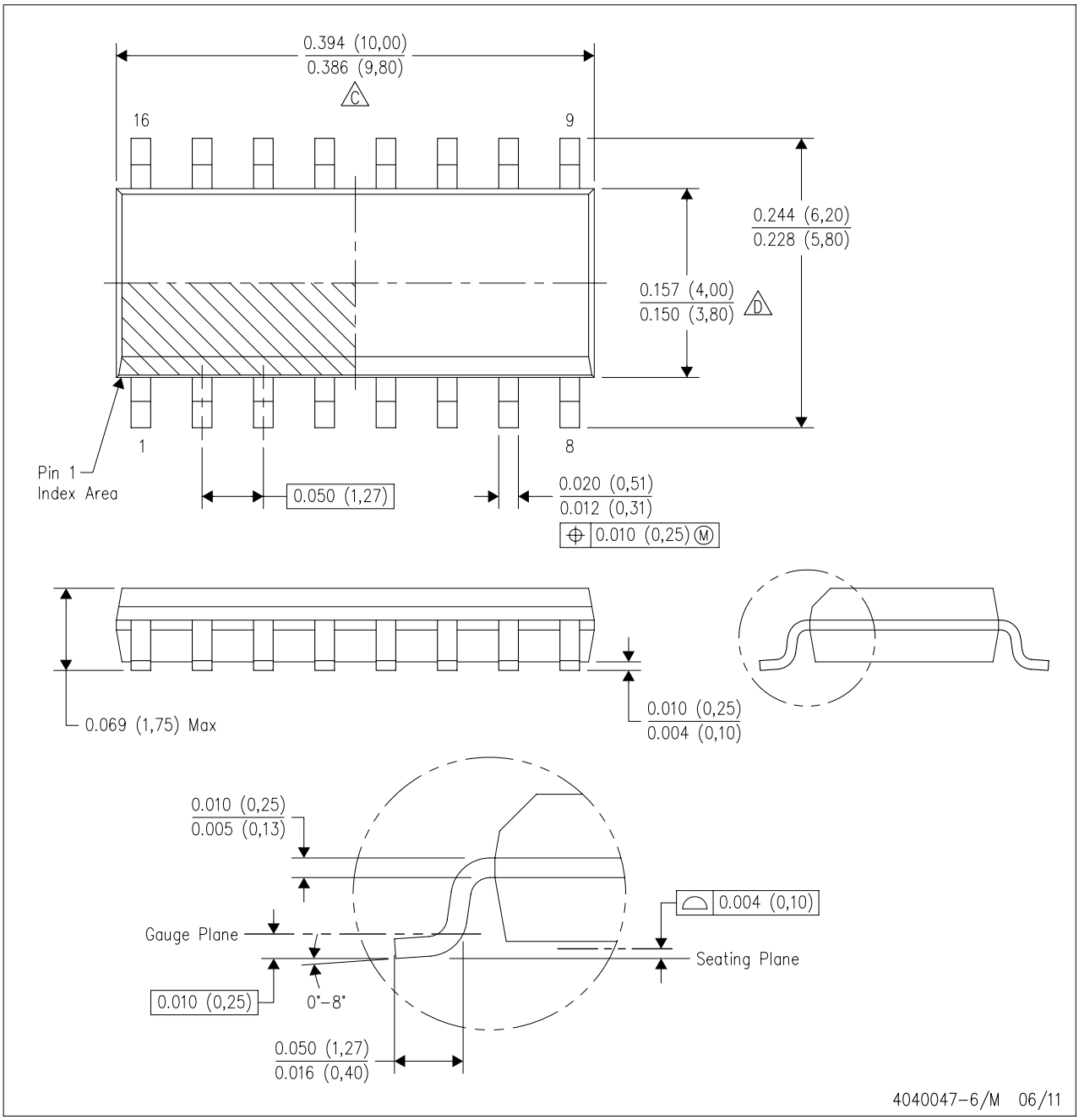
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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