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18-Line SCSI Terminator (Reverse Disconnect)

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI and FAST-20 Standards
- 2pF Channel Capacitance During Disconnect
- 50mA Supply Current in Disconnect Mode
- 110Ω Termination
- SCSI Hot Plugging Compliant, 10nA Typical
- +400mA Sinking Current for Active Negation
- -650mA Sourcing Current for Termination
- Trimmed Impedance to 5%
- Thermal Shutdown
- Current Limit

DESCRIPTION

The UCC5617 provides 18 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends and Fast-20 (Ultra) requires active termination at both ends of the cable.

Pin for pin compatible with the UC5609, the UCC5617 is ideal for high performance 5V SCSI systems, $TRMPWR$ 4.0-5.25V. During disconnect the supply current is only 50μA typical, which makes the IC attractive for lower powered systems.

The UCC5617 is designed with a low channel capacitance of 2pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

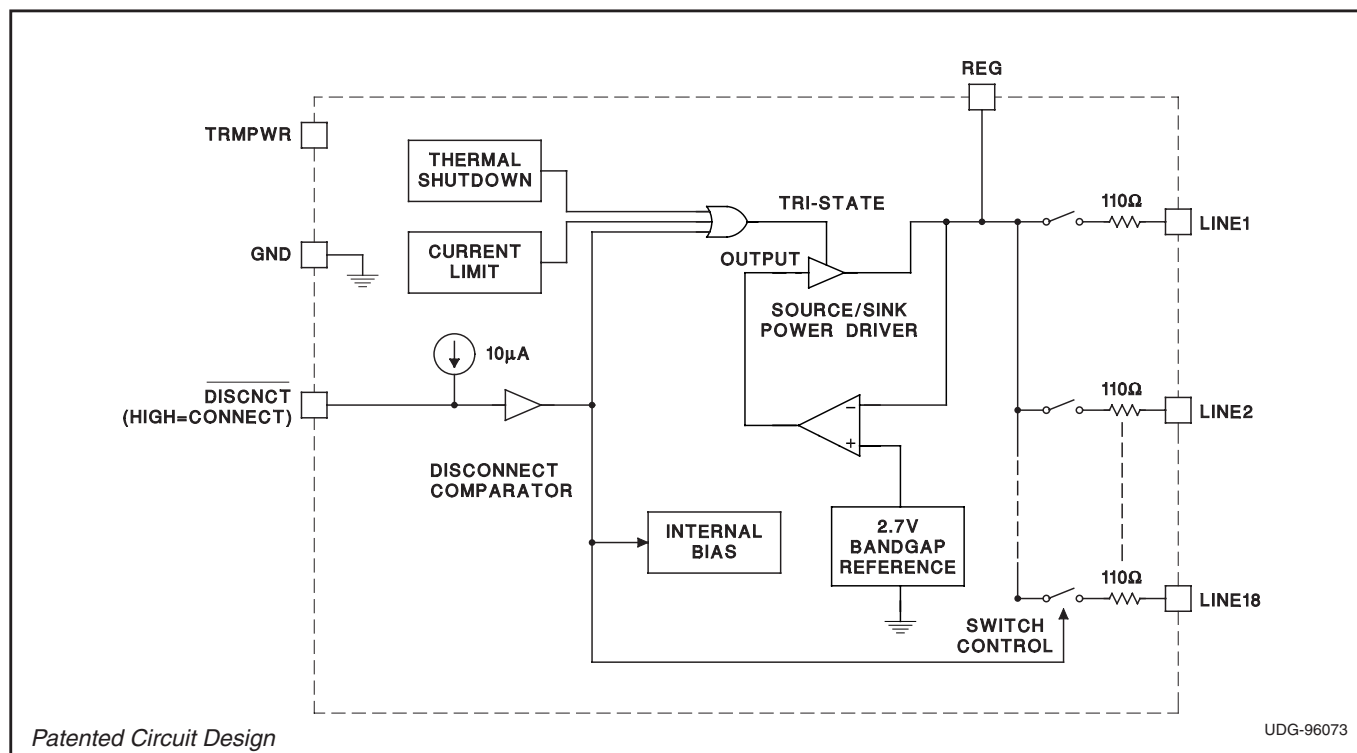
The power amplifier output stage allows the UCC5617 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5617, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with $TRMPWR = 0V$ or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in fast SCSI operation.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC.

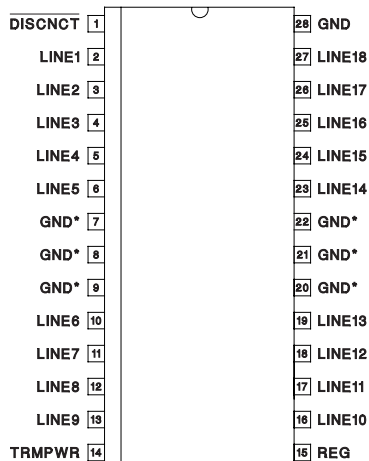
BLOCK DIAGRAM



UCC5617

CONNECTION DIAGRAMS

SOIC-28 (Top View) DWP Package



* DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.

ABSOLUTE MAXIMUM RATINGS

TEMPWR. +7V
Signal Line Voltage 0V to +7V
Regulator Output Current 1A
Storage Temperature -65°C to +150°C
Operating Junction Temperature -55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) 300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

UCC5617

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for $T_A = 0^\circ\text{C}$ to 70°C ,
 $\text{TRMPWR} = 4.75\text{V}$, $\text{DISCNCT} = 0\text{V}$, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|-------|-------|-------|------------------|
| Supply Current Section | | | | | |
| TERMPWR Supply Current | All Termination Lines = Open | | 1 | 2 | mA |
| | All Termination Lines = 0.2V | | 420 | 440 | mA |
| Power Down Mode | $\overline{\text{DISCNCT}} = 0\text{V}$ | | 50 | 100 | μA |
| Output Section (Termination Lines) | | | | | |
| Termination Impedance | (Note 3) | 104.5 | 110 | 115.5 | Ω |
| Output High Voltage | $V_{\text{TRMPWR}} = 4\text{V}$ (Note 1) | 2.6 | 2.8 | 3 | V |
| Max Output Current | $V_{\text{LINE}} = 0.2\text{V}$, $T_J = 25^\circ\text{C}$ | -22.1 | -23.3 | -24 | mA |
| | $V_{\text{LINE}} = 0.2\text{V}$ | -20.7 | -23.3 | -24 | mA |
| | $V_{\text{LINE}} = 0.2\text{V}$, $\text{TERMPWR} = 4\text{V}$, $T_J = 25^\circ\text{C}$ (Note 1) | -21 | -23.3 | -24 | mA |
| | $V_{\text{LINE}} = 0.2\text{V}$, $\text{TRMPWR} = 4\text{V}$ (Note 1) | -20 | -23 | -24 | mA |
| | $V_{\text{LINE}} = 0.5\text{V}$ | | | -22.4 | mA |
| Output Leakage | $\overline{\text{DISCNCT}} = 2.4\text{V}$, $\text{TRMPWR} = 0\text{V}$ to 5.25V , $\text{REG} = 0.2\text{V}$, $V_{\text{LINE}} = 5.25\text{V}$ | | 10 | 400 | nA |
| Output Capacitance | $\overline{\text{DISCNCT}} = 2.4\text{V}$ (Note 2) | | 2 | 3.5 | pF |
| Regulator Section | | | | | |
| Regulator Output Voltage | | 2.6 | 2.8 | 3 | V |
| Drop Out Voltage | All Termination Lines = 0.2V | | 0.4 | 0.8 | V |
| Short Circuit Current | $V_{\text{REG}} = 0\text{V}$ | -475 | -650 | -850 | mA |
| Sinking Current Capability | $V_{\text{REG}} = 3.5\text{V}$ | 200 | 400 | 800 | mA |
| Thermal Shutdown | | | 170 | | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis | | | 10 | | $^\circ\text{C}$ |
| Disconnect Section | | | | | |
| Disconnect Threshold | | 0.8 | 1.5 | 2 | V |
| Input Current | $\overline{\text{DISCNCT}} = 0\text{V}$ | | -10 | -30 | μA |

Note 1: Measuring each termination line while other 17 are low (0.2V).

Note 2: Guaranteed by design. Not 100% tested in production.

Note 3: Tested by measuring I_{OUT} with $V_{\text{OUT}} = 0.2\text{V}$ and V_{OUT} with no load, then calculating: $Z = \frac{V_{\text{OUT}} \text{ N.L.} - 0.2\text{V}}{I_{\text{OUT}} \text{ at } 0.2\text{V}}$

PIN DESCRIPTIONS

DISCNCT: Taking this pin low causes the 18 channels to become high impedance and the chip to go into low-power mode; a high or open state allows the channels to provide normal termination.

GND: Ground reference for the IC.

LINE1–LINE18: 110 Ω termination channels.

REG: Output of the internal 2.8V regulator.

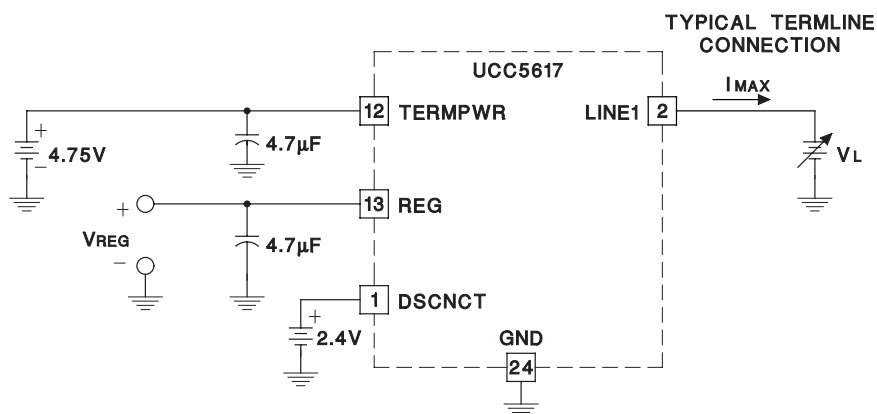
TRMPWR: Power for the IC.

UCC5617

APPLICATION INFORMATION

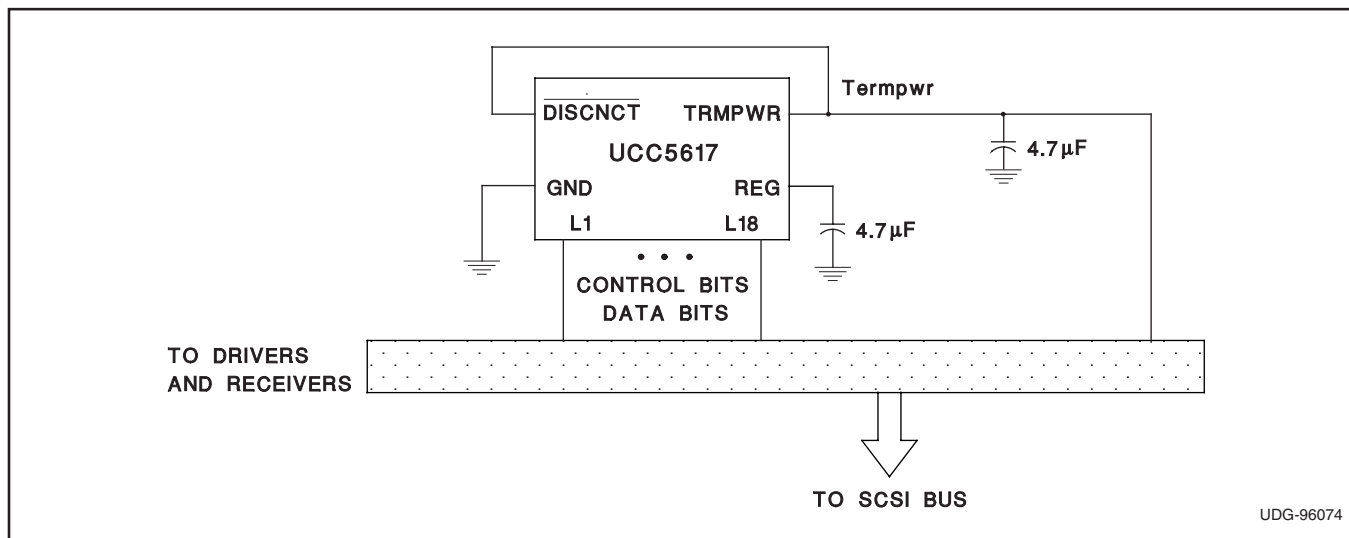
Procedure:

- 1) Measure V_{REG} N.L.
- 2) Set $V_L = 0.2V$
- 3) Measure I_{MAX} at 0.2V
- 4) Impedance = $\frac{V_{REG} \text{ N.L.} - 0.2V}{I_{MAX}}$



UDG-96108

Figure 1. Termlane Impedance Measurement Circuit



UDG-96074



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|-------------------------|----------------------|--------------|-------------------------|---------|
| UCC5617DWP | OBSOLETE | SOIC | DW | 28 | | TBD | Call TI | Call TI | 0 to 70 | UCC5617DWP | |
| UCC5617DWPG4 | OBSOLETE | SOIC | DW | 28 | | TBD | Call TI | Call TI | 0 to 70 | UCC5617DWP | |
| UCC5617DWPTR | OBSOLETE | SOIC | DW | 28 | | TBD | Call TI | Call TI | 0 to 70 | UCC5617DWP | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

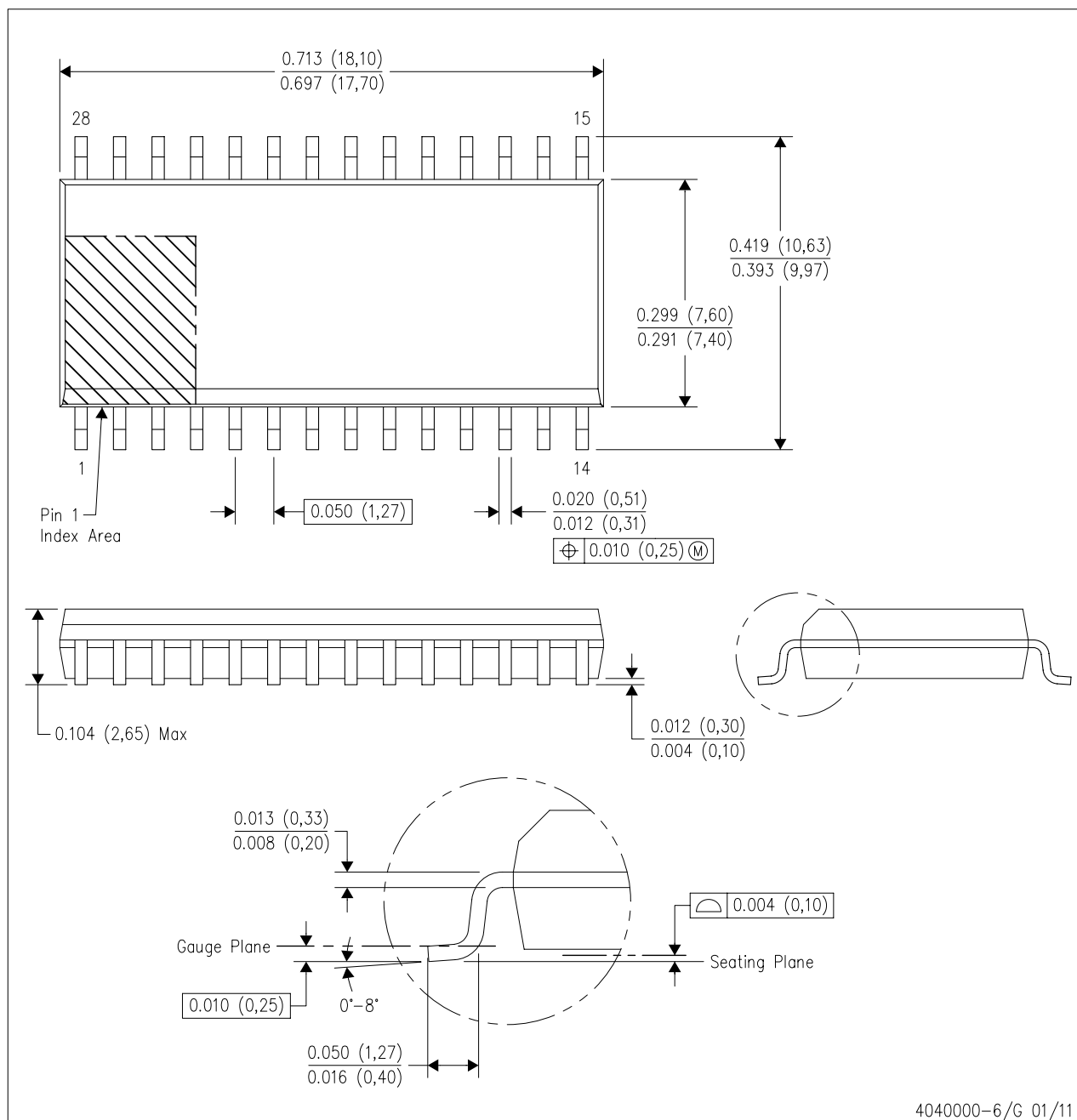
24-Mar-2015

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MECHANICAL DATA

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.

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