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SN74ALS841, SN74AS841A, SN74ALS842 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity**
- **Buffered Control Inputs to Reduce dc Loading Effects**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

description

These 10-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

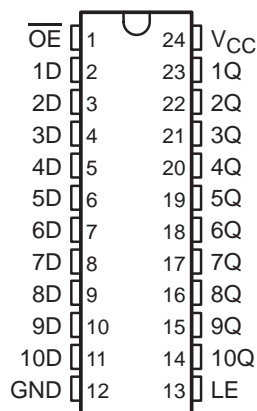
The ten latches are transparent D-type latches. The SN74ALS841 and SN74AS841A have noninverting data (D) inputs. The SN74ALS842 has inverting \bar{D} inputs.

A buffered output-enable (\overline{OE}) input places the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

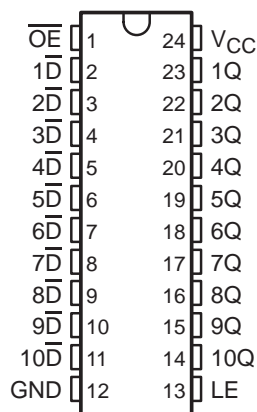
\overline{OE} does not affect the internal operation of the latches. Previously stored data can be retained or new data can be entered while the outputs are off.

The SN74ALS841, SN74AS841A, and SN74ALS842 are characterized for operation from 0°C to 70°C.

SN74ALS841, SN74AS841A . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS842 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS841, SN74AS841A, SN74ALS842

10-BIT BUS-INTERFACE D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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Function Tables

SN74ALS841, SN74AS841A

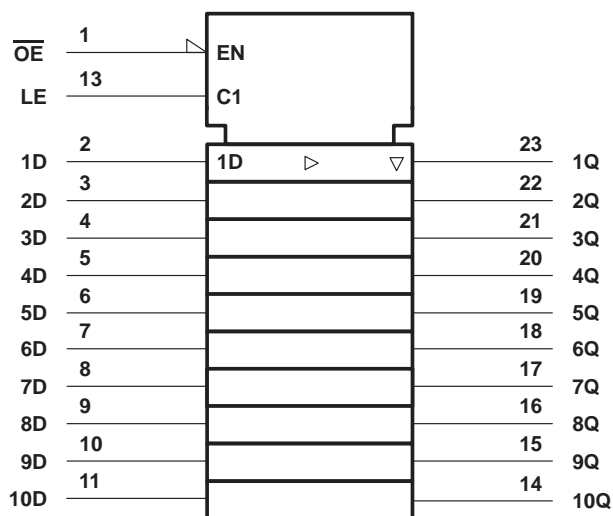
INPUTS			OUTPUT Q
\overline{OE}	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN74ALS842

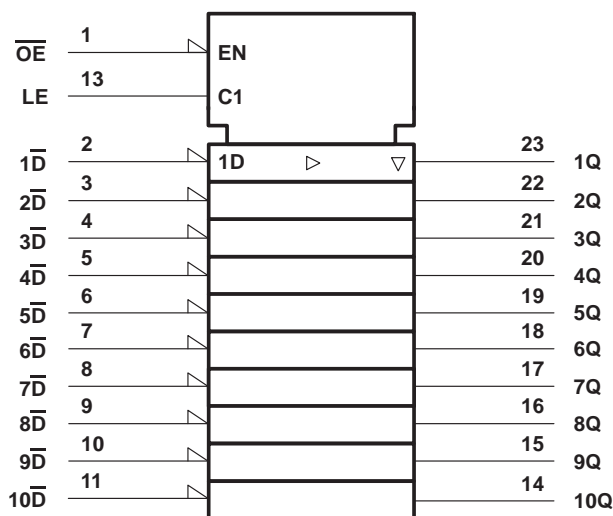
INPUTS			OUTPUT Q
\overline{OE}	LE	\overline{D}	
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

logic symbols†

SN74ALS841, SN74AS841A



SN74ALS842

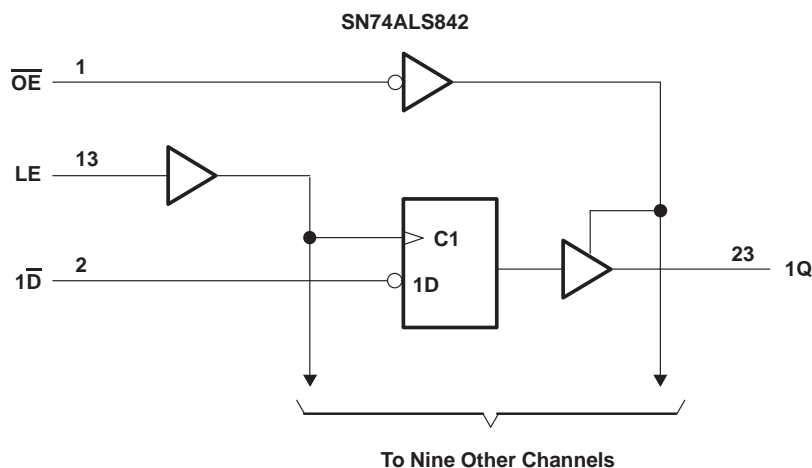
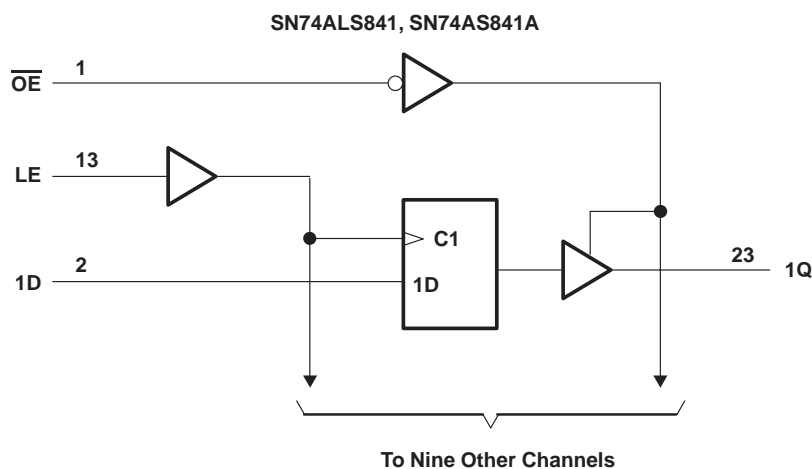


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALS841, SN74AS841A, SN74ALS842 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN74ALS841, SN74ALS842	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS841, SN74AS841A, SN74ALS842 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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recommended operating conditions

		SN74ALS841 SN74ALS842			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
t_w	Pulse duration, LE high	20			ns
t_{su}	Setup time, data before LE↓	10			ns
t_h	Hold time, data after LE↓	5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS841 SN74ALS842		UNIT
				MIN	TYP†	
V _{IK}		V _{CC} = 4.5 V,	I _I = −18 mA	−1.2		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V,	I _{OH} = −0.4 mA	V _{CC} − 2		V
		V _{CC} = 4.5 V,	I _{OH} = −2.6 mA	2.4	3.2	
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	V
			I _{OL} = 24 mA	0.35	0.5	
I _{OZH}		V _{CC} = 5.5 V,	V _O = 2.7 V	20		μA
I _{OZL}		V _{CC} = 5.5 V,	V _O = 0.4 V	−20		μA
I _I		V _{CC} = 5.5 V,	V _I = 7 V	0.1		mA
I _{IH}		V _{CC} = 5.5 V,	V _I = 2.7 V	20		μA
I _{IL}		V _{CC} = 5.5 V,	V _I = 0.4 V	−0.1		mA
I _O ‡		V _{CC} = 5.5 V,	V _O = 2.25 V	−30	−112	mA
I _{CC}	SN74ALS841	V _{CC} = 5.5 V	Outputs high	19	30	mA
			Outputs low	38	62	
			Outputs disabled	23	40	
	SN74ALS842	V _{CC} = 5.5 V	Outputs high	20	35	
			Outputs low	48	74	
			Outputs disabled	27	44	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN74ALS841, SN74AS841A, SN74ALS842
10-BIT BUS-INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX†		UNIT
			SN74ALS841		
			MIN	MAX	
tPLH	D	Q	2	13	ns
tPHL			2	13	
tPLH	LE	Q	7	21	ns
tPHL			8	26	
tPZH	\overline{OE}	Q	2	12	ns
tPZL			2	12	
tPHZ	\overline{OE}	Q	2	10	ns
tPLZ			2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX†		UNIT
			SN74ALS842		
			MIN	MAX	
tPLH	\overline{D}	Q	4	18	ns
tPHL			3	13	
tPLH	LE	Q	8	27	ns
tPHL			6	20	
tPZH	\overline{OE}	Q	2	12	ns
tPZL			2	12	
tPHZ	\overline{OE}	Q	1	10	ns
tPLZ			2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T _A : SN74AS841A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS841, SN74AS841A, SN74ALS842

10-BIT BUS-INTERFACE D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS059C – DECEMBER 1983 – REVISED JANUARY 1995

recommended operating conditions

		SN74AS841A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, LE high	4			ns
t_{su}	Setup time, data before LE↓	2.5			ns
t_h	Hold time, data after LE↓	2.5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74AS841A			UNIT
		MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			–1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -15\text{ mA}$	2.4	3.2		
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -24\text{ mA}$	2			
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$		0.35	0.5	V
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			50	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$			–50	μA
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			–0.5	mA
I_O^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	–30		–112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high		36	mA
		Outputs low		58	
		Outputs disabled		56	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN74ALS841, SN74AS841A, SN74ALS842 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics (see Figure 1)

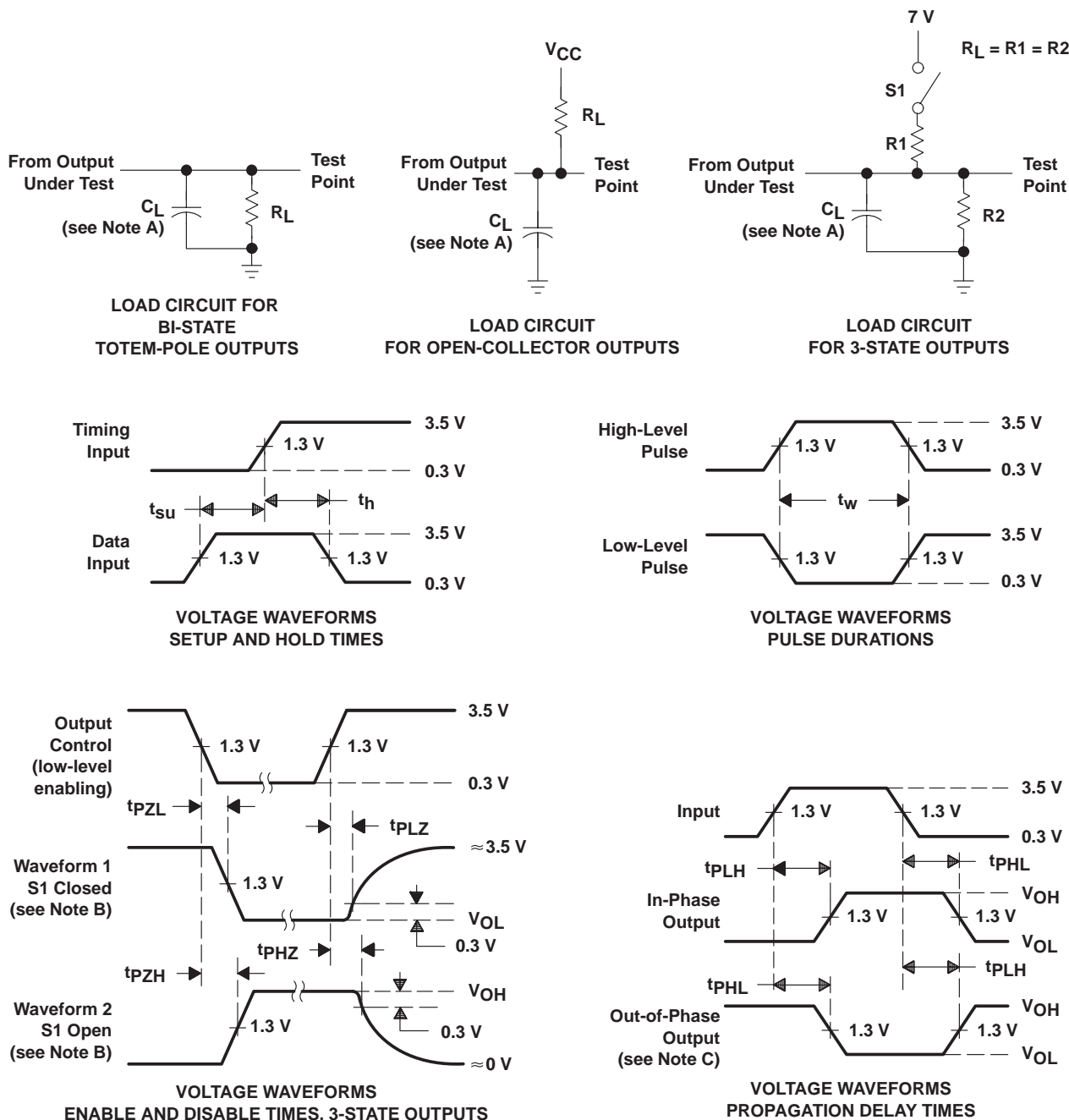
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX†		UNIT
			SN74AS841A		
			MIN	MAX	
tPLH	D	Q	1	6.5	ns
tPHL			1	10.5	
tPLH	LE	Q	2	12	ns
tPHL			2	12	
tPZH	\overline{OE}	Q	2	14	ns
tPZL			2	16	
tPHZ	\overline{OE}	Q	1	8	ns
tPLZ			1	8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN74ALS841, SN74AS841A, SN74ALS842 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. When measuring propagation delay items of 3-state outputs, switch S1 is open.

D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS841DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS841	Samples
SN74ALS842DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74ALS842NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74AS841ADW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74AS841ADWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74AS841ANT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



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PACKAGE OPTION ADDENDUM

15-Oct-2015

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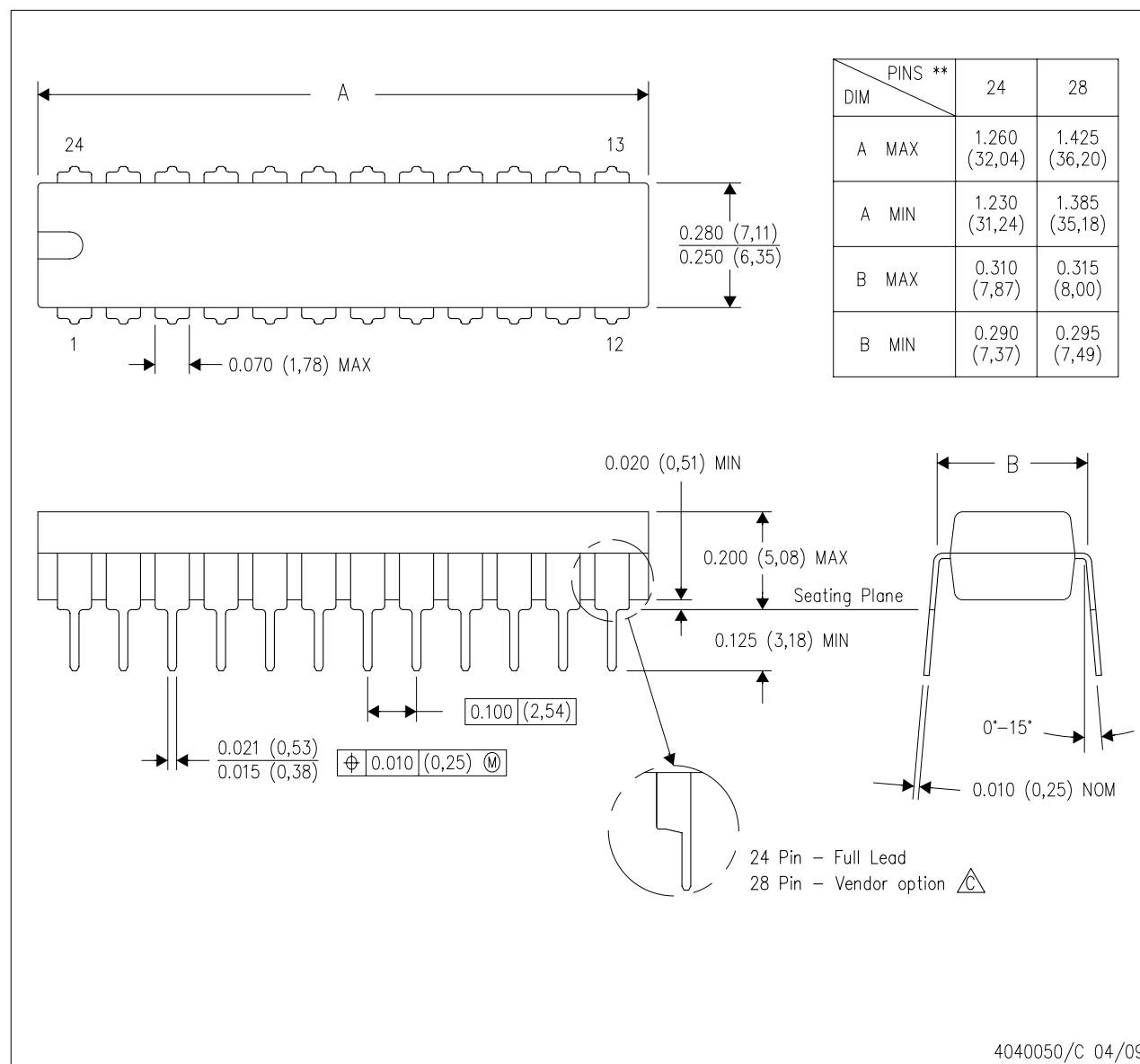
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MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

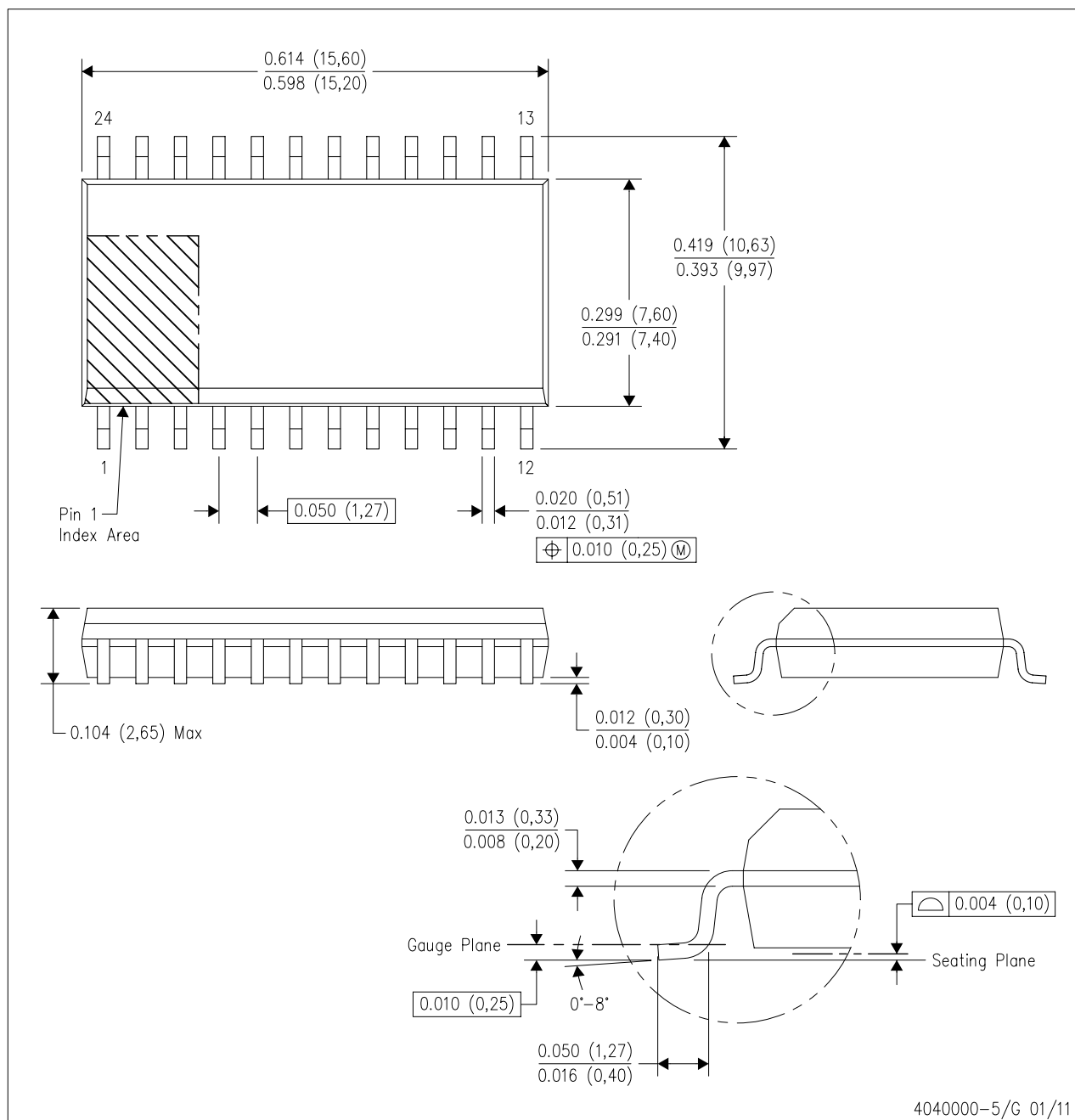


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - \triangle The 28 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

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