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SN54AHC367, SN74AHC367
HEX BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS

SCLS424E – JUNE 1998 – REVISED FEBRUARY 2002

- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

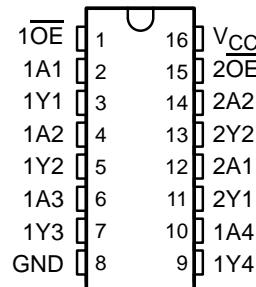
description

The 'AHC367 devices are hex buffers and line drivers designed for 2-V to 5.5-V V_{CC} operation.

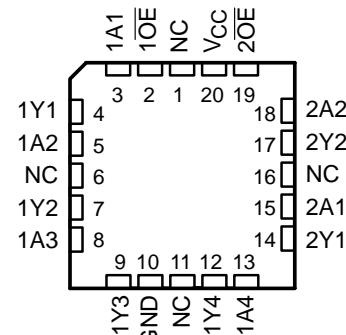
These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'AHC367 devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ($1\overline{OE}$ and $2\overline{OE}$) inputs. When \overline{OE} is low, the device passes noninverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHC367 . . . J OR W PACKAGE
SN74AHC367 . . . D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC367 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AHC367N	SN74AHC367N
	SOIC – D	Tube	SN74AHC367D	AHC367
		Tape and reel	SN74AHC367DR	
	SSOP – DB	Tape and reel	SN74AHC367DBR	HA367
	TSSOP – PW	Tape and reel	SN74AHC367PWR	HA367
-55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHC367DGVR	HA367
	CDIP – J	Tube	SNJ54AHC367J	SNJ54AHC367J
	CFP – W	Tube	SNJ54AHC367W	SNJ54AHC367W
	LCCC – FK	Tube	SNJ54AHC367FK	SNJ54AHC367FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54AHC367, SN74AHC367 HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS424E – JUNE 1998 – REVISED FEBRUARY 2002

FUNCTION TABLE (each buffer/driver)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

SN54AHC367, SN74AHC367
HEX BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS
 SCLS424E – JUNE 1998 – REVISED FEBRUARY 2002

recommended operating conditions (see Note 3)

		SN54AHC367		SN74AHC367		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 3 V	2.1	2.1		
		V _{CC} = 5.5 V	3.85	3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 3 V	0.9	0.9		
		V _{CC} = 5.5 V	1.65	1.65		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	-50	μA	mA
		V _{CC} = 3.3 V ± 0.3 V	-4	-4		
		V _{CC} = 5 V ± 0.5 V	-8	-8		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50	μA	mA
		V _{CC} = 3.3 V ± 0.3 V	4	4		
		V _{CC} = 5 V ± 0.5 V	8	8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	100		ns/V
		V _{CC} = 5 V ± 0.5 V	20	20		
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC367	SN74AHC367	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9	1.9	V
		3 V	2.9	3		2.9	2.9	
		4.5 V	4.4	4.5		4.4	4.4	
	I _{OH} = -4 mA	3 V	2.58			2.48	2.48	
	I _{OH} = -8 mA	4.5 V	3.94			3.8	3.8	
V _{OL}	I _{OL} = 50 μA	2 V		0.1		0.1	0.1	V
		3 V		0.1		0.1	0.1	
		4.5 V		0.1		0.1	0.1	
	I _{OL} = 4 mA	3 V		0.36		0.5	0.44	
	I _{OL} = 8 mA	4.5 V		0.36		0.5	0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V		±0.1		±1*	±1	μA
I _{OZ}	V _I = V _{CC} or GND, V _O = V _{CC} or GND, OE = V _{IH}	5.5 V		±0.25		±2.5	±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		4		40	40	μA
C _i	V _I = V _{CC} or GND	5 V		3	10		10	pF
C _o	V _O = V _{CC} or GND	5 V		5.1				pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54AHC367, SN74AHC367
HEX BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS

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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			SN54AHC367		SN74AHC367		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	A	Y	CL = 15 pF	4.7*	8.3*	10*	1*	10*	1	10	ns
tPHL				4.7*	8.3*	10*	1*	10*	1	10	
tPZH	OE	Y	CL = 15 pF	5.1*	10.5*	12.5*	1*	12.5*	1	12.5	ns
tPZL				5.1*	10.5*	12.5*	1*	12.5*	1	12.5	
tPHZ	OE	Y	CL = 15 pF	4*	10.5*	12.5*	1*	12.5*	1	12.5	ns
tPLZ				4.9*	10.5*	12.5*	1*	12.5*	1	12.5	
tPLH	A	Y	CL = 50 pF	6.1	11.8	13.5	1	13.5	1	13.5	ns
tPHL				6.2	11.8	13.5	1	13.5	1	13.5	
tPZH	OE	Y	CL = 50 pF	6.4	14	16	1	16	1	16	ns
tPZL				6.8	14	16	1	16	1	16	
tPHZ	OE	Y	CL = 50 pF	6.2	13.6	15.5	1	15.5	1	15.5	ns
tPLZ				7.3	13.6	15.5	1	15.5	1	15.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			SN54AHC367		SN74AHC367		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	A	Y	CL = 15 pF	3.4*	5.9*	7*	1*	7*	1	7	ns
tPHL				3.6*	5.9*	7*	1*	7*	1	7	
tPZH	OE	Y	CL = 15 pF	3.6*	7.2*	8.5*	1*	8.5*	1	8.5	ns
tPZL				3.8*	7.2*	8.5*	1*	8.5*	1	8.5	
tPHZ	OE	Y	CL = 15 pF	2.6*	7.2*	8.5*	0*	8.5*	0	8.5	ns
tPLZ				2.6*	7.2*	8.5*	0*	8.5*	0	8.5	
tPLH	A	Y	CL = 50 pF	4.3	7.9	9	1	9	1	9	ns
tPHL				4.5	7.9	9	1	9	1	9	
tPZH	OE	Y	CL = 50 pF	4.6	9.2	10.5	1	10.5	1	10.5	ns
tPZL				4.9	9.2	10.5	1	10.5	1	10.5	
tPHZ	OE	Y	CL = 50 pF	3.4	9.2	10.5	0	10.5	0	10.5	ns
tPLZ				4.5	9.2	10.5	0	10.5	0	10.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC367			UNIT
	MIN	TYP	MAX	
VOL(P)	0.9			V
VOL(V)	-0.8			V
VOH(V)	4.2			V
VIH(D)	3.5			V
VIL(D)	1.5			V

NOTE 4: Characteristics are for surface-mount packages only.

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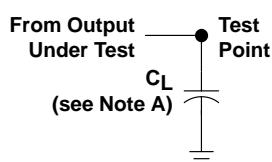


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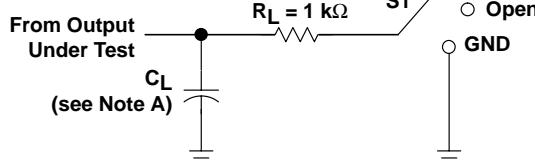
operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled No load, $f = 1$ MHz	22.4	pF

PARAMETER MEASUREMENT INFORMATION

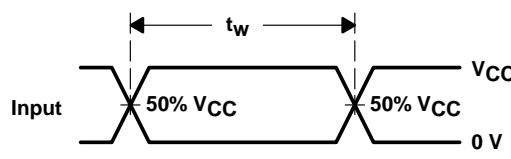


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

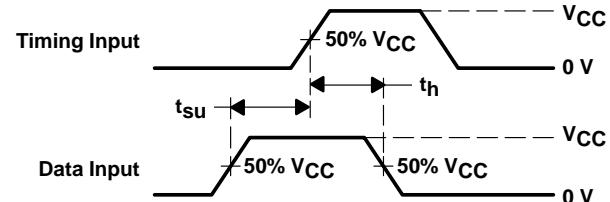


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

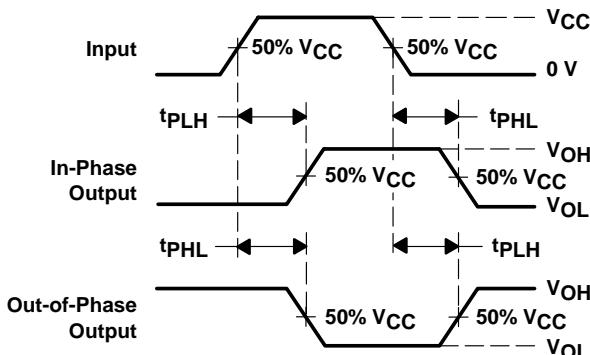
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



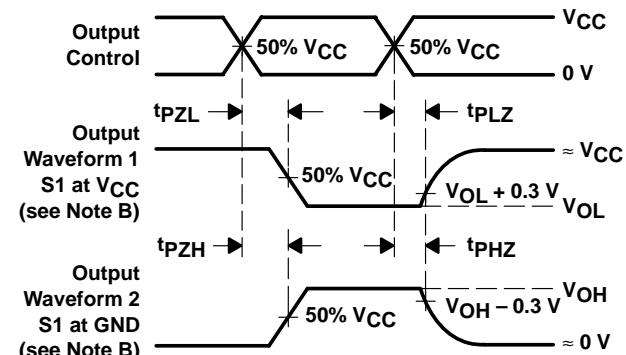
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC367D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC367	Samples
SN74AHC367DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC367	Samples
SN74AHC367N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC367N	Samples
SN74AHC367PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA367	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

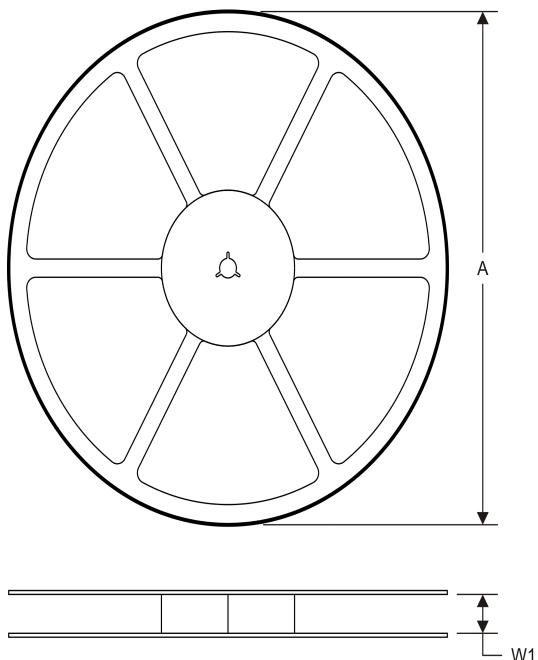
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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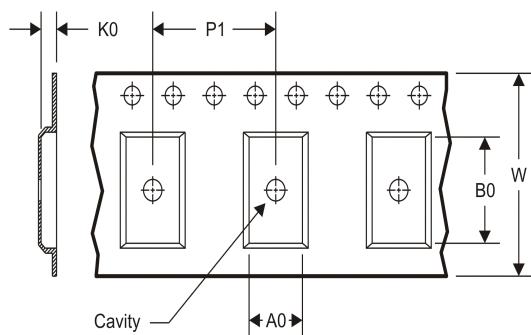
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

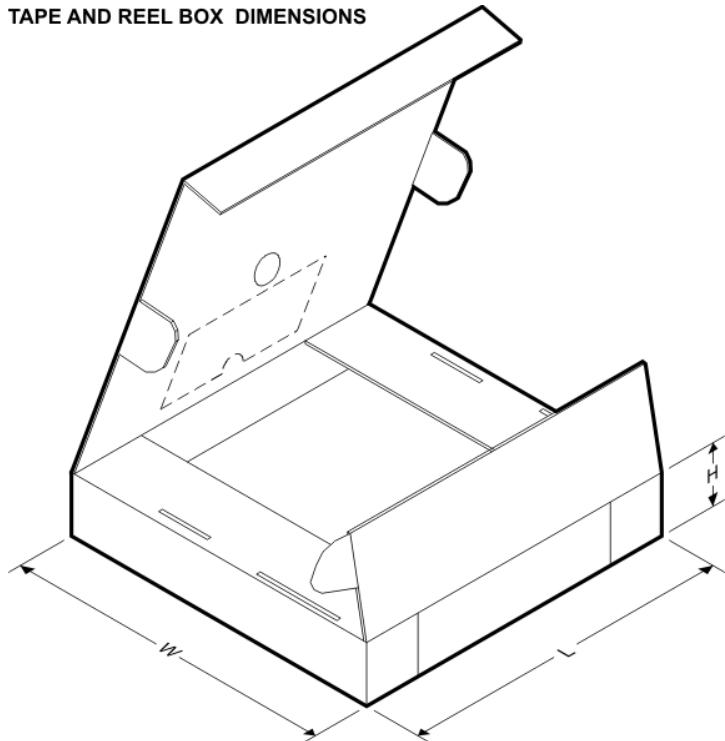


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC367DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC367PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

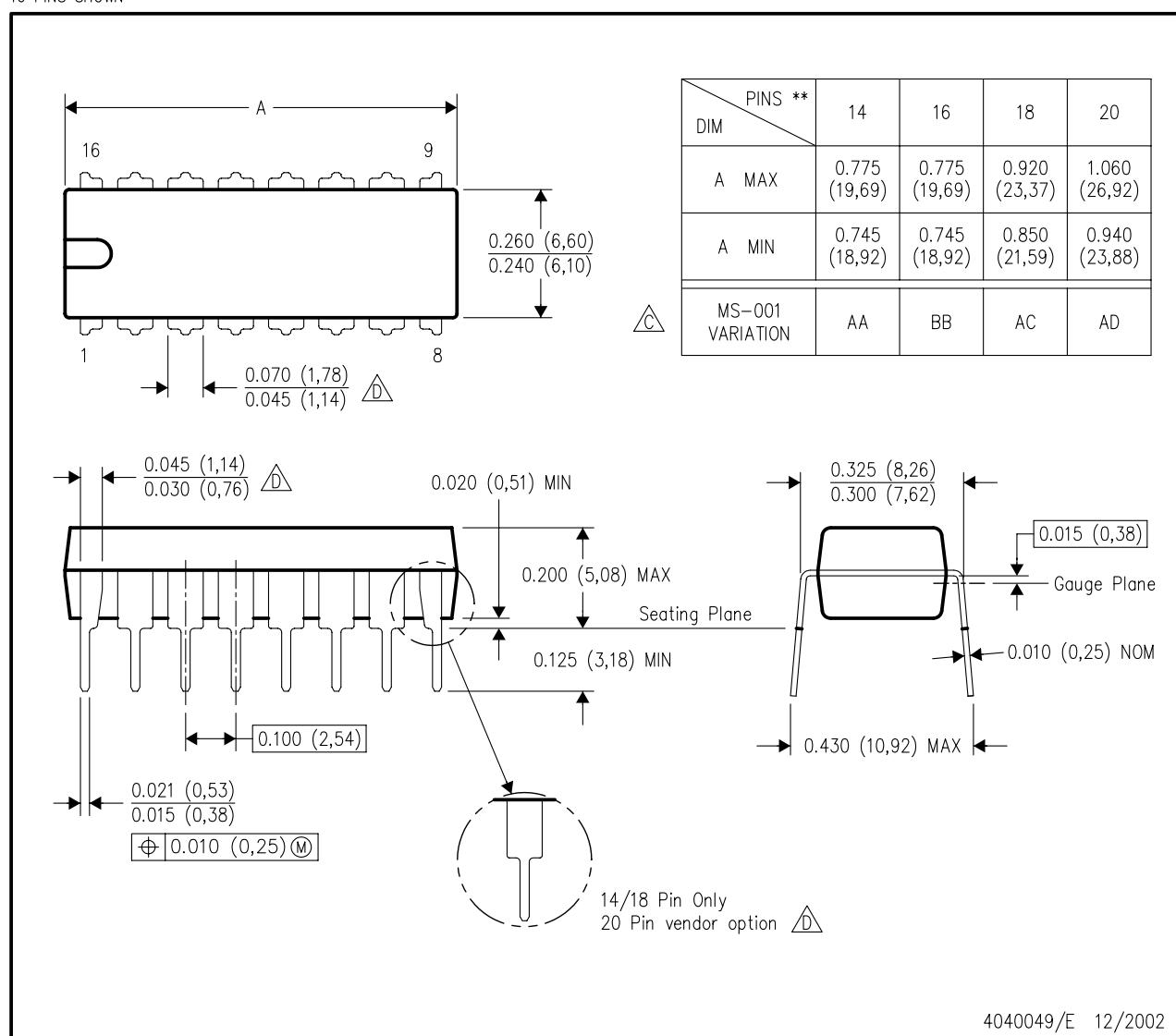
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC367DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AHC367PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

MECHANICAL DATA

N (R-PDIP-T**)

16 PINS SHOWN

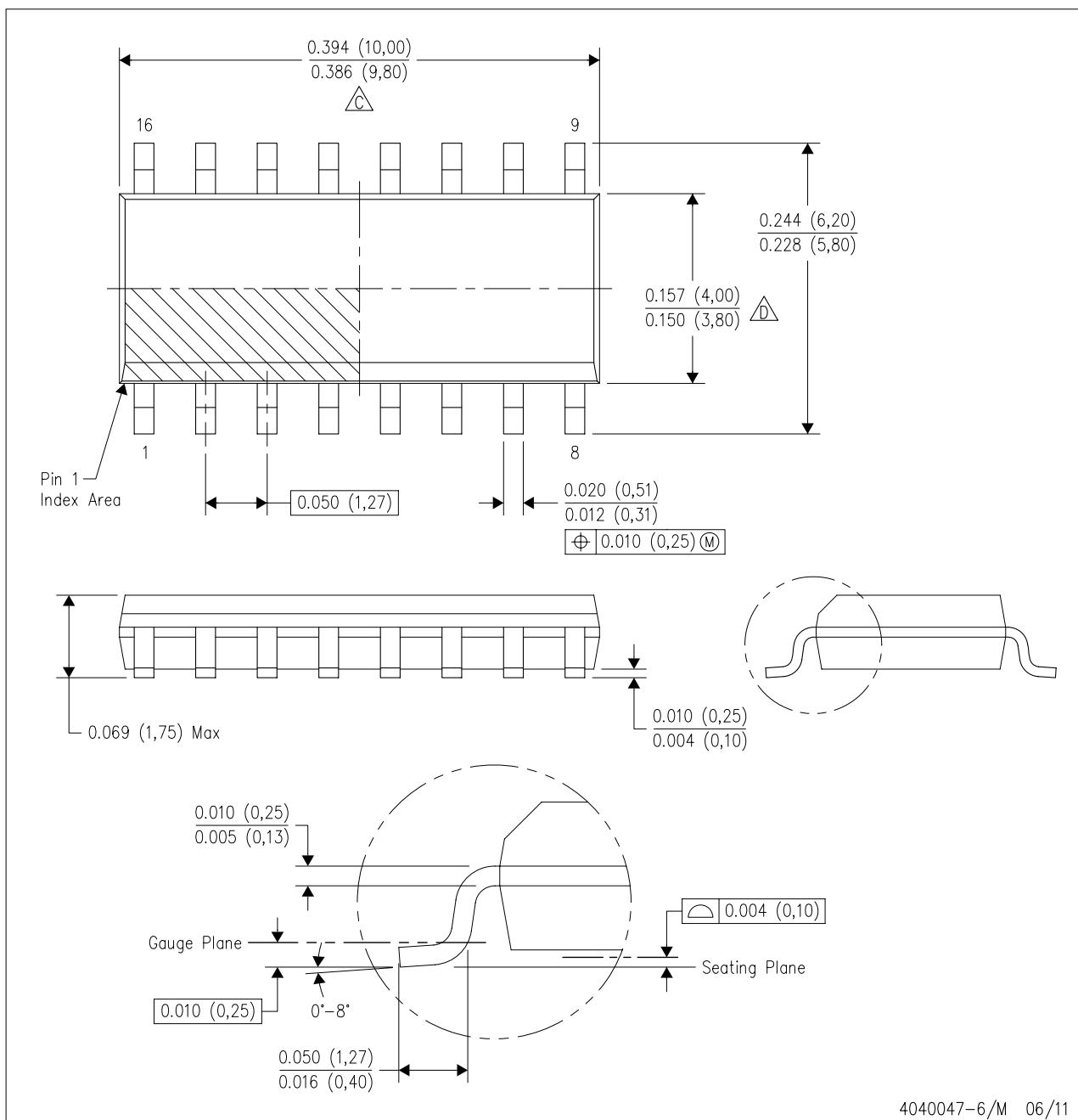
PLASTIC DUAL-IN-LINE PACKAGE



MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall

 Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

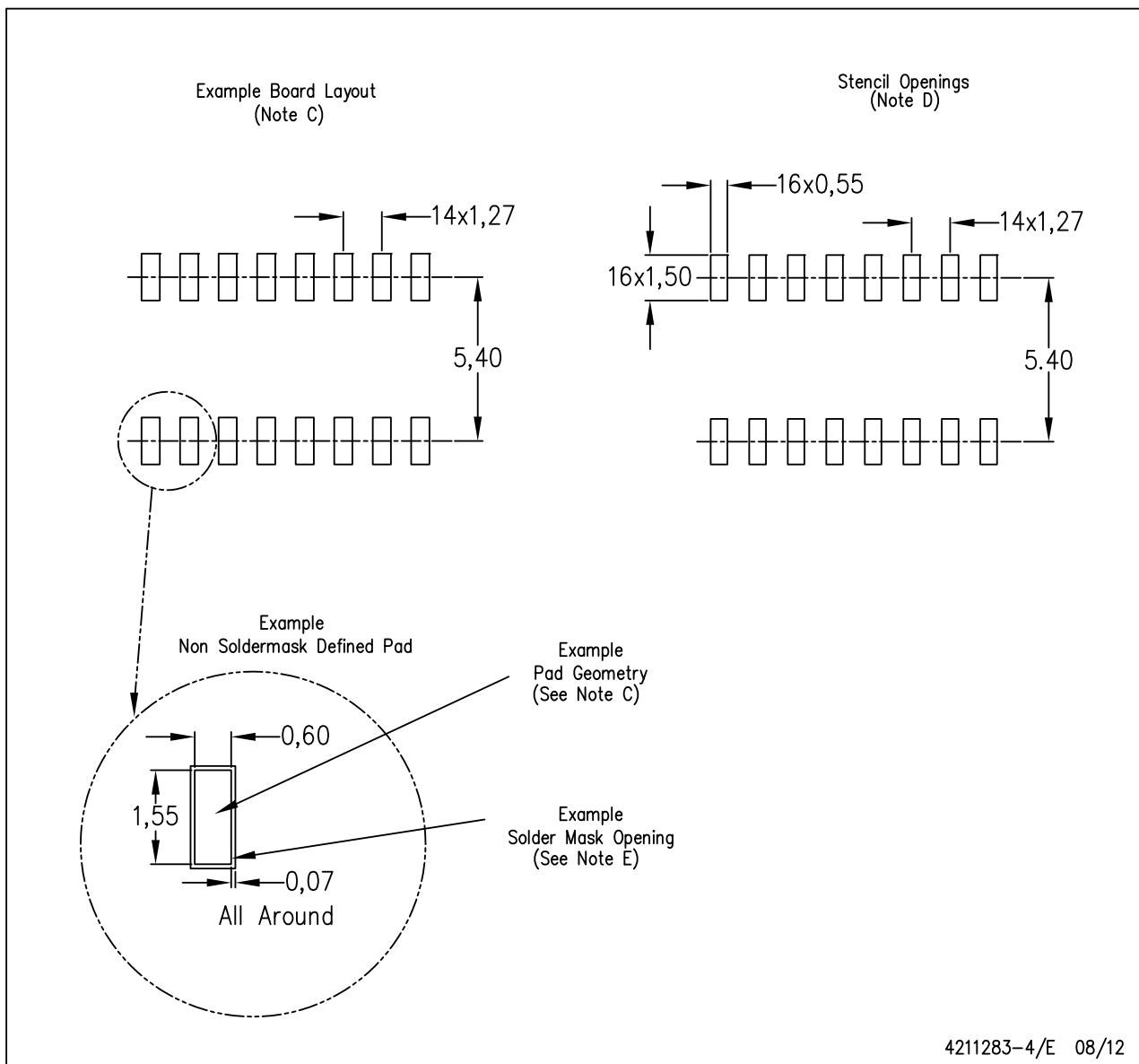
D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference GEDEC MS 012 Variation Ac.

LAND PATTERN DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



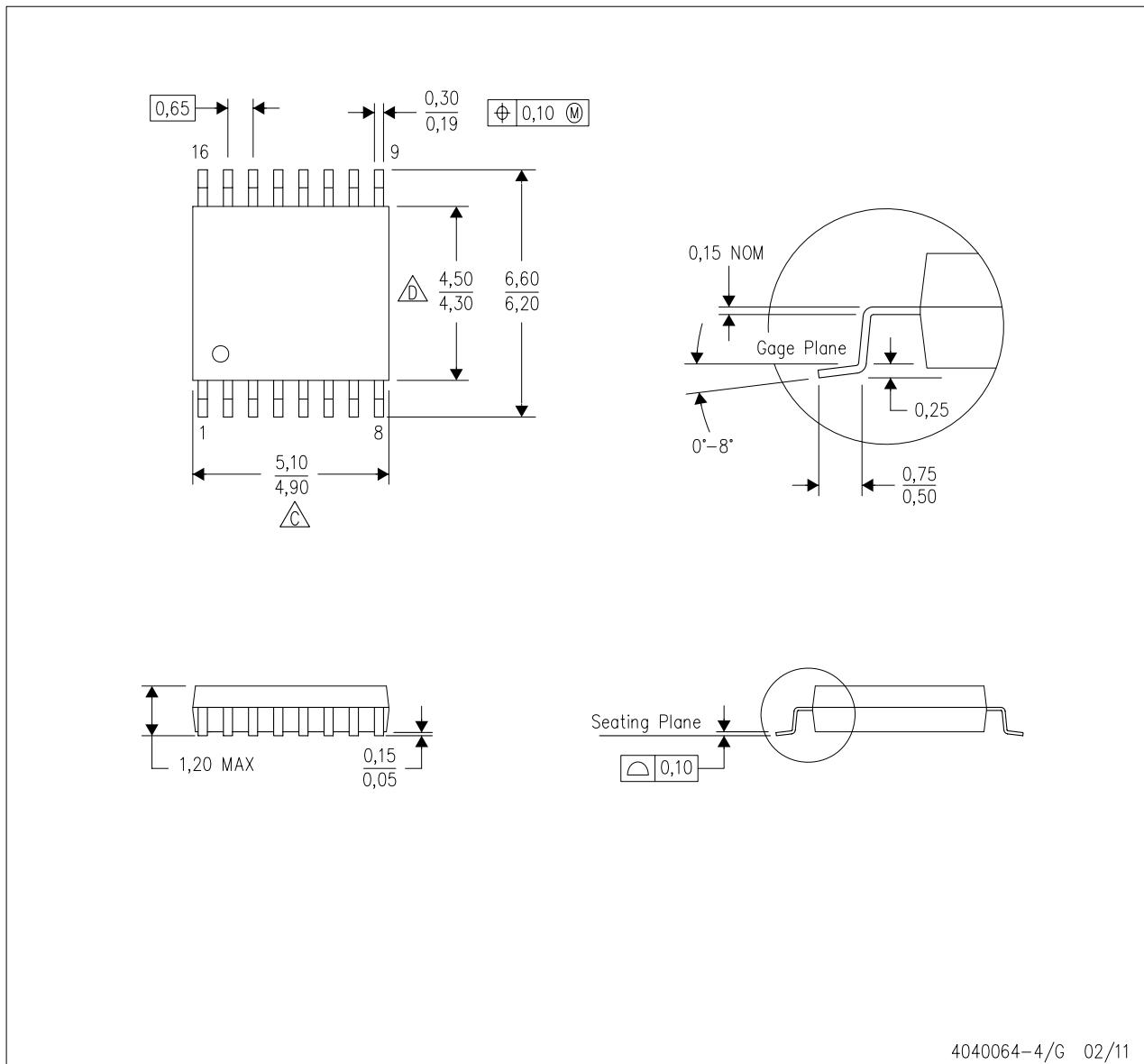
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

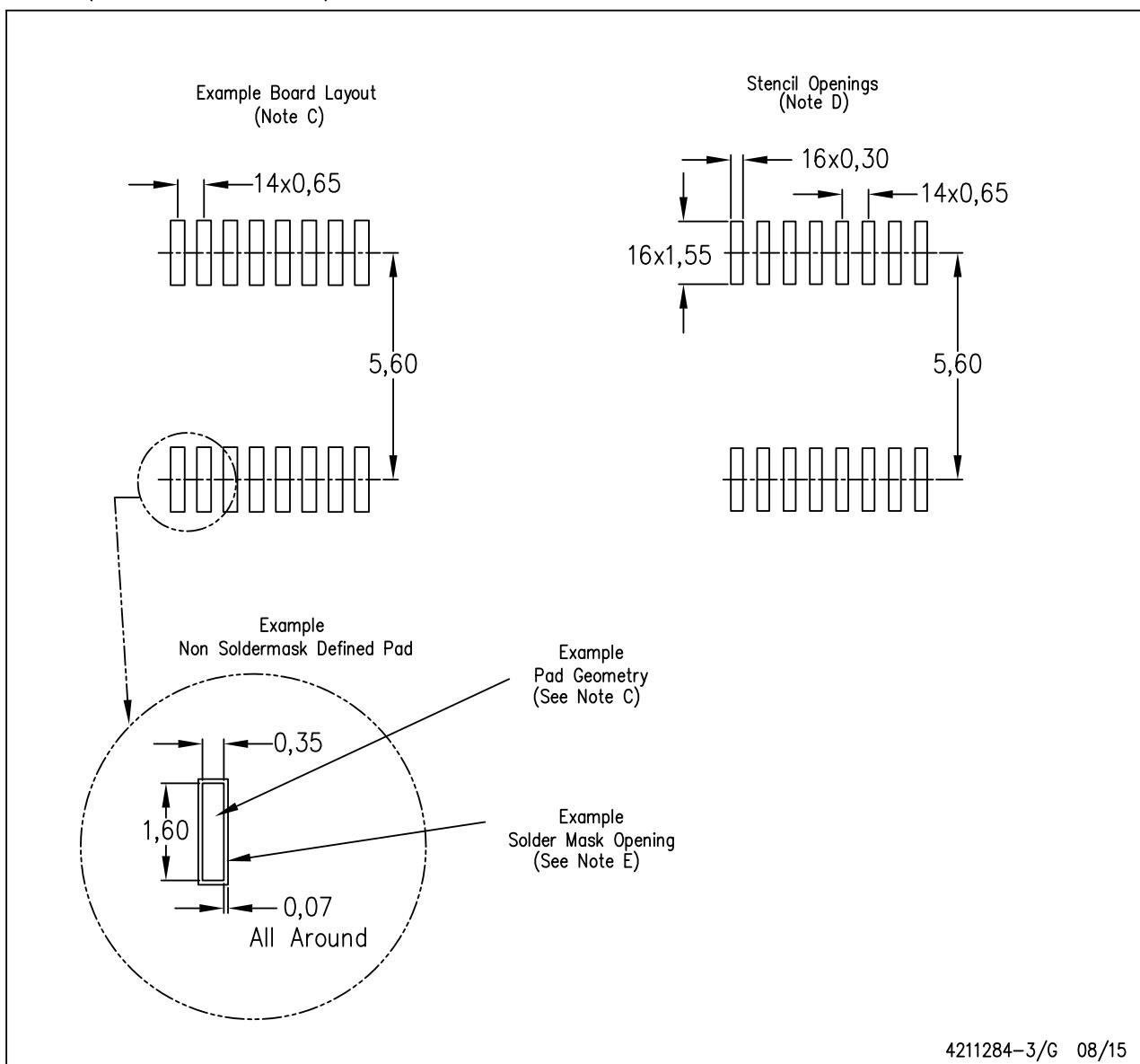
△D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

LAND PATTERN DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/G 08/15

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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