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**SN54AHC16240, SN74AHC16240**  
**16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

SCLS326G – MARCH 1996 – REVISED JANUARY 2000

- **Members of the Texas Instruments**  
**Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted**  
**CMOS) Process**
- **Operating Range 2-V to 5.5-V  $V_{CC}$**
- **Distributed  $V_{CC}$  and GND Pins Minimize**  
**High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB**  
**Layout**
- **Latch-Up Performance Exceeds 250 mA Per**  
**JESD 17**
- **Package Options Include Plastic Shrink**  
**Small-Outline (DL), Thin Shrink**  
**Small-Outline (DGG), and Thin Very**  
**Small-Outline (DGV) Packages and 380-mil**  
**Fine-Pitch Ceramic Flat (WD) Package**  
**Using 25-mil Center-to-Center Spacings**

**description**

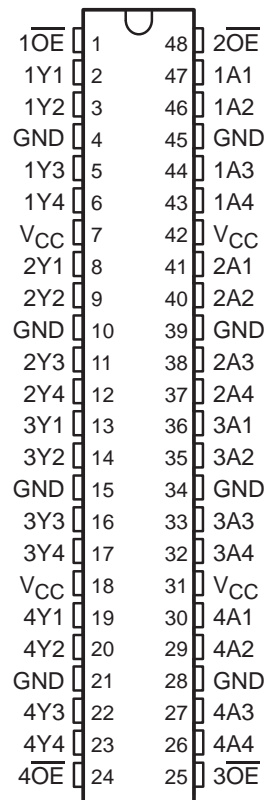
The 'AHC16240 devices are 16-bit buffers and line drivers designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. They provide inverting outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC16240 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHC16240 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54AHC16240 . . . WD PACKAGE  
SN74AHC16240 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



**FUNCTION TABLE**  
(each 4-bit buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z



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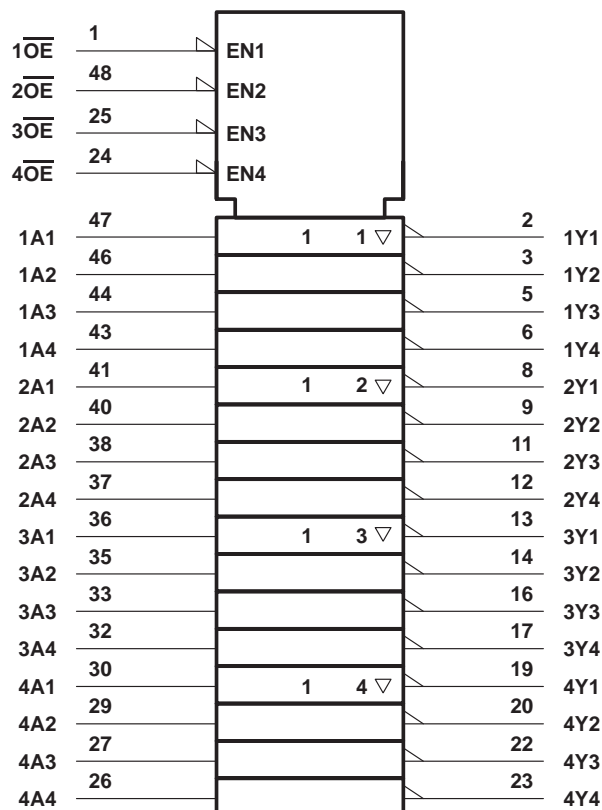
# SN54AHC16240, SN74AHC16240

## 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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#### logic symbol†

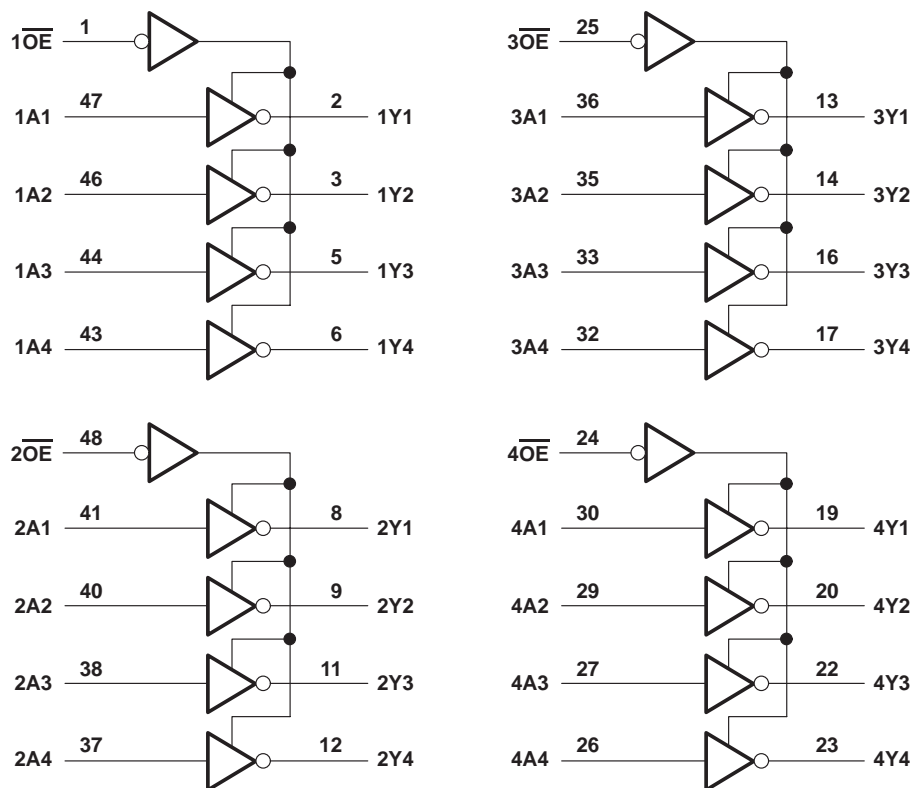


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	−0.5 V to 7 V	
Input voltage range, $V_I$ (see Note 1)	−0.5 V to 7 V	
Output voltage range, $V_O$ (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V	
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	−20 mA	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA	
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA	
Continuous current through each $V_{CC}$ or GND	±75 mA	
Package thermal impedance, $\theta_{JA}$ (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, $T_{sta}$	−65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

# SN54AHC16240, SN74AHC16240

## 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

			SN54AHC16240		SN74AHC16240		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5		V
		V <sub>CC</sub> = 3 V	2.1		2.1		
		V <sub>CC</sub> = 5.5 V	3.85		3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5		0.5		V
		V <sub>CC</sub> = 3 V	0.9		0.9		
		V <sub>CC</sub> = 5.5 V	1.65		1.65		
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	−50		−50		μA
		V <sub>CC</sub> = 3.3 ± 0.3 V	−4		−4		mA
		V <sub>CC</sub> = 5 ± 0.5 V	−8		−8		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50		50		μA
		V <sub>CC</sub> = 3.3 ± 0.3 V	4		4		mA
		V <sub>CC</sub> = 5 ± 0.5 V	8		8		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 ± 0.3 V	100		100		ns/V
		V <sub>CC</sub> = 5 ± 0.5 V	20		20		
T <sub>A</sub>	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC16240		SN74AHC16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = −50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I <sub>OH</sub> = −4 mA	3 V	2.58			2.48		2.48		
	I <sub>OH</sub> = −8 mA	4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V			±0.25		±2.5		±2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		40	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			2.5				10	pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			3.5					pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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**SN54AHC16240, SN74AHC16240**  
**16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$		5.3*	8.4*	1*	10*	1	10	ns
$t_{PHL}$					5.3*	8.4*	1*	10*	1	10	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		6.6*	10.6*	1*	12.5*	1	12.5	ns
$t_{PZL}$					6.6*	10.6*	1*	12.5*	1	12.5	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		7.8*	11.5*	1*	12.5*	1	12.5	ns
$t_{PLZ}$					7.8*	11.5*	1*	12.5*	1	12.5	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$		7.8	11.9*	1	13.5	1	13.5	ns
$t_{PHL}$					7.8	11.9	1	13.5	1	13.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		9.1	14.1	1	16	1	16	ns
$t_{PZL}$					9.1	14.1	1	16	1	16	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		10.3	14	1	16	1	16	ns
$t_{PLZ}$					10.3	14	1	16	1	16	
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1.5**				1.5	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

**switching characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$		3.6*	6*	1*	7*	1	6.5	ns
$t_{PHL}$					3.6*	6*	1*	7*	1	6.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		4.7*	7.3*	1*	8.5*	1	8.5	ns
$t_{PZL}$					4.7*	7.3*	1*	8.5*	1	8.5	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		5.2*	7.2*	1*	8.5*	1	8.5	ns
$t_{PLZ}$					5.2*	7.2*	1*	8.5*	1	8.5	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$		5.1	8	1	9	1	8.5	ns
$t_{PHL}$					5.1	8	1	9	1	8.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		6.2	9.3	1	10.5	1	10.5	ns
$t_{PZL}$					6.2	9.3	1	10.5	1	10.5	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		6.7	9.2	1	10.5	1	10.5	ns
$t_{PLZ}$					6.7	9.2	1	10.5	1	10.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1**				1	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

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# SN54AHC16240, SN74AHC16240

## 16-BIT BUFFERS/DRIVERS

## WITH 3-STATE OUTPUTS

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER	SN74AHC16240			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.6		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		–0.6		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.6		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

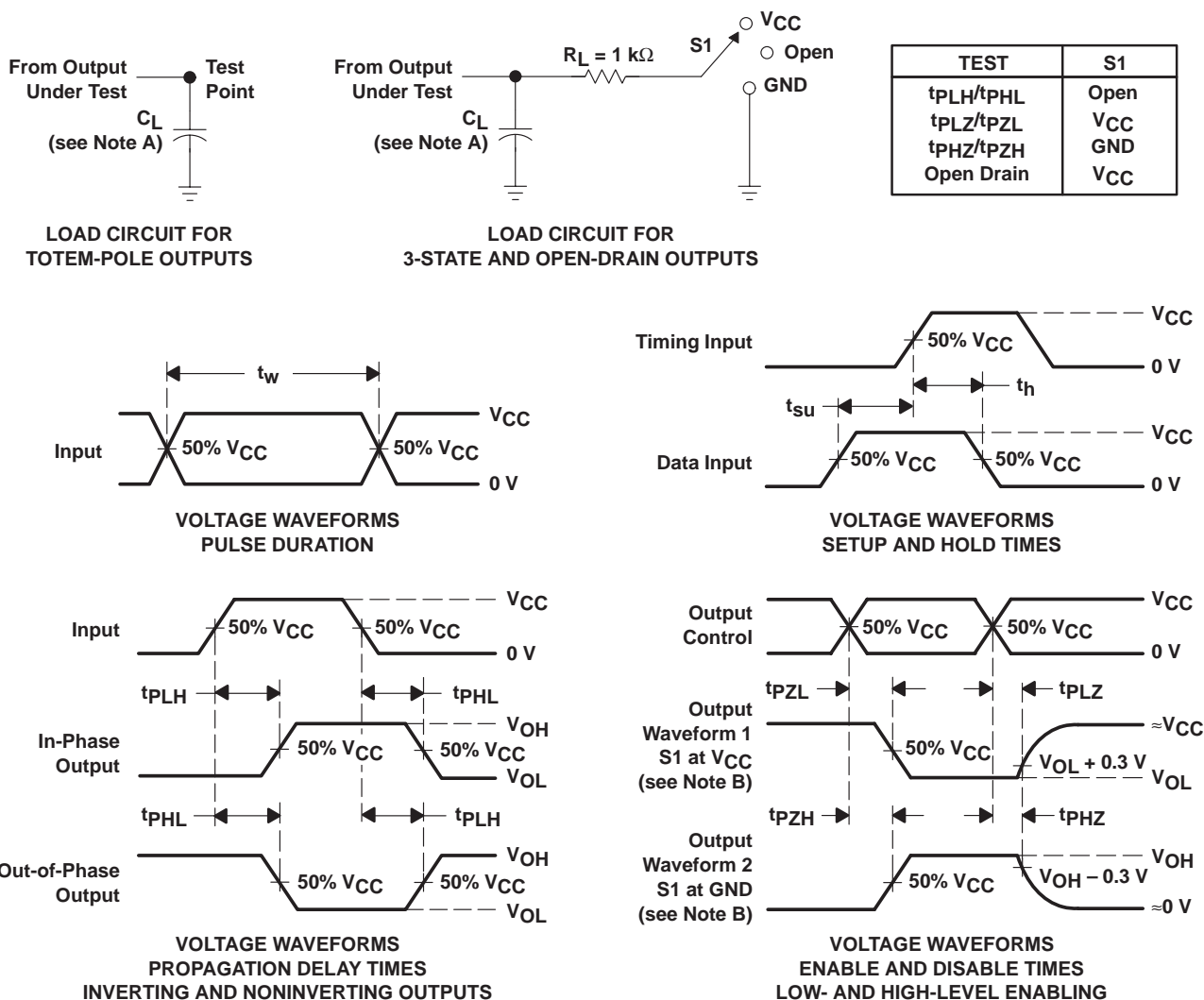
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	10	pF

**SN54AHC16240, SN74AHC16240**  
**16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**



## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AHC16240DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHC16240DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHC16240DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHC16240DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16240DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16240DGV	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16240DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16240DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

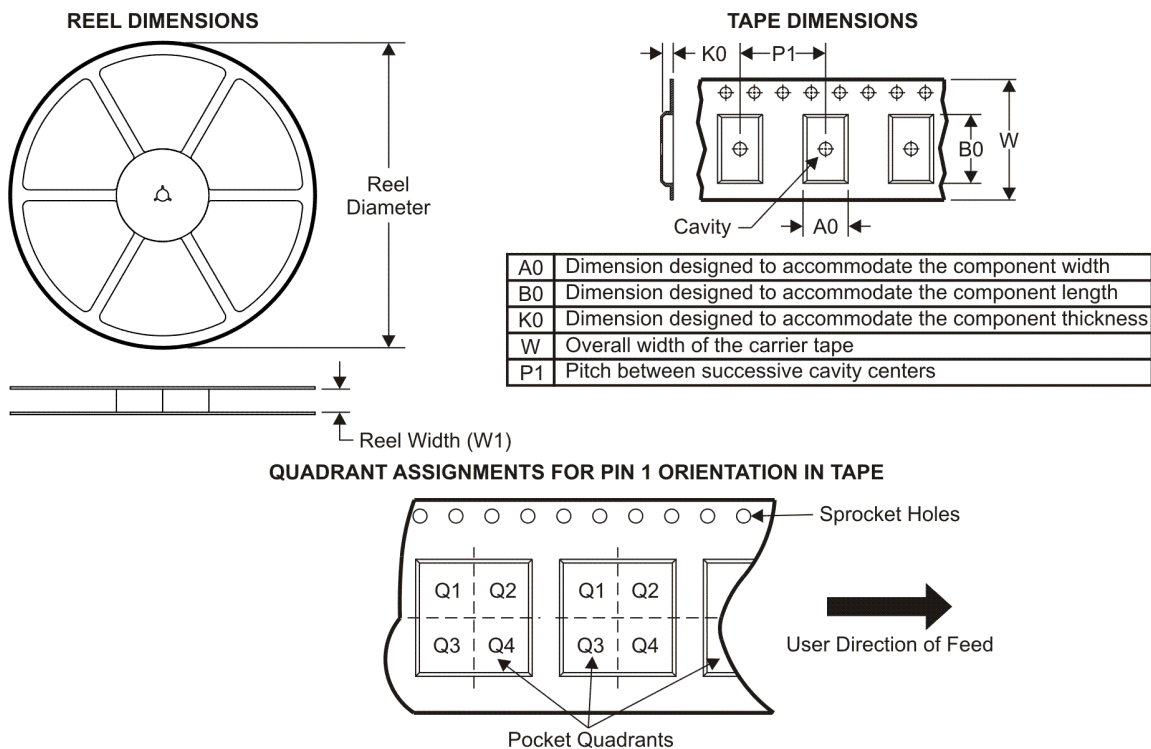
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## PACKAGE MATERIALS INFORMATION

### TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC16240DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74AHC16240DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

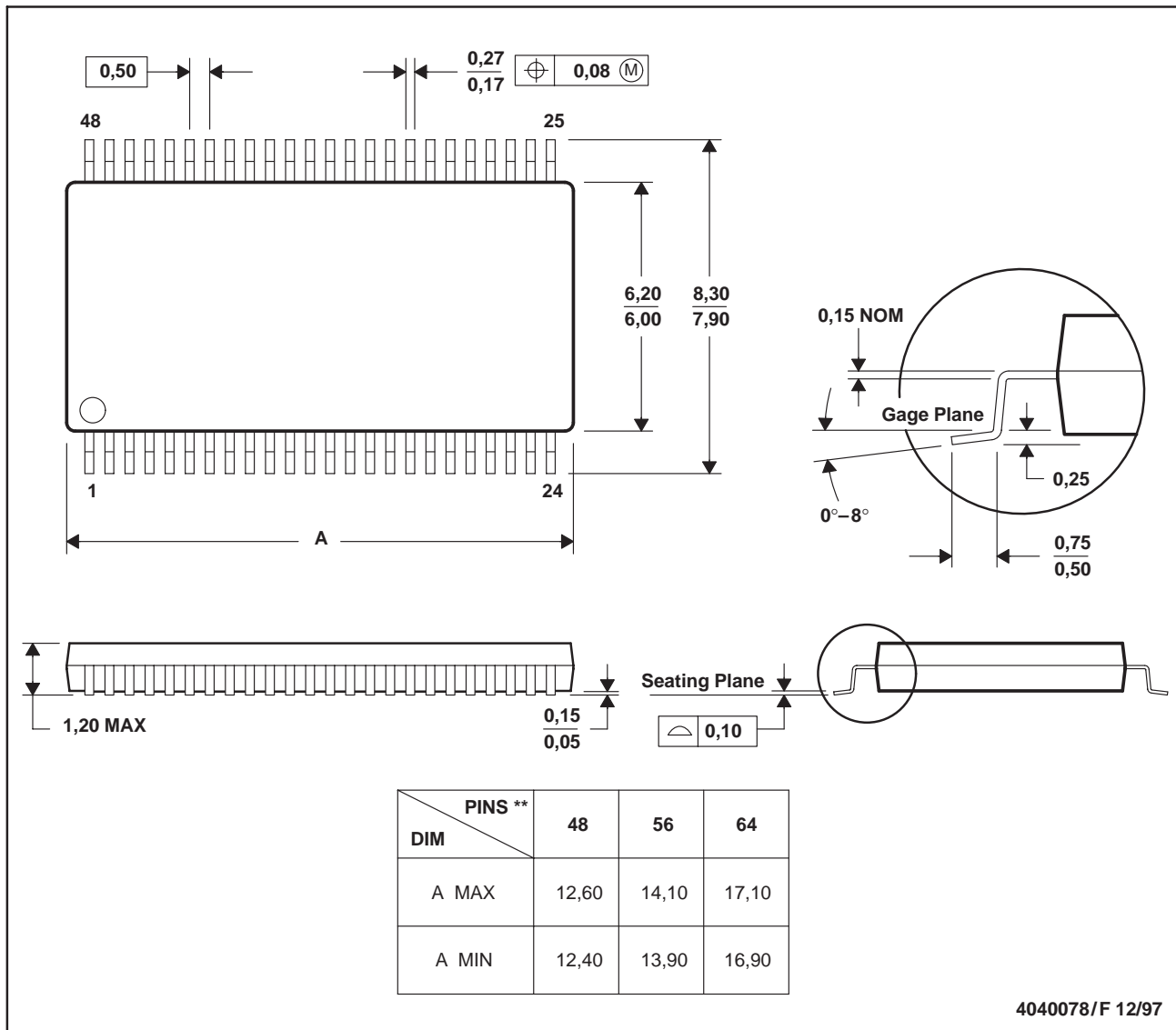
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC16240DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74AHC16240DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

**DGG (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold protrusion not to exceed 0,15.  
D. Falls within JEDEC MO-153



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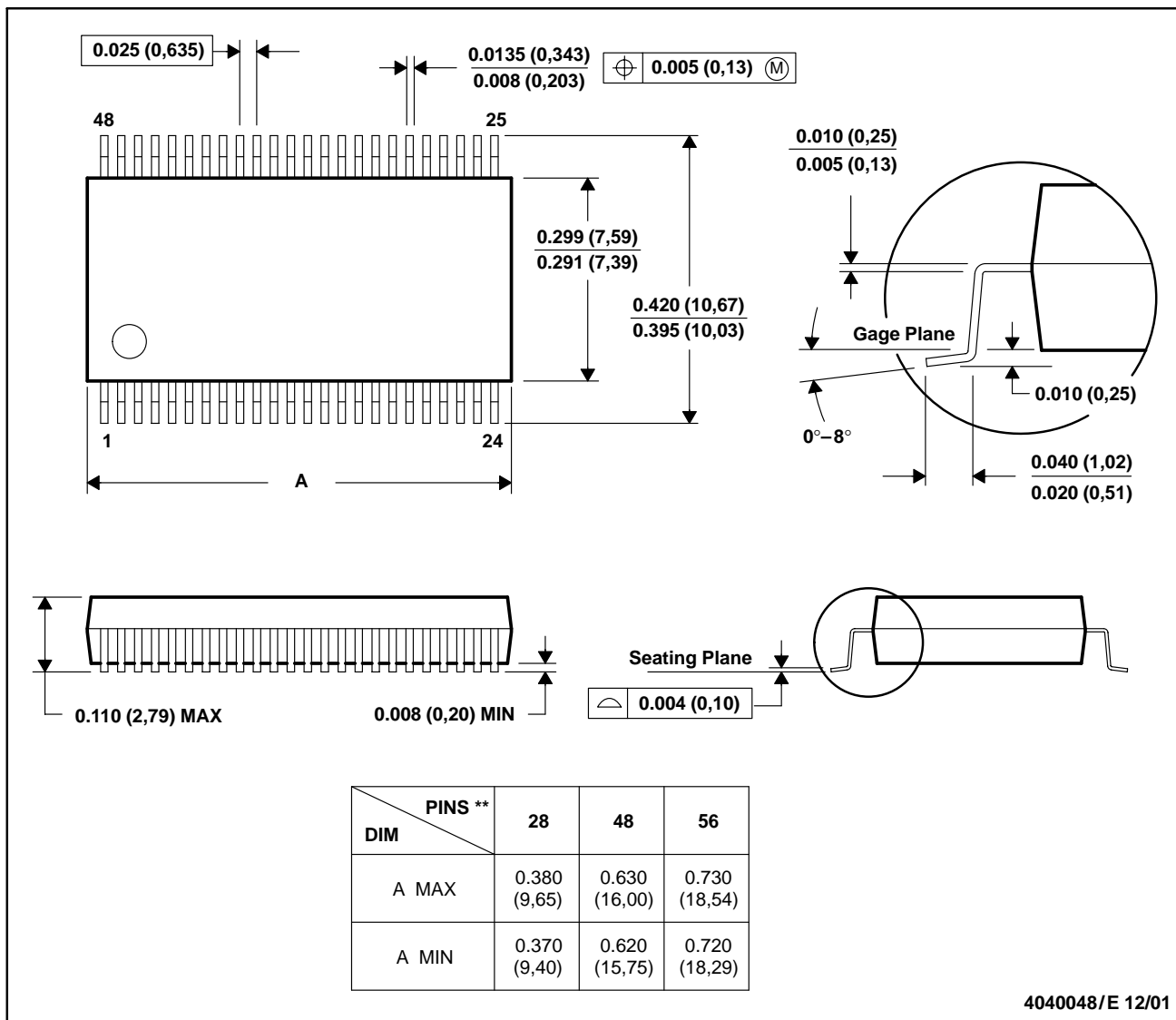
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MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

**DL (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MO-118



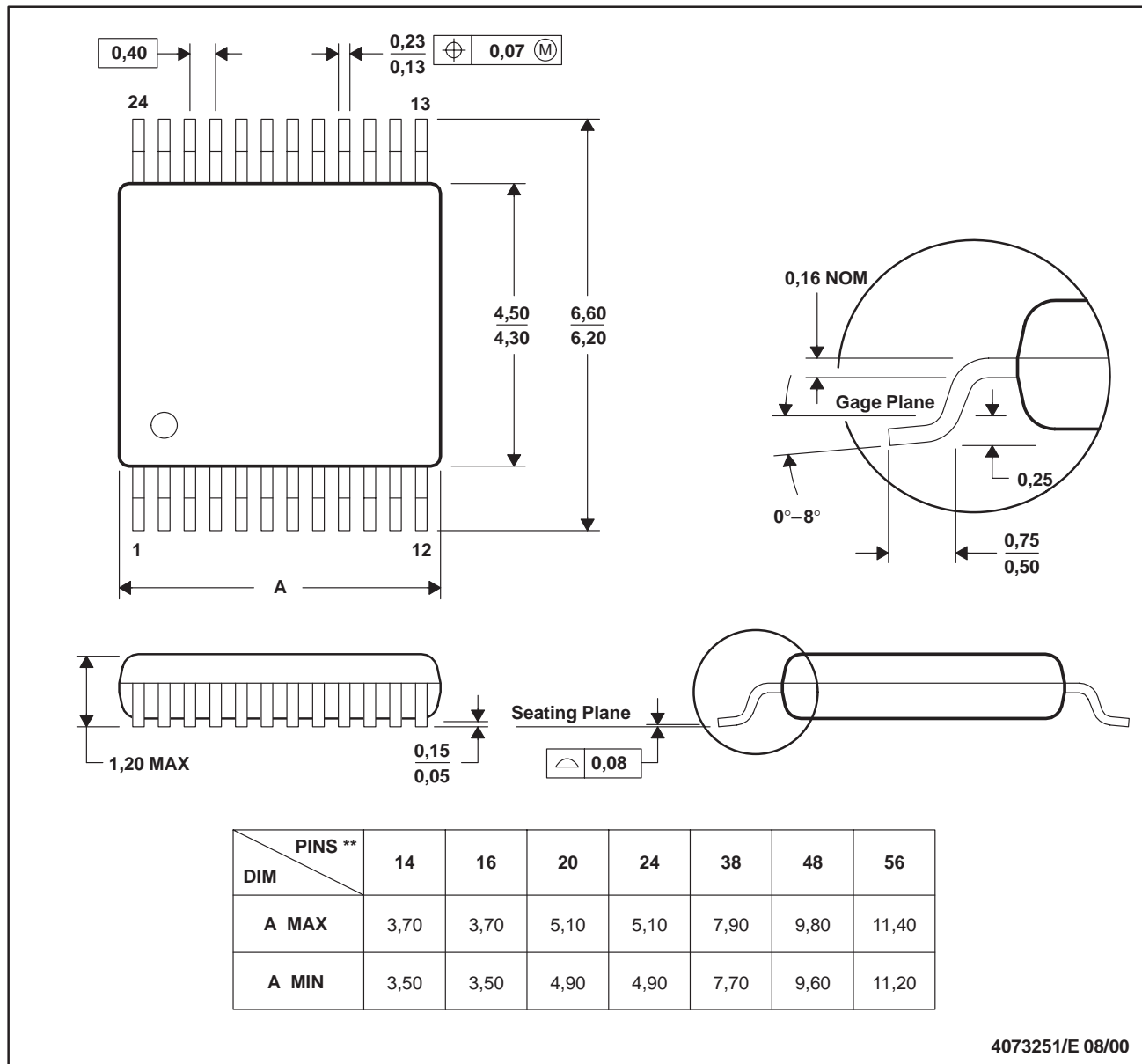
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**DGV (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



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