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SN54ABT827, SN74ABT827
10-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS159E – JANUARY 1991 – REVISED APRIL 2005

- State-of-the-Art **EPIC-II^B** BiCMOS Design Significantly Reduces Power Dissipation
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (-32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

description

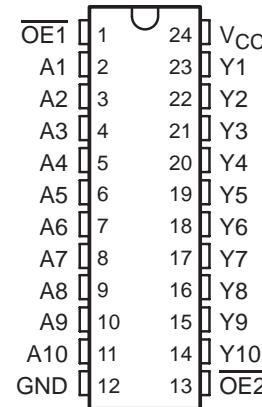
These 10-bit buffers or bus drivers provide a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable (\overline{OE}_1 or \overline{OE}_2) input is high, all ten outputs are in the high-impedance state. The 'ABT827 provides true data at the outputs.

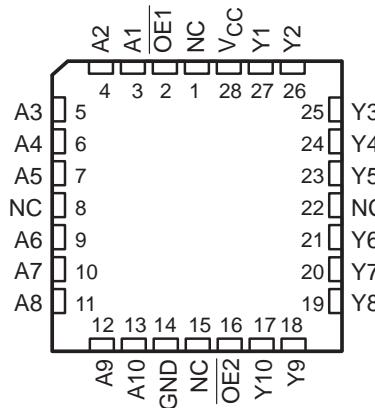
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT827 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT827 is characterized for operation from -40°C to 85°C .

SN54ABT827 . . . JT PACKAGE
SN74ABT827 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT827 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS			OUTPUT
\overline{OE}_1	\overline{OE}_2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-II^B is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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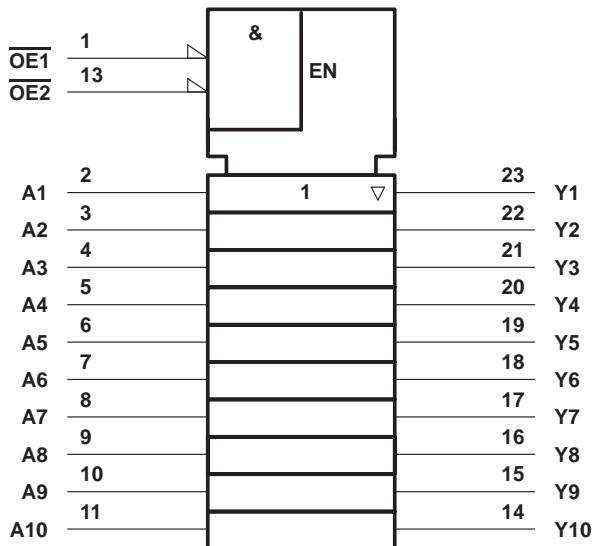
SN54ABT827, SN74ABT827

10-BIT BUFFERS/DRIVERS

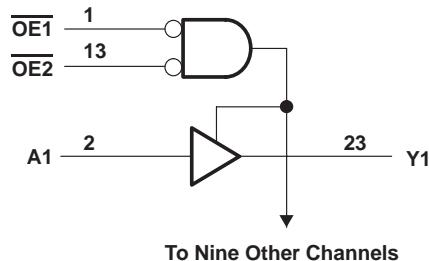
WITH 3-STATE OUTPUTS

SCBS159E – JANUARY 1991 – REVISED APRIL 2005

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT827	96 mA
SN74ABT827	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	104°C/W
DW package	81°C/W
NT package	67°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

SN54ABT827, SN74ABT827
10-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

		SN54ABT827		SN74ABT827		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage			0.8		V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current			-24		mA
I _{OL}	Low-level output current			48		mA
Δt/Δv	Input transition rise or fall rate			5		ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

SN54ABT827, SN74ABT827
10-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS159E – JANUARY 1991 – REVISED APRIL 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TA = 25°C			SN54ABT827		SN74ABT827		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
VIK	VCC = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
VOH	VCC = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
	VCC = 5 V, I _{OH} = -3 mA	3			3		3		
	VCC = 4.5 V, I _{OH} = -24 mA	2			2				
	I _{OH} = -32 mA	2*					2		
VOL	VCC = 4.5 V, I _{OL} = 48 mA		0.55		0.55				V
	I _{OL} = 64 mA		0.55*				0.55		
V _{hys}		100							mV
I _I	VCC = 0 to 5.5 V, V _I = VCC or GND		±1		±1		±1		µA
I _{OZPU} †	VCC = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, OE = X		±50		±10		±50		µA
I _{OZPD} †	VCC = 2.1 V to 0, V _O = 0.5 V to 2.7 V, OE = X		±50		±10		±50		µA
I _{OZH}	VCC = 2.1 V to 5.5 V, V _O = 2.7 V, OE ≥ 2 V		10§		10		10§		µA
I _{OZL}	VCC = 2.1 V to 5.5 V, V _O = 0.5 V, OE ≥ 2 V		-10§		-10		-10§		µA
I _{off}	VCC = 0, V _I or V _O ≤ 5.5 V		±100				±100		µA
I _{CEX}	VCC = 5.5 V, V _O = 5.5 V	Outputs high		50		50		50	µA
I _{O¶}	VCC = 5.5 V, V _O = 2.5 V	-50 -140 -225§			-50 -225§		-50 -225§		mA
I _{CC}	VCC = 5.5 V, I _O = 0, V _I = VCC or GND	Outputs high	80	250		250		250	µA
		Outputs low	35	40§		40§		40§	mA
		Outputs disabled	80	250		250		250	µA
ΔI _{CC} #	VCC = 5.5 V, One input at 3.4 V, Other inputs at VCC or GND	Outputs enabled		1.5		1.5		1.5	mA
		Outputs disabled		50		50		50	µA
		Control inputs		1.5		1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V		4						pF
C _o	V _O = 2.5 V or 0.5 V		8						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at VCC = 5 V.

‡ This parameter is characterized, but not production tested.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level, rather than VCC or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, CL = 50 pF (unless otherwise noted) (see Figure 1)

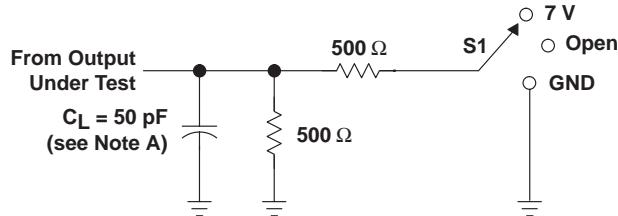
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 5 V, TA = 25°C			SN54ABT827		SN74ABT827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH			1.1	2.6	4.4	1.1	4.9	1.1	4.8	
tPHL	A	Y	1.1	2.3	4.1	1.1	4.8	1.1	4.7	ns
tpZH			1§	3.2	5.1	1	6	1§	5.9	
tpZL			1§	3.3	5.9	1	7.1	1§	6.9	ns
tPHZ			2	4.9	6.3	2	7	2	6.8	
tPLZ	OE	Y	1.3§	4.2	6.6	1.3	7.9	1.3§	6.9	ns

§ This data sheet limit may vary among suppliers.



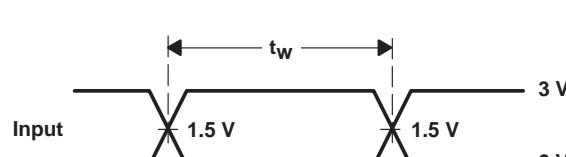
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PARAMETER MEASUREMENT INFORMATION

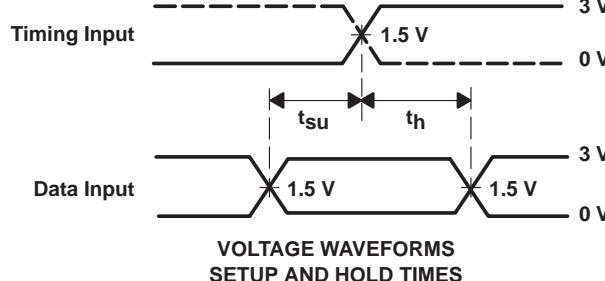


TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	7 V
t _{PHZ} /t _{PZH}	Open

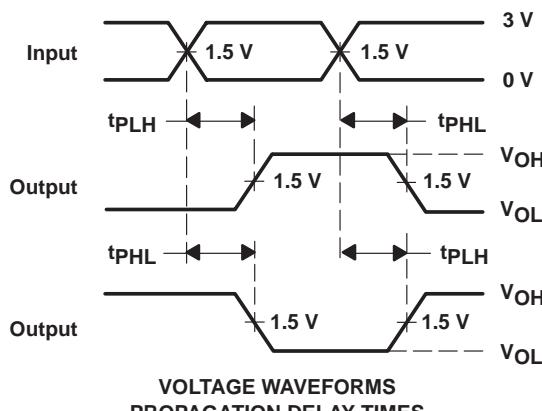
LOAD CIRCUIT



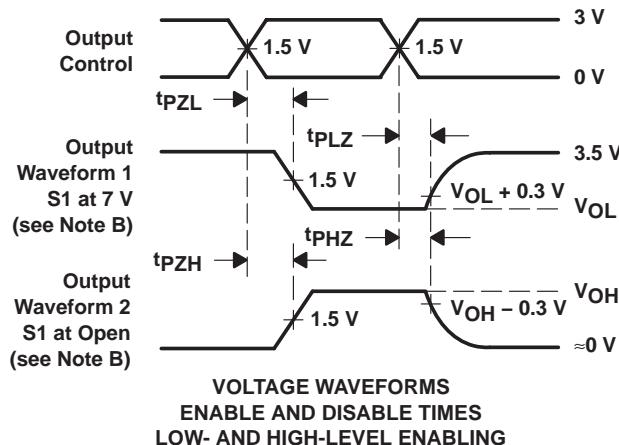
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9450901QKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9450901QK A SNJ54ABT827W	Samples
5962-9450901QLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9450901QL A SNJ54ABT827JT	Samples
SN74ABT827DBLE	OBsolete	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		
SN74ABT827DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827	Samples
SN74ABT827DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT827	Samples
SN74ABT827DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT827	Samples
SN74ABT827PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827	Samples
SN74ABT827PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827	Samples
SN74ABT827PWLE	OBsolete	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
SN74ABT827PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827	Samples
SNJ54ABT827JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9450901QL A SNJ54ABT827JT	Samples
SNJ54ABT827W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9450901QK A SNJ54ABT827W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ABT827, SN74ABT827 :

• Catalog: [SN74ABT827](#)

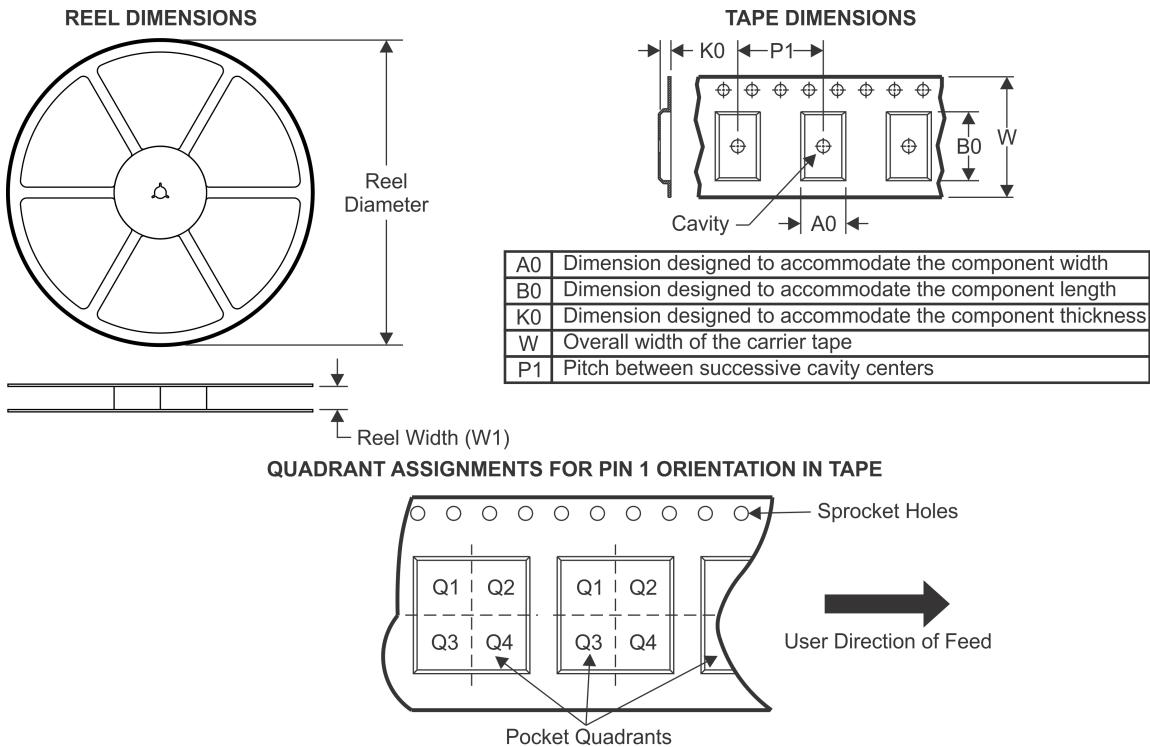
• Military: [SN54ABT827](#)

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

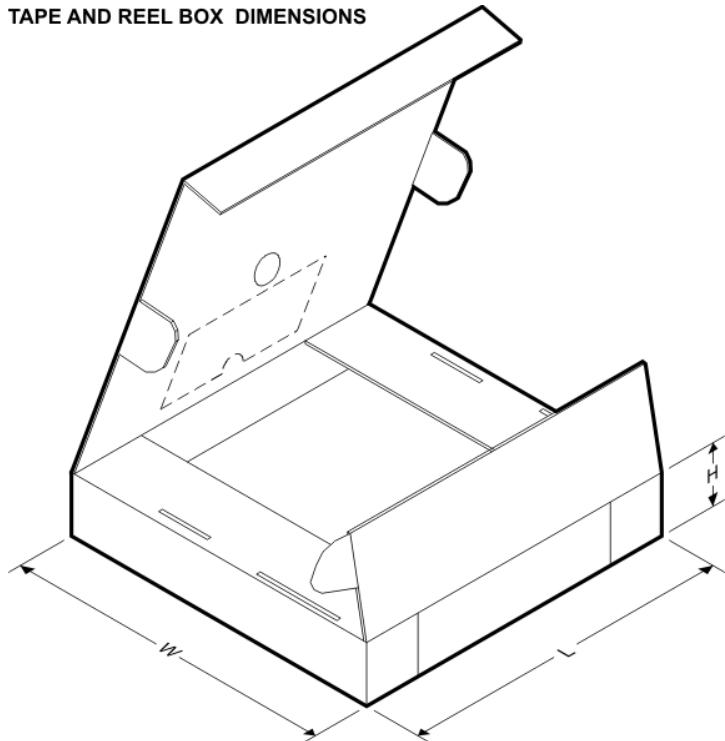
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT827DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT827DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABT827PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

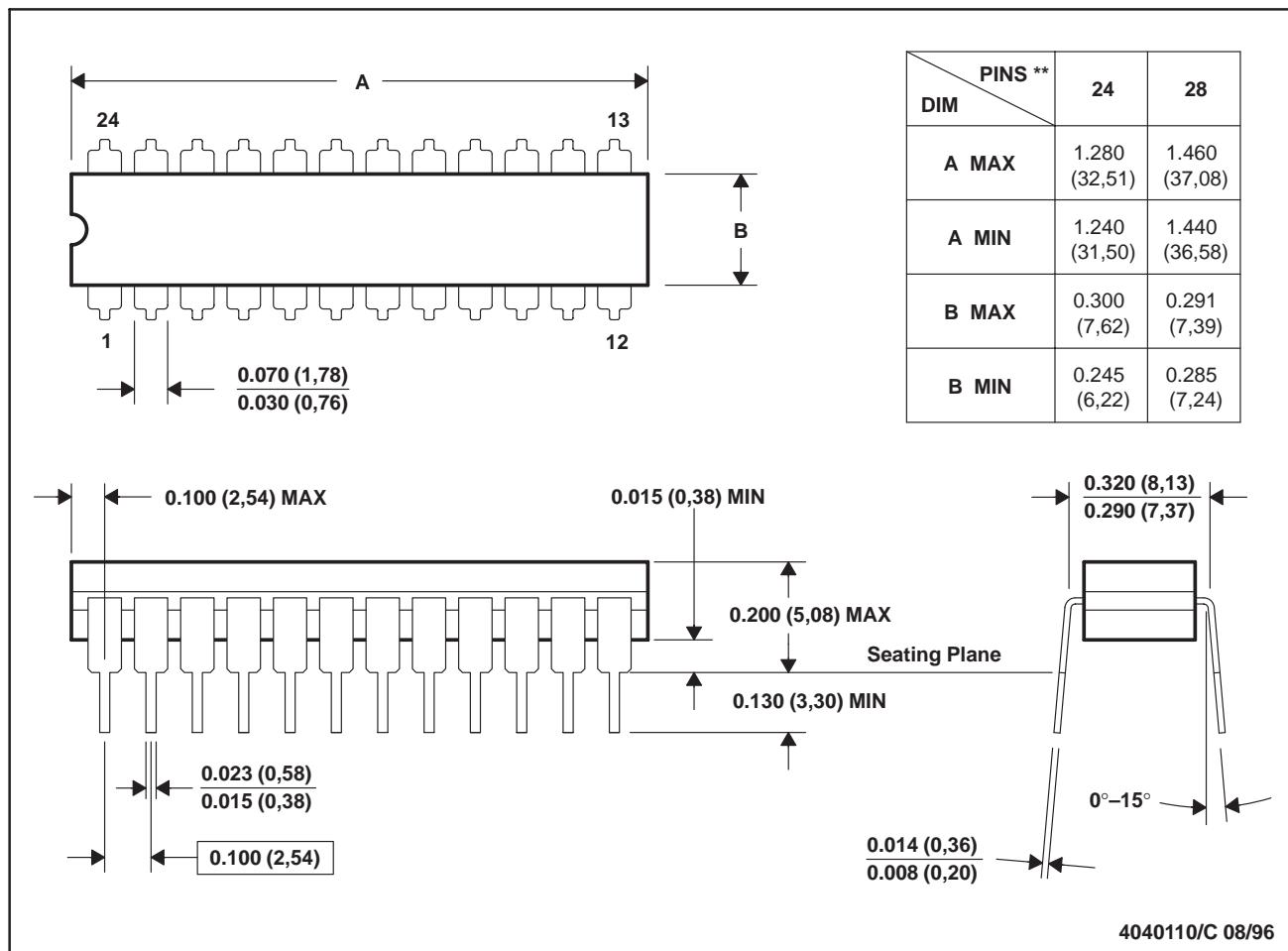
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT827DBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74ABT827DWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74ABT827PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

JT (R-GDIP-T)**

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE

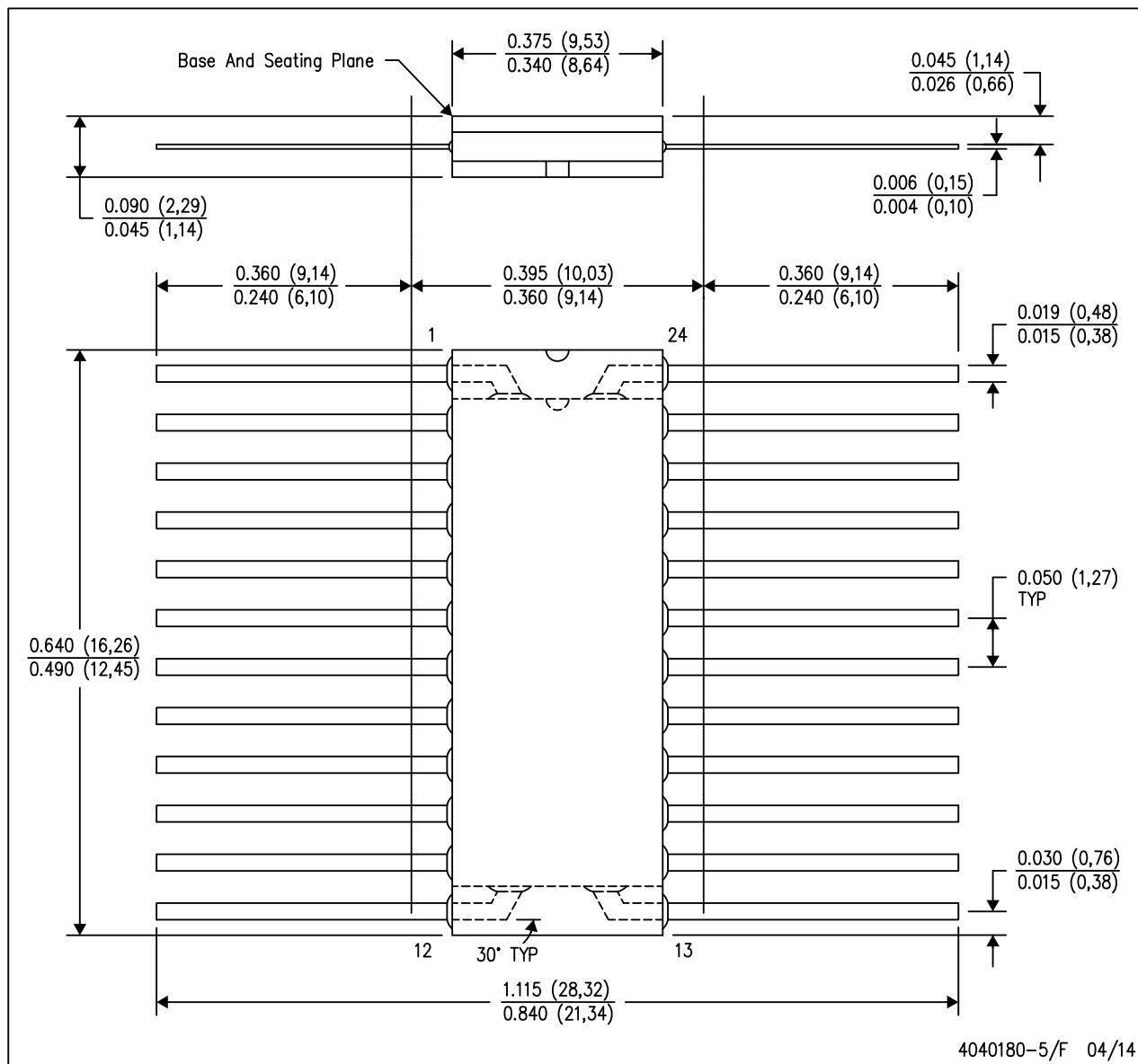


NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

MECHANICAL DATA

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



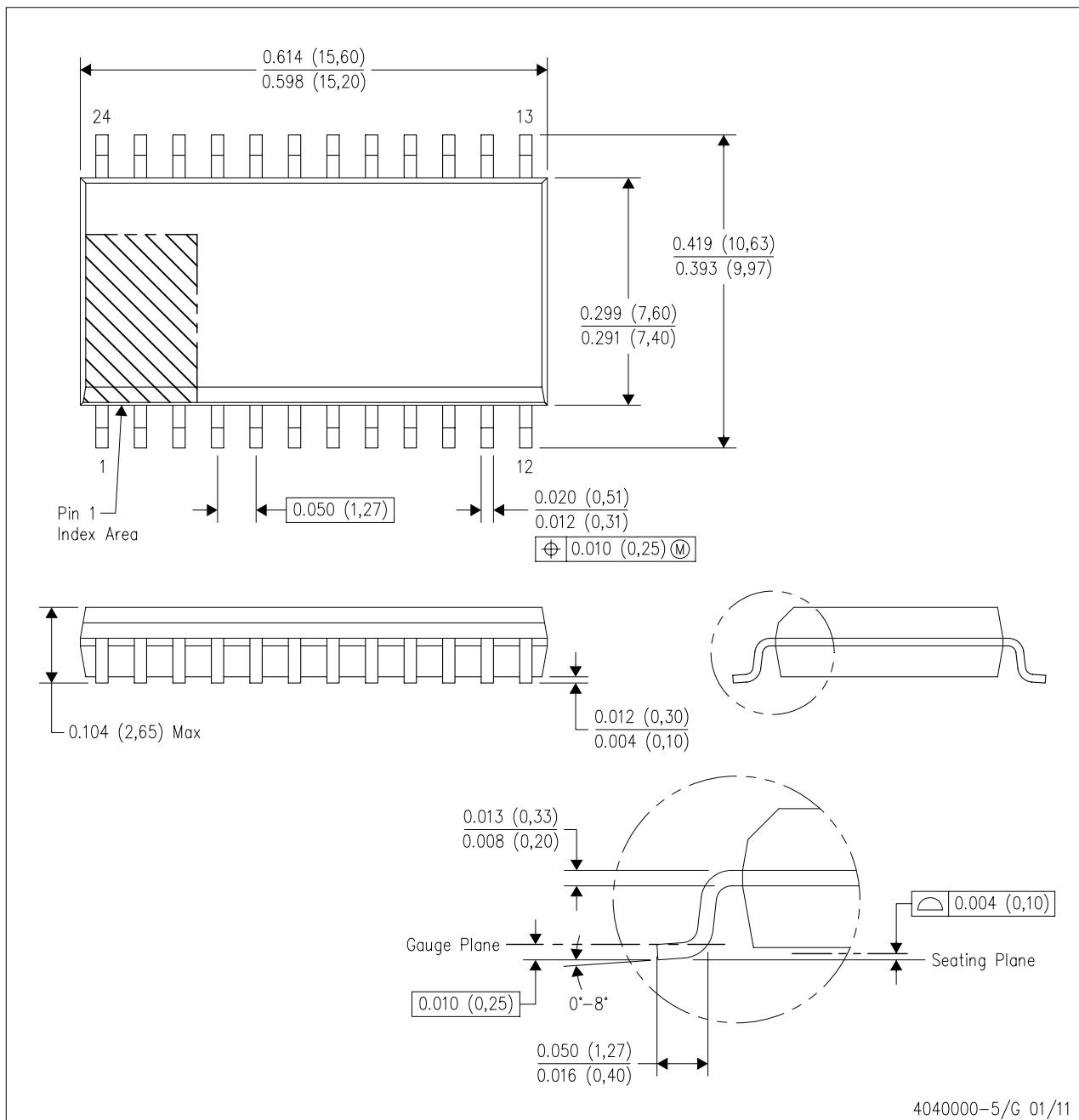
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

MECHANICAL DATA

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



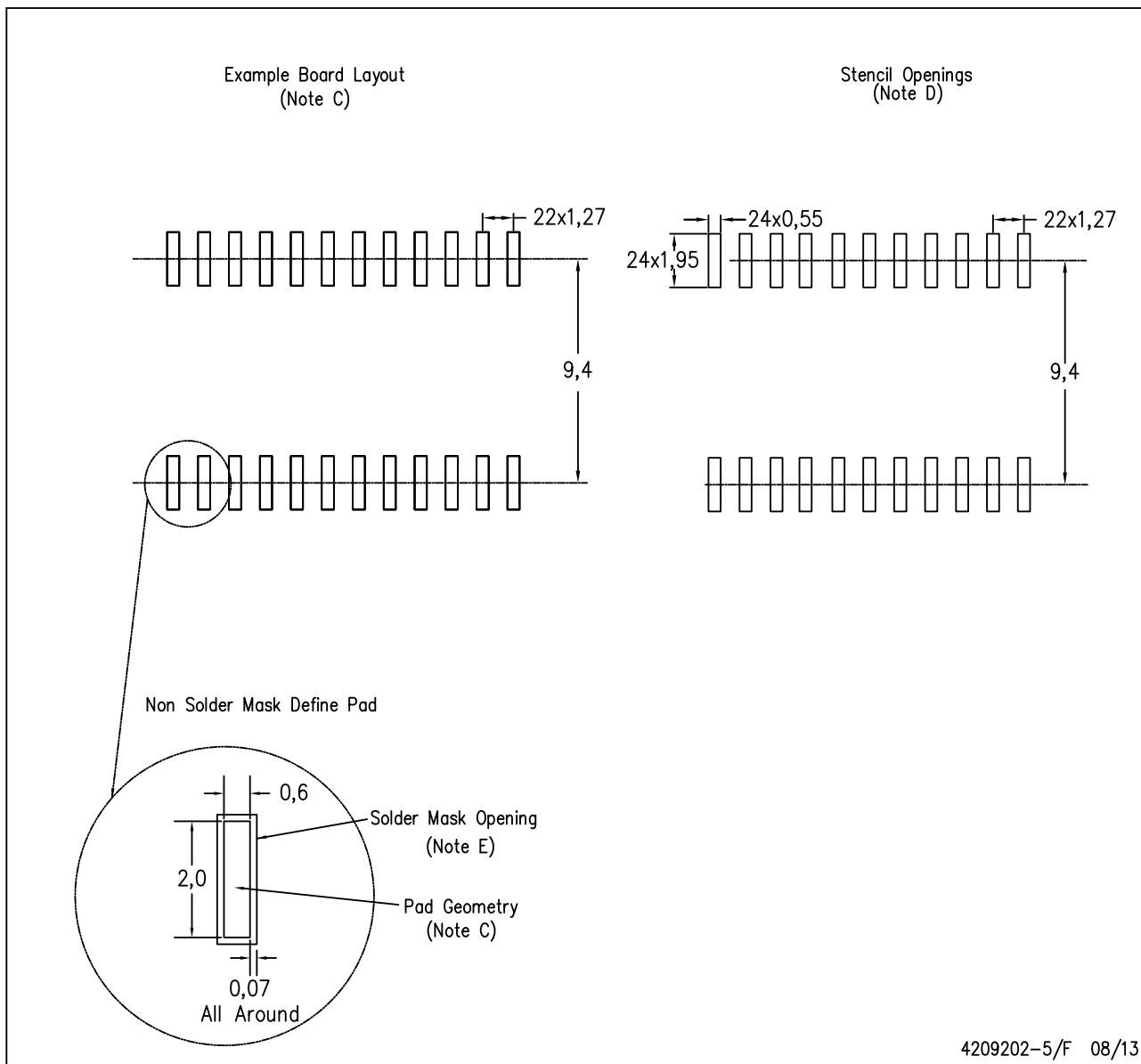
NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-013 variation AD.

LAND PATTERN DATA

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



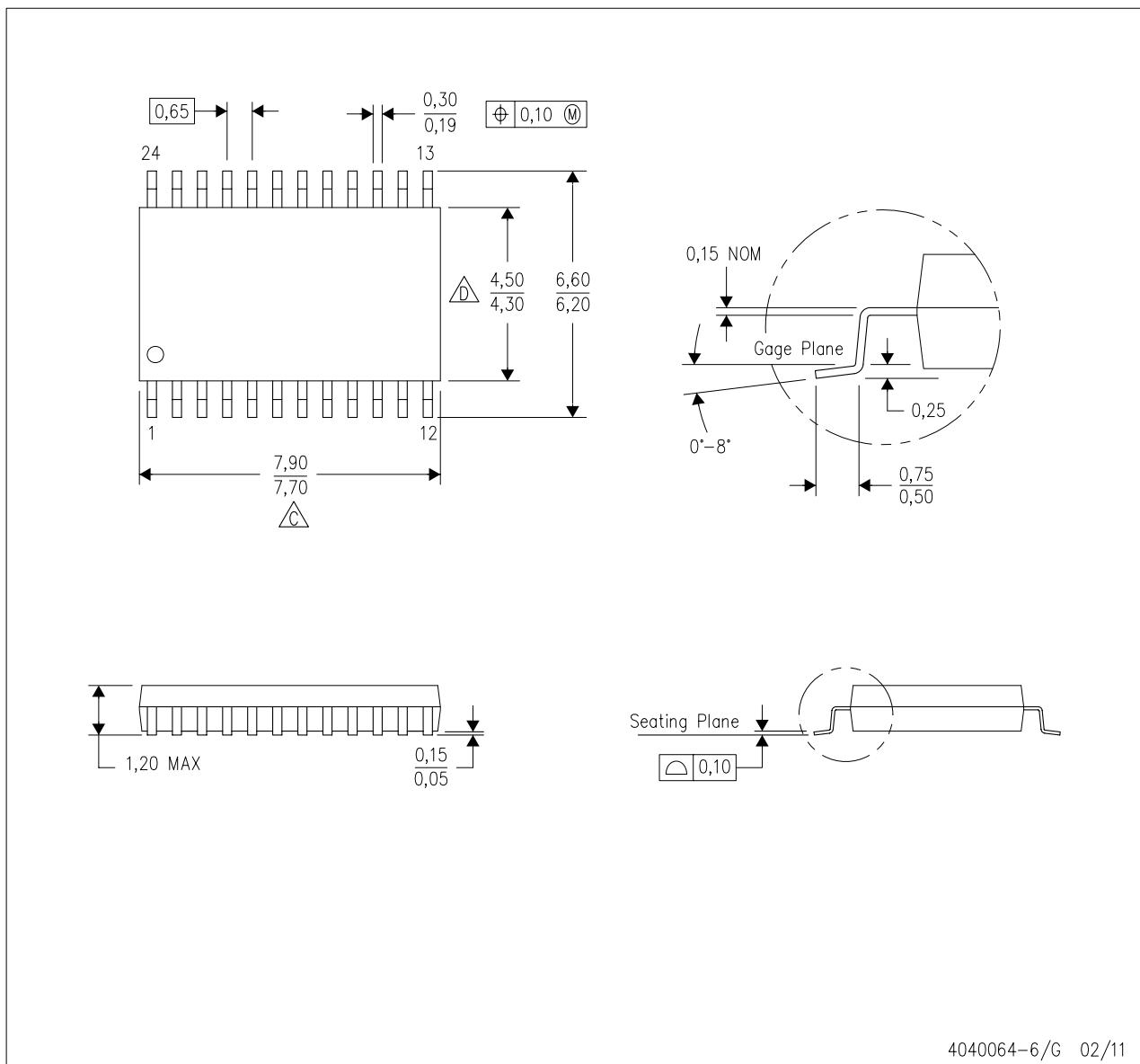
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4040064-6/G 02/11

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
-  C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
-  D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

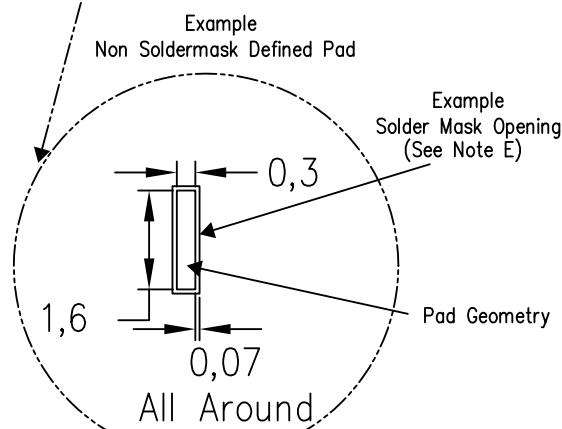
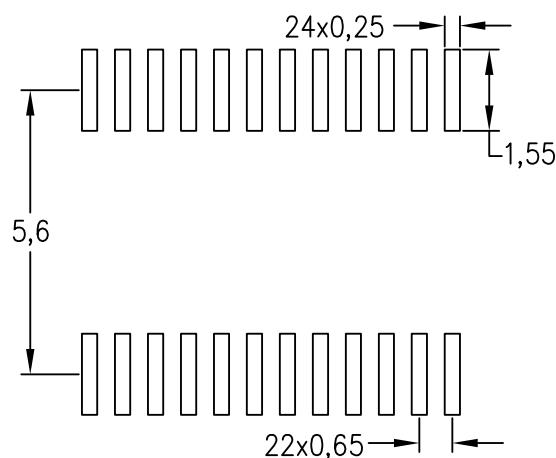
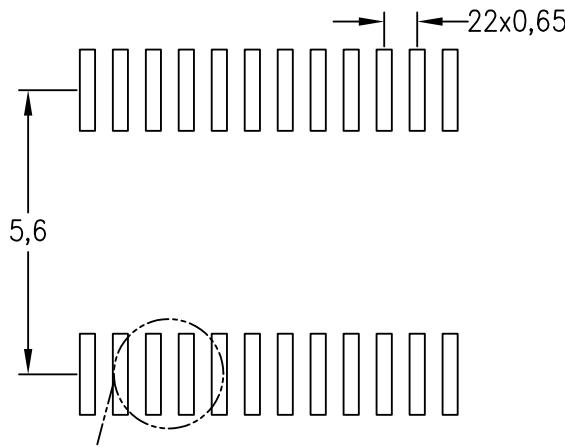
LAND PATTERN DATA

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4211284-4/G 08/15

NOTES:

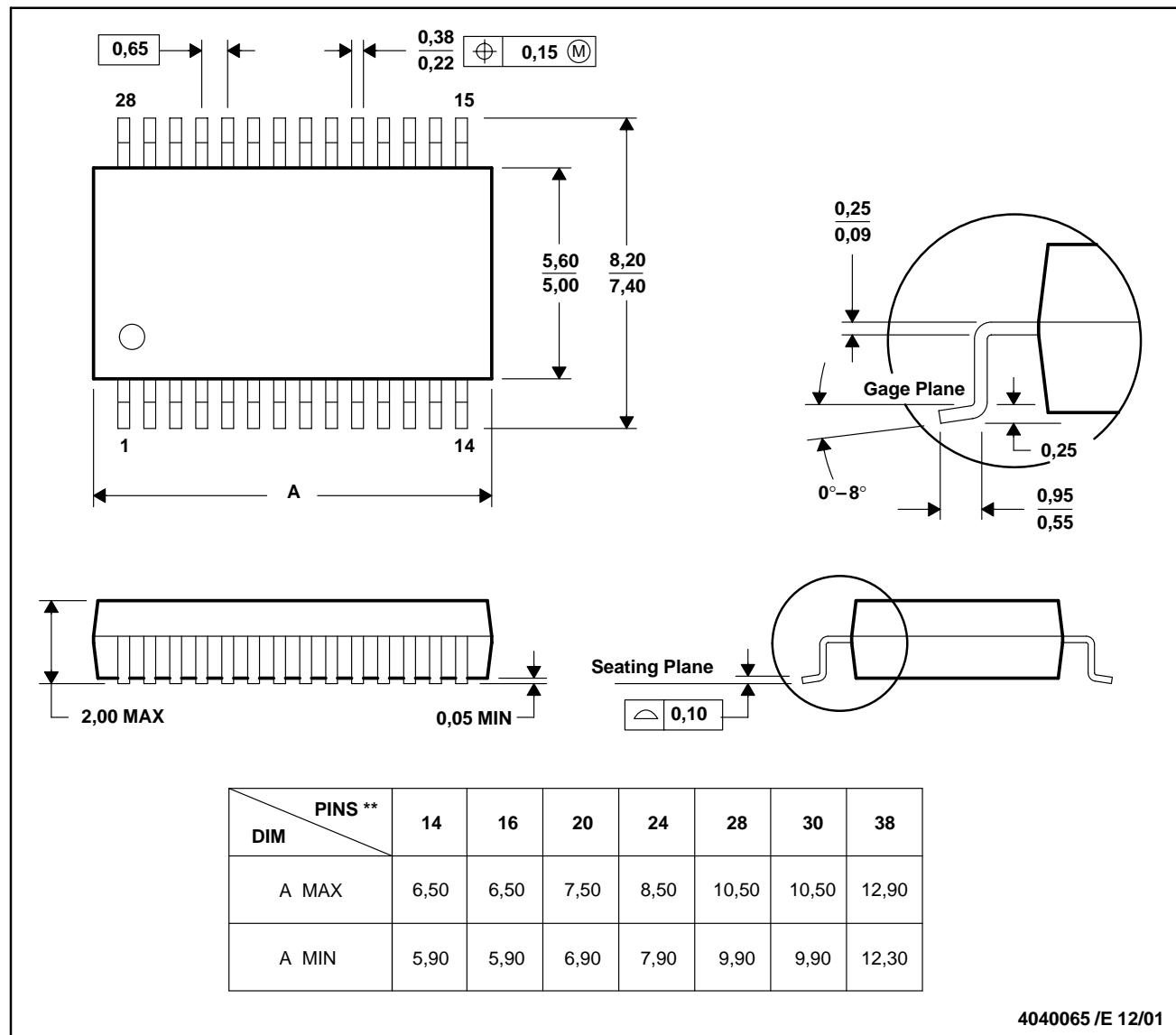
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSS002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)**

28 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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