

## Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Texas Instruments](#)

[SN74ACT7806-20DL](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

**SN74ACT7806**

**256 × 18**

**STROBED FIRST-IN, FIRST-OUT MEMORY**

SCAS438C – APRIL 1992 – REVISED APRIL 1998

- **Member of the Texas Instruments Widebus™ Family**
- **Load Clock and Unload Clock Can Be Asynchronous or Coincident**
- **256 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates up to 50 MHz**
- **3-State Outputs**
- **Pin-to-Pin Compatible With SN74ACT7804 and SN74ACT7814**
- **Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Spacing**

**description**

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7806 is a 256-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 256. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ( $\overline{\text{FULL}}$ ), empty ( $\overline{\text{EMPTY}}$ ), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The FULL output is low when the memory is full and high when the memory is not full. The EMPTY output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 128 or more words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ( $\overline{\text{PEN}}$ ) is low. The AF/AE flag is high when the FIFO contains X or fewer words or (256 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (255 – Y) words.

DL PACKAGE (TOP VIEW)			
$\overline{\text{RESET}}$	1	56	$\overline{\text{OE}}$
D17	2	55	Q17
D16	3	54	Q16
D15	4	53	Q15
D14	5	52	GND
D13	6	51	Q14
D12	7	50	V <sub>CC</sub>
D11	8	49	Q13
D10	9	48	Q12
V <sub>CC</sub>	10	47	Q11
D9	11	46	Q10
D8	12	45	Q9
GND	13	44	GND
D7	14	43	Q8
D6	15	42	Q7
D5	16	41	Q6
D4	17	40	Q5
D3	18	39	V <sub>CC</sub>
D2	19	38	Q4
D1	20	37	Q3
D0	21	36	Q2
HF	22	35	GND
$\overline{\text{PEN}}$	23	34	Q1
AF/AE	24	33	Q0
LDCK	25	32	UNCK
NC	26	31	NC
NC	27	30	NC
FULL	28	29	EMPTY

NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

## SN74ACT7806

256 × 18

### STROBED FIRST-IN, FIRST-OUT MEMORY

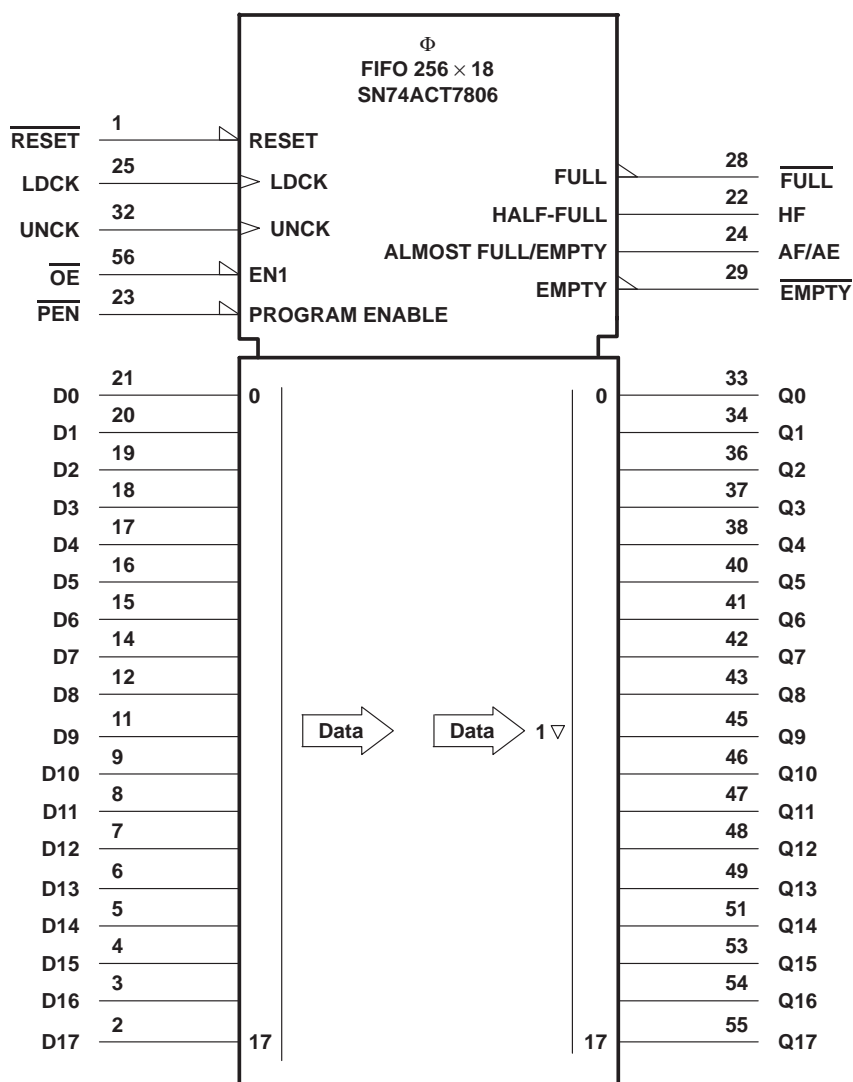
SCAS438C – APRIL 1992 – REVISED APRIL 1998

#### description (continued)

A low level on the reset ( $\overline{\text{RESET}}$ ) input resets the internal stack pointers and sets  $\overline{\text{FULL}}$  high, HF low, and  $\overline{\text{EMPTY}}$  low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The first word loaded into empty memory causes  $\overline{\text{EMPTY}}$  to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ( $\overline{\text{OE}}$ ) input is high.

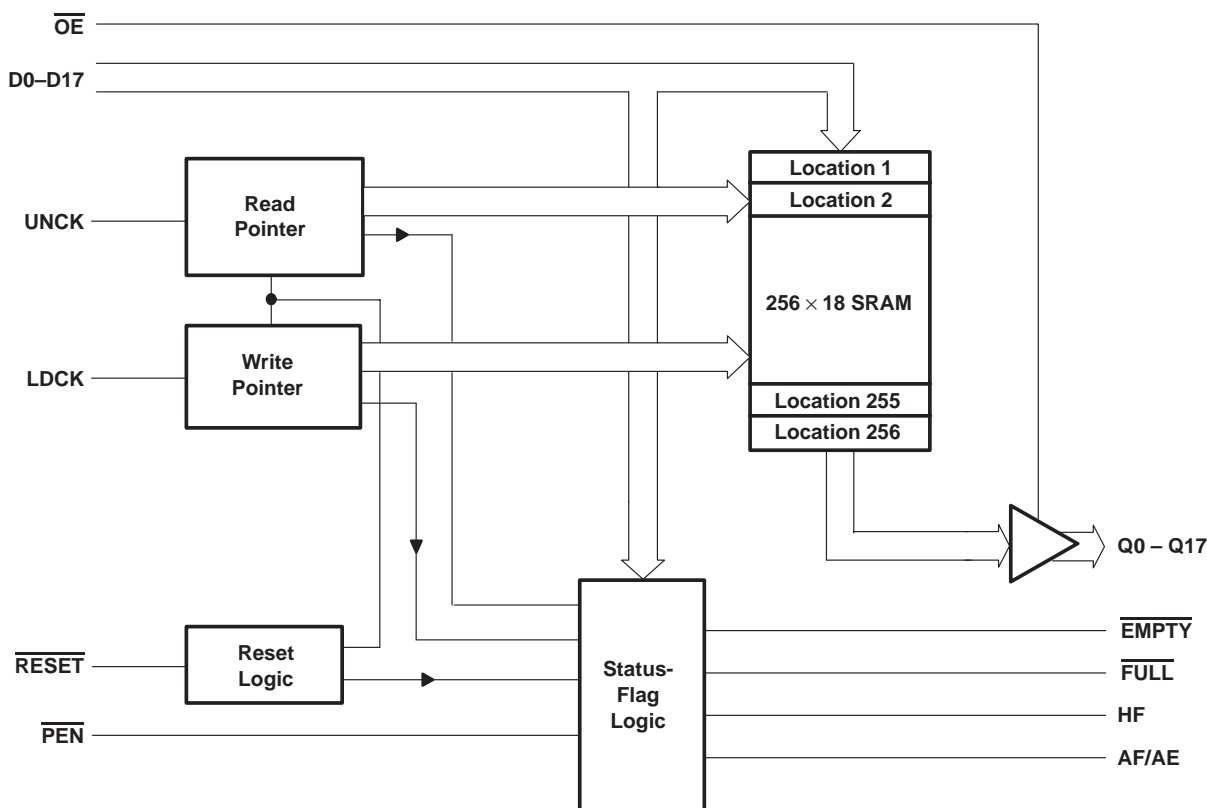
The SN74ACT7806 is characterized for operation from 0°C to 70°C.

#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**functional block diagram**



**Terminal Functions**

TERMINAL NAME	NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth-offset values can be programmed for AF/AE, or the default value of 32 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or fewer words or (256 – Y) or more words. AF/AE is high after reset.
D0–D17	2–9, 11–12, 12–14	I	18-bit data input port
$\overline{\text{EMPTY}}$	29	O	Empty flag. $\overline{\text{EMPTY}}$ is high when the FIFO memory is not empty; $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty or upon assertion of $\overline{\text{RESET}}$ .
$\overline{\text{FULL}}$	28	O	Full flag. $\overline{\text{FULL}}$ is high when the FIFO memory is not full or upon assertion of $\overline{\text{RESET}}$ ; $\overline{\text{FULL}}$ is low when the FIFO memory is full.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 128 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
$\overline{\text{OE}}$	56	I	Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D6 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on this input resets the FIFO and drives $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.

## SN74ACT7806

256 × 18

### STROBED FIRST-IN, FIRST-OUT MEMORY

SCAS438C – APRIL 1992 – REVISED APRIL 1998

#### offset values for AF/AE

The AF/AE flag has two programmable limits, the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or fewer words or (256 – Y) or more words.

To program the offset values,  $\overline{\text{PEN}}$  can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D6 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding  $\overline{\text{PEN}}$  low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D6 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 127 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 32,  $\overline{\text{PEN}}$  must be held high.

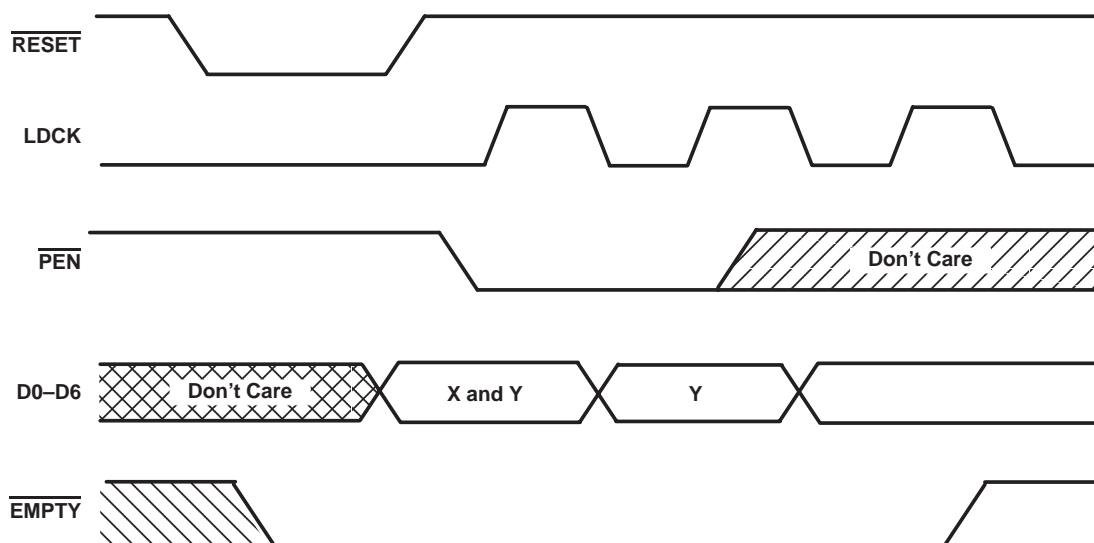


Figure 1. Programming X and Y Separately

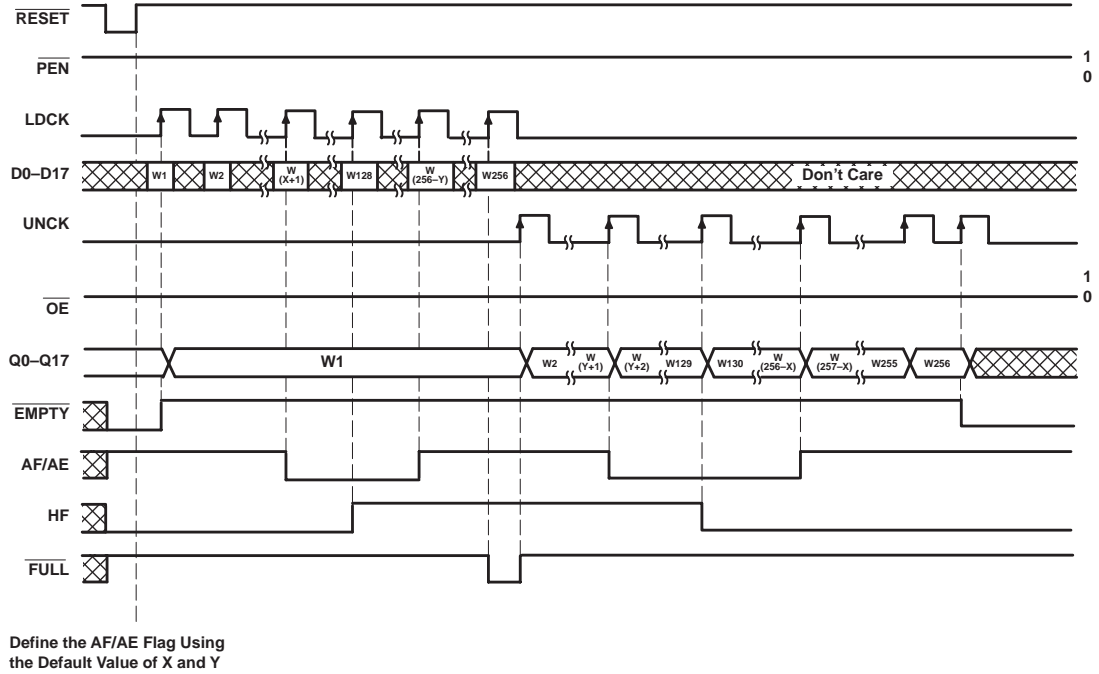


Figure 2. Write, Read, and Flag Timing Reference

# SN74ACT7806

256 × 18

## STROBED FIRST-IN, FIRST-OUT MEMORY

SCAS438C – APRIL 1992 – REVISED APRIL 1998

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$	–0.5 V to 7 V
Voltage range applied to a disabled 3-state output	–0.5 V to 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1)	74°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions

		'ACT7806-20		'ACT7806-25		'ACT7806-40		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8		0.8	V
$I_{OH}$	High-level output current		–8		–8		–8	mA
$I_{OL}$	Low-level output current		16		16		16	mA
	Flags		8		8		8	
$T_A$	Operating free-air temperature	0	70	0	70	0	70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -8\text{ mA}$	2.4			V
$V_{OL}$	Flags	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 8\text{ mA}$			0.5	V
	Q outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 16\text{ mA}$			0.5	
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = V_{CC}$ or 0			±5	μA
$I_{OZ}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = V_{CC}$ or 0			±5	μA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = V_{CC} - 0.2\text{ V}$ or 0			400	μA
$\Delta I_{CC}^{\S}$	$V_{CC} = 5.5\text{ V}$ ,	One input at 3.4 V, Other inputs at $V_{CC}$ or GND			1	mA
$C_i$	$V_I = 0$ ,	$f = 1\text{ MHz}$		4		pF
$C_o$	$V_O = 0$ ,	$f = 1\text{ MHz}$		8		pF

<sup>‡</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>\S</sup> This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

**SN74ACT7806**

**256 × 18**

**STROBED FIRST-IN, FIRST-OUT MEMORY**

SCAS438C – APRIL 1992 – REVISED APRIL 1998

**timing requirements over recommended operating conditions (see Figures 1 through 3)**

			'ACT7806-20		'ACT7806-25		'ACT7806-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		50		40		25		MHz
t <sub>w</sub>	Pulse duration	LDCK high or low	7		8		12		ns
		UNCK high or low	7		8		12		
		$\overline{\text{PEN}}$ low	7		8		12		
		$\overline{\text{RESET}}$ low	10		10		12		
t <sub>su</sub>	Setup time	D0–D17 before LDCK↑	5		5		5		ns
		$\overline{\text{PEN}}$ before LDCK↑	5		5		5		
		LDCK inactive before $\overline{\text{RESET}}$ high	5		6		6		
t <sub>h</sub>	Hold time	D0–D17 after LDCK↑	0		0		0		ns
		LDCK inactive after $\overline{\text{RESET}}$ high	5		6		6		
		$\overline{\text{PEN}}$ low after LDCK↑	3		3		3		
		$\overline{\text{PEN}}$ high after LDCK↓	0		0		0		

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figures 5 and 6)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7806-20			'ACT7806-25		'ACT7806-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$	LDCK or UNCK		50			40		25		MHz
$t_{\text{pd}}$	LDCK $\uparrow$	Any Q	9		20	9	22	9	24	ns
	UNCK $\uparrow$		6	11.5	15	6	18	6	20	
$t_{\text{pd}}^\ddagger$	UNCK $\uparrow$	Any Q	10.5							ns
$t_{\text{PLH}}$	LDCK $\uparrow$	$\overline{\text{EMPTY}}$	6		15	6	17	6	19	ns
$t_{\text{PHL}}$	UNCK $\uparrow$	$\overline{\text{EMPTY}}$	6		15	6	17	6	19	ns
	$\overline{\text{RESET}}$ low		4		16	4	18	4	20	
	LDCK $\uparrow$	$\overline{\text{FULL}}$	6		15	6	17	6	19	
$t_{\text{PLH}}$	UNCK $\uparrow$	$\overline{\text{FULL}}$	6		15	6	17	6	19	ns
	$\overline{\text{RESET}}$ low		4		18	4	20	4	22	
$t_{\text{pd}}$	LDCK $\uparrow$	AF/AE	7		18	7	20	7	22	ns
	UNCK $\uparrow$		7		18	7	20	7	22	
$t_{\text{PLH}}$	$\overline{\text{RESET}}$ low	AF/AE	2		10	2	12	2	14	ns
	LDCK $\uparrow$	HF	5		18	5	20	5	22	
$t_{\text{PHL}}$	UNCK $\uparrow$	HF	7		18	7	20	7	22	ns
	$\overline{\text{RESET}}$ low		3		12	3	14	3	16	
$t_{\text{en}}$	$\overline{\text{OE}}$	Any Q	2		9	2	10	2	11	ns
$t_{\text{dis}}$	$\overline{\text{OE}}$	Any Q	2		10	2	11	2	12	ns

† All typical values are at  $V_{\text{CC}} = 5$  V,  $T_A = 25^\circ\text{C}$ .

‡ This parameter is measured at  $C_L = 30$  pF (see Figure 4).

**operating characteristics,  $V_{\text{CC}} = 5$  V,  $T_A = 25^\circ\text{C}$**

PARAMETER			TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance per FIFO channel	Outputs enabled	$C_L = 50$ pF, $f = 5$ MHz	53	pF



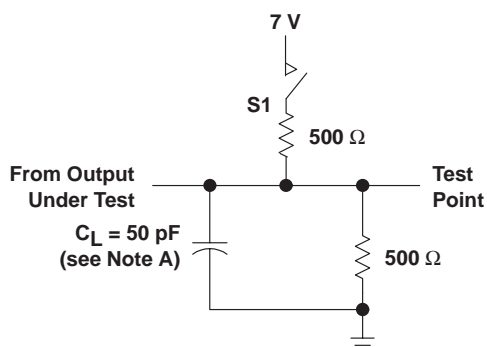
# SN74ACT7806

256 × 18

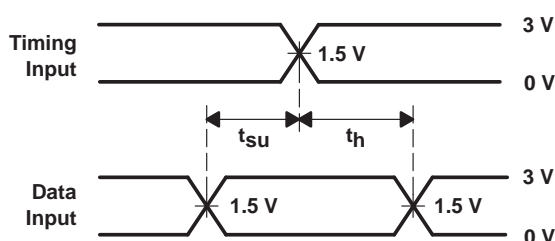
## STROBED FIRST-IN, FIRST-OUT MEMORY

SCAS438C – APRIL 1992 – REVISED APRIL 1998

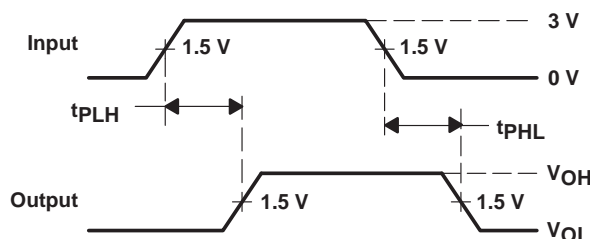
### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

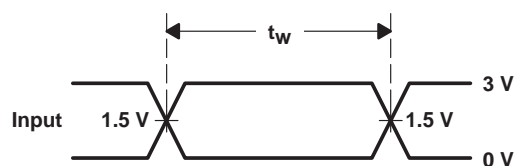


VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES

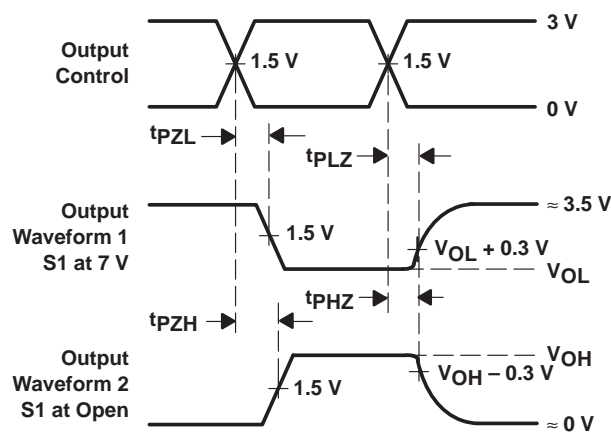


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

PARAMETER		S1
$t_{en}$	$t_{PZH}$	Open
	$t_{PZL}$	Closed
$t_{dis}$	$t_{PHZ}$	Open
	$t_{PLZ}$	Closed
$t_{pd}$	$t_{PLH}$	Open
	$t_{PHL}$	Open



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 3. Load Circuit and Voltage Waveforms

**SN74ACT7806**

**256 × 18**

**STROBED FIRST-IN, FIRST-OUT MEMORY**

SCAS438C – APRIL 1992 – REVISED APRIL 1998

## TYPICAL CHARACTERISTICS

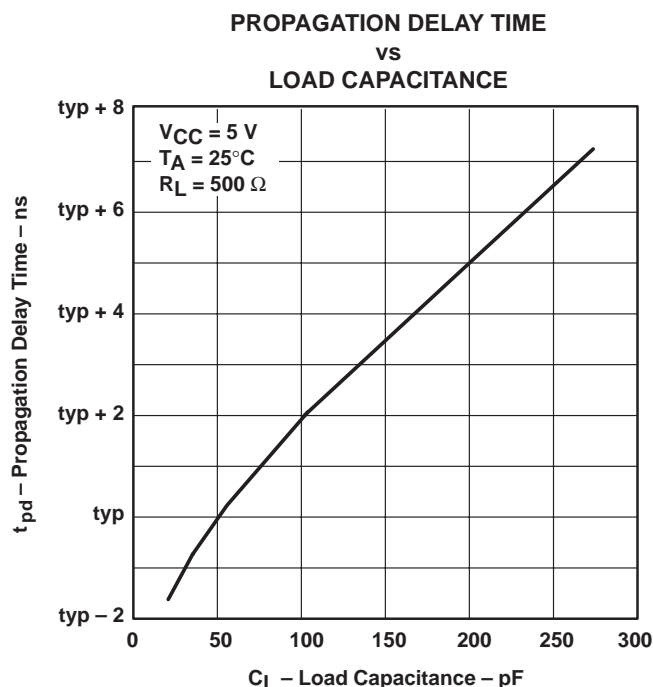


Figure 4

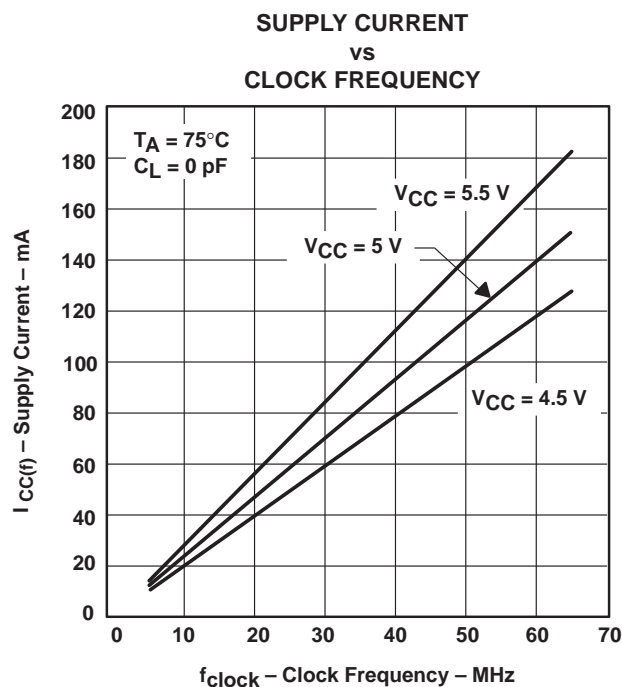


Figure 5

## APPLICATION INFORMATION

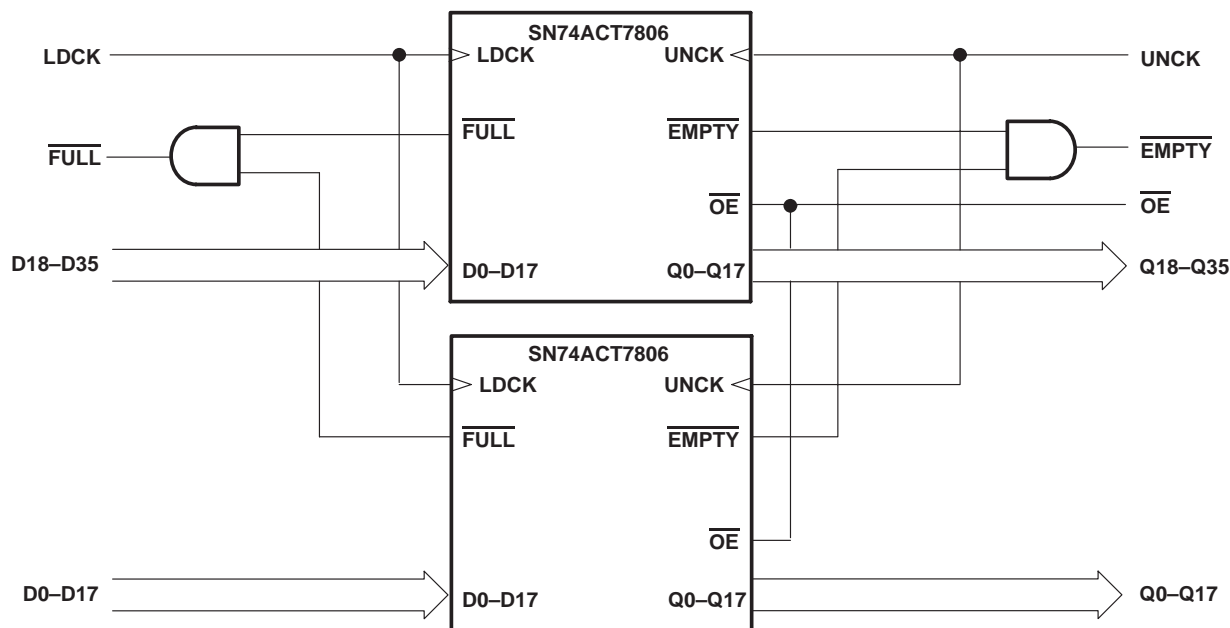


Figure 6. Word-Width Expansion: 256 × 36 Bits



**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
1M7806-40DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT7806-20DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT7806-25DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT7806-40DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

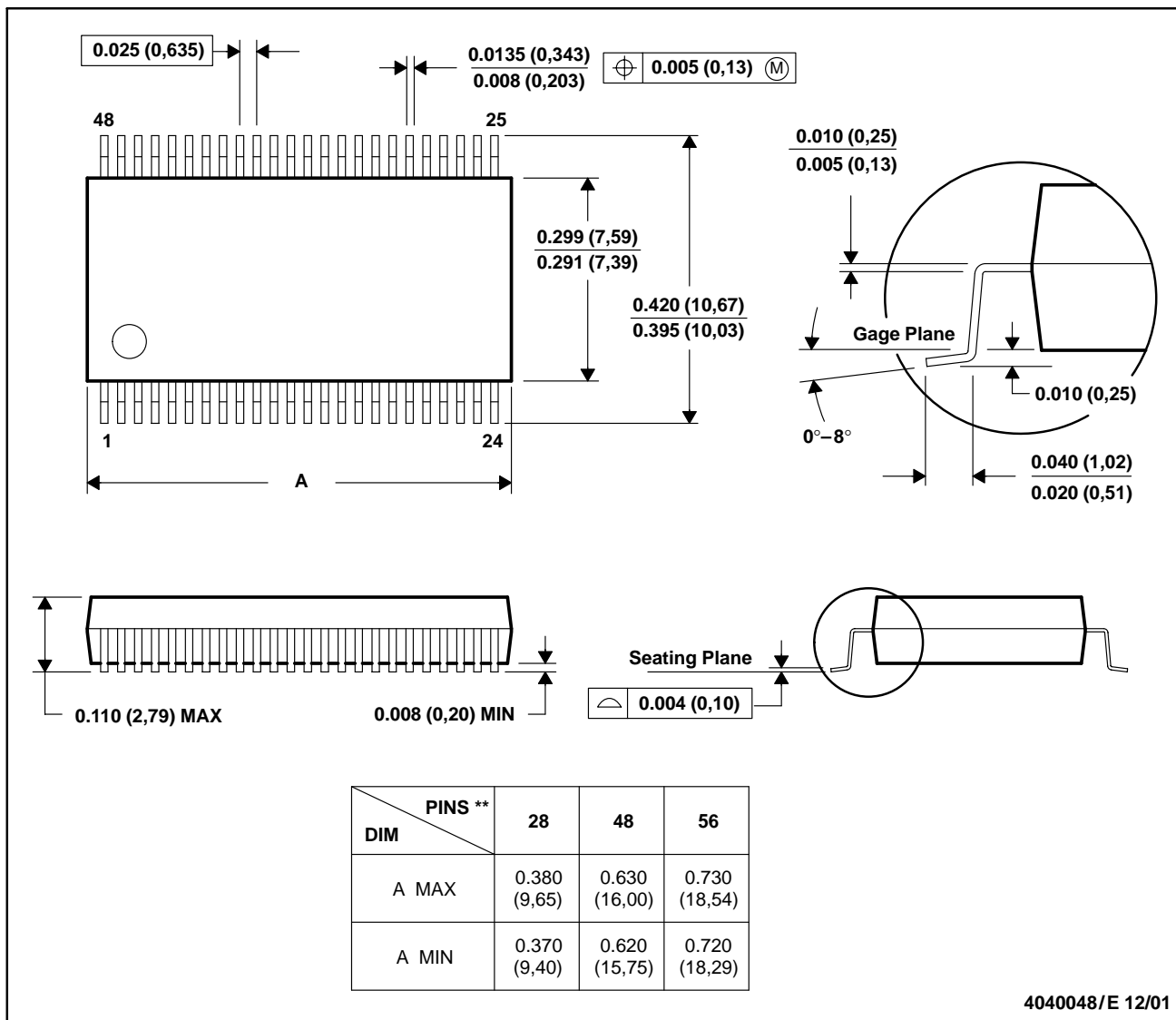
## MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

**DL (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118



**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2008, Texas Instruments Incorporated