

## Excellent Integrated System Limited

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[Texas Instruments](#)  
[SN74LVCH16952ADGGR](#)

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## FEATURES

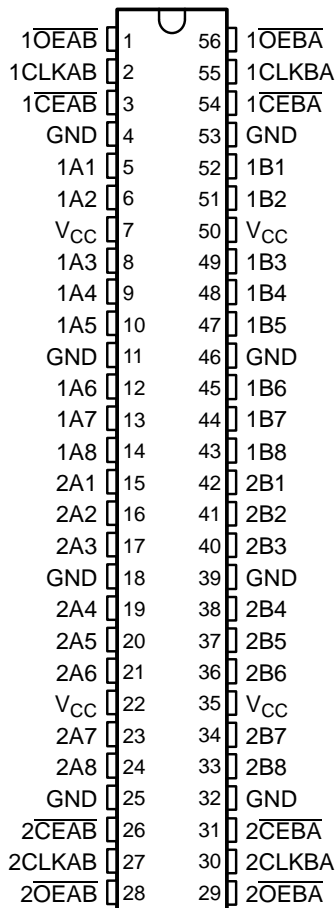
- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.6 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCH16952A contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock ( $\overline{\text{CLKAB}}$  or  $\overline{\text{CLKBA}}$ ) input, provided that the clock-enable ( $\overline{\text{CEAB}}$  or  $\overline{\text{CEBA}}$ ) input is low. Taking the output-enable ( $\overline{\text{OEAB}}$  or  $\overline{\text{OEBA}}$ ) input low accesses the data on either port.

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVCH16952ADL	LVCH16952A
		Tape and reel	SN74LVCH16952ADLR	
	TSSOP – DGG	Tape and reel	SN74LVCH16952ADGGR	LVCH16952A
	TVSOP – DGV	Tape and reel	SN74LVCH16952ADGVR	LDH952A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN74LVCH16952A**  
**16-BIT REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCAS320L–NOVEMBER 1993–REVISED MARCH 2005

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

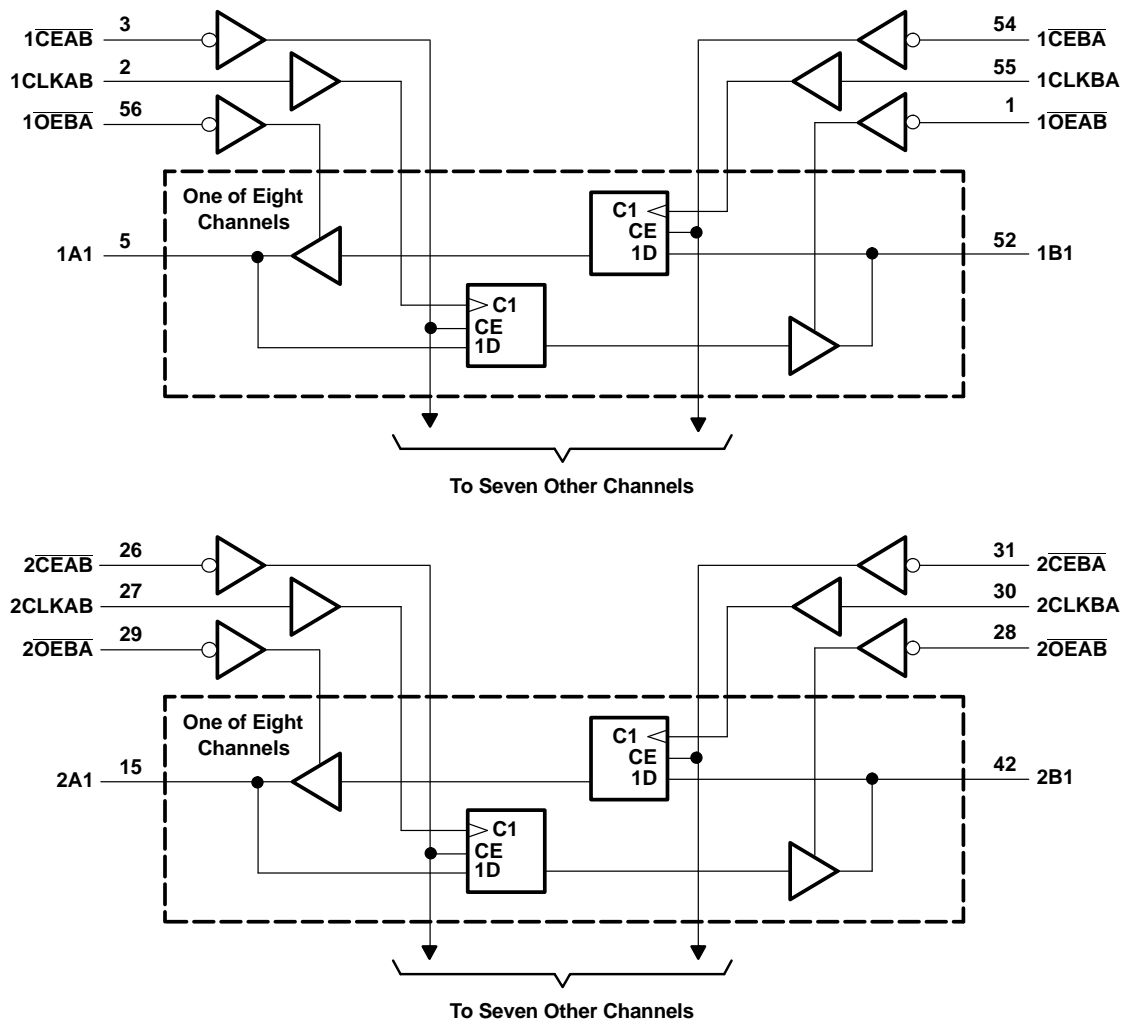
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by  $\overline{OE}$  or DIR.

**FUNCTION TABLE<sup>(1)</sup>**

INPUTS				OUTPUT B
$\overline{CEBA}$	CLKAB	$\overline{OEBA}$	A	
H	X	L	X	$B_0^{(2)}$
X	L	L	X	$B_0^{(2)}$
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

- (1) A-to-B data flow is shown; B-to-A data flow is similar, but uses  $\overline{CEBA}$ , CLKBA, and  $\overline{OEBA}$ .  
(2) Level of B before the indicated steady-state input conditions were established

**LOGIC DIAGRAM (POSITIVE LOGIC)**



# SN74LVCH16952A

## 16-BIT REGISTERED TRANSCEIVER

### WITH 3-STATE OUTPUTS

SCAS320L—NOVEMBER 1993—REVISED MARCH 2005



#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	−0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	−0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	−0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	−0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		−50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		−50 mA
I <sub>O</sub>	Continuous output current			±50 mA
	Continuous current through V <sub>CC</sub> or GND			±100 mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package		64 °C/W
		DGV package		48 °C/W
		DL package		56 °C/W
T <sub>stg</sub>	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JEDEC 51-7.

#### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6
		Data retention only	1.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>
		3-state	0	5.5
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	−4	mA
		V <sub>CC</sub> = 2.3 V	−8	
		V <sub>CC</sub> = 2.7 V	−12	
		V <sub>CC</sub> = 3 V	−24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4	mA
		V <sub>CC</sub> = 2.3 V	8	
		V <sub>CC</sub> = 2.7 V	12	
		V <sub>CC</sub> = 3 V	24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T <sub>A</sub>	Operating free-air temperature	−40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = −100 μA	1.65 V to 3.6 V	V <sub>CC</sub> − 0.2			V
		I <sub>OH</sub> = −4 mA	1.65 V	1.2			
		I <sub>OH</sub> = −8 mA	2.3 V	1.7			
		I <sub>OH</sub> = −12 mA	2.7 V	2.2			
			3 V	2.4			
		I <sub>OH</sub> = −24 mA	3 V	2.2			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		I <sub>OL</sub> = 8 mA	2.3 V			0.7	
		I <sub>OL</sub> = 12 mA	2.7 V			0.4	
		I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	μA
I <sub>I(hold)</sub>	A or B ports	V <sub>I</sub> = 0.58 V	1.65 V	15			μA
		V <sub>I</sub> = 1.07 V		−15			
		V <sub>I</sub> = 0.7 V	2.3 V	45			
		V <sub>I</sub> = 1.7 V		−45			
		V <sub>I</sub> = 0.8 V	3 V	75			
		V <sub>I</sub> = 2 V		−75			
		V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V	±500			
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	±10		μA	
I <sub>OZ</sub> <sup>(3)</sup>		V <sub>O</sub> = 0 V or (V <sub>CC</sub> to 5.5 V)	3.6 V	±10		μA	
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	20		μA	
		3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(4)</sup> , I <sub>O</sub> = 0		20			
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500		μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5		pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	8.5		pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current required to switch the input from one state to another.

(3) For the total leakage current in an I/O port, please consult the I<sub>I(hold)</sub> specification for the input voltage condition 0 V < V<sub>I</sub> < V<sub>CC</sub>, and the I<sub>OZ</sub> specification for the input voltage conditions V<sub>I</sub> = 0 V or V<sub>I</sub> = V<sub>CC</sub> to 5.5 V. The bus-hold current, at input voltage greater than V<sub>CC</sub>, is negligible.

(4) This applies in the disabled state only.

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		130		150		150		150		MHz
t <sub>w</sub>	Pulse duration, CLK high or low		5		3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time	Data before CLK↑	5.8		3.4		3.4		2.8		ns
		$\overline{\text{CE}}$ before CLK↑	1.4		1.3		1.8		1.4		
t <sub>h</sub>	Hold time	Data after CLK↑	0		0.5		0.5		0.5		ns
		$\overline{\text{CE}}$ after CLK↑	1.1		1.6		1.1		1.9		

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**16-BIT REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCAS320L–NOVEMBER 1993–REVISED MARCH 2005



**Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

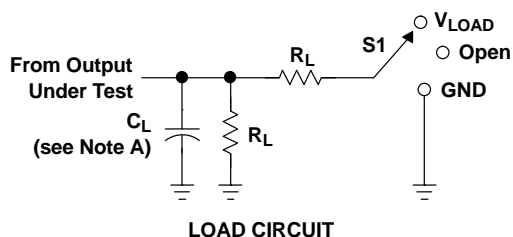
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			130		150		150		150		MHz
$t_{pd}$	CLKAB or CLKBA	B or A	2	11	1	7.6	1	7.6	1.6	6.6	ns
$t_{en}$	$\overline{OE}$	A or B	2	10.6	1	8	1	8	1.1	6.6	ns
$t_{dis}$	$\overline{OE}$	A or B	2	12.7	1	7.1	1	7.1	1.9	6.7	ns
$t_{sk(o)}$									1		ns

**Operating Characteristics**

$T_A = 25^\circ\text{C}$

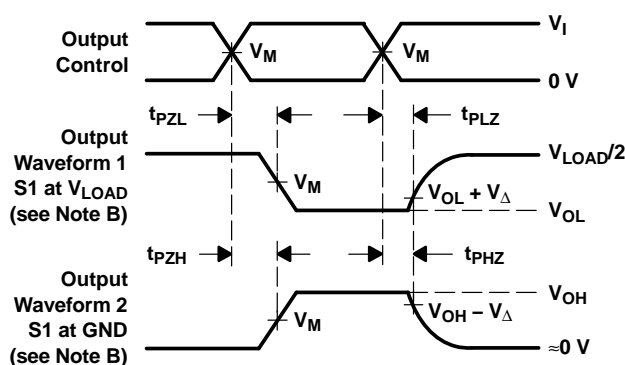
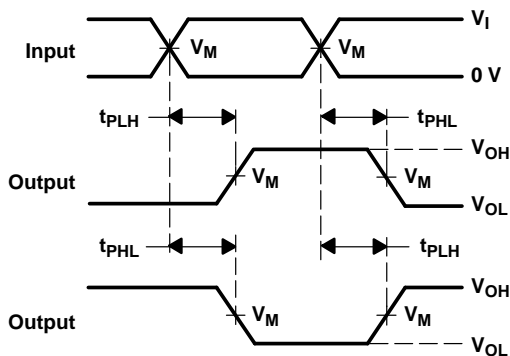
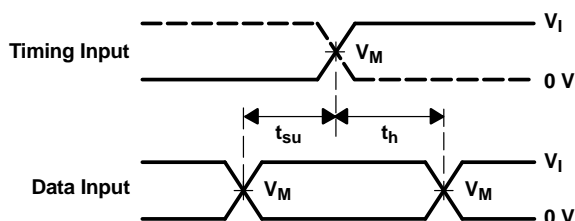
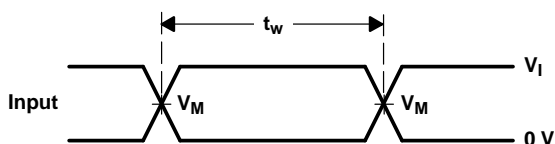
PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	55	61	69	pF
		Outputs disabled		22	24	27	

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74LVCH16952ADGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVCH16952ADGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVCH16952ADGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVCH16952ADGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVCH16952ADLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH16952ADGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH16952ADGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH16952ADL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH16952ADLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH16952ADLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

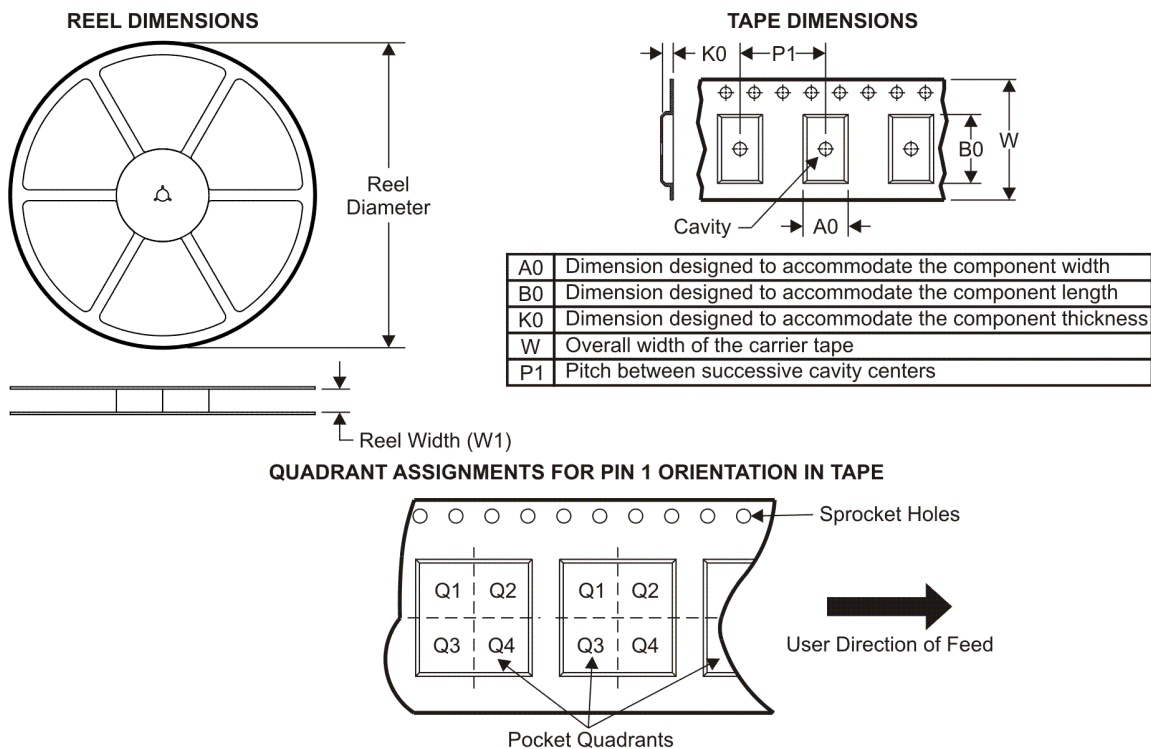
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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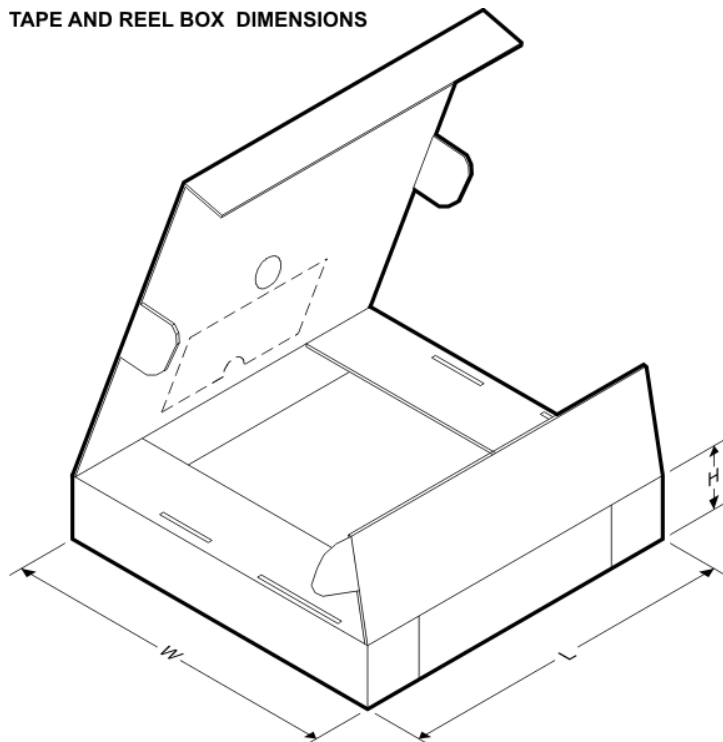
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH16952ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74LVCH16952ADGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74LVCH16952ADLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

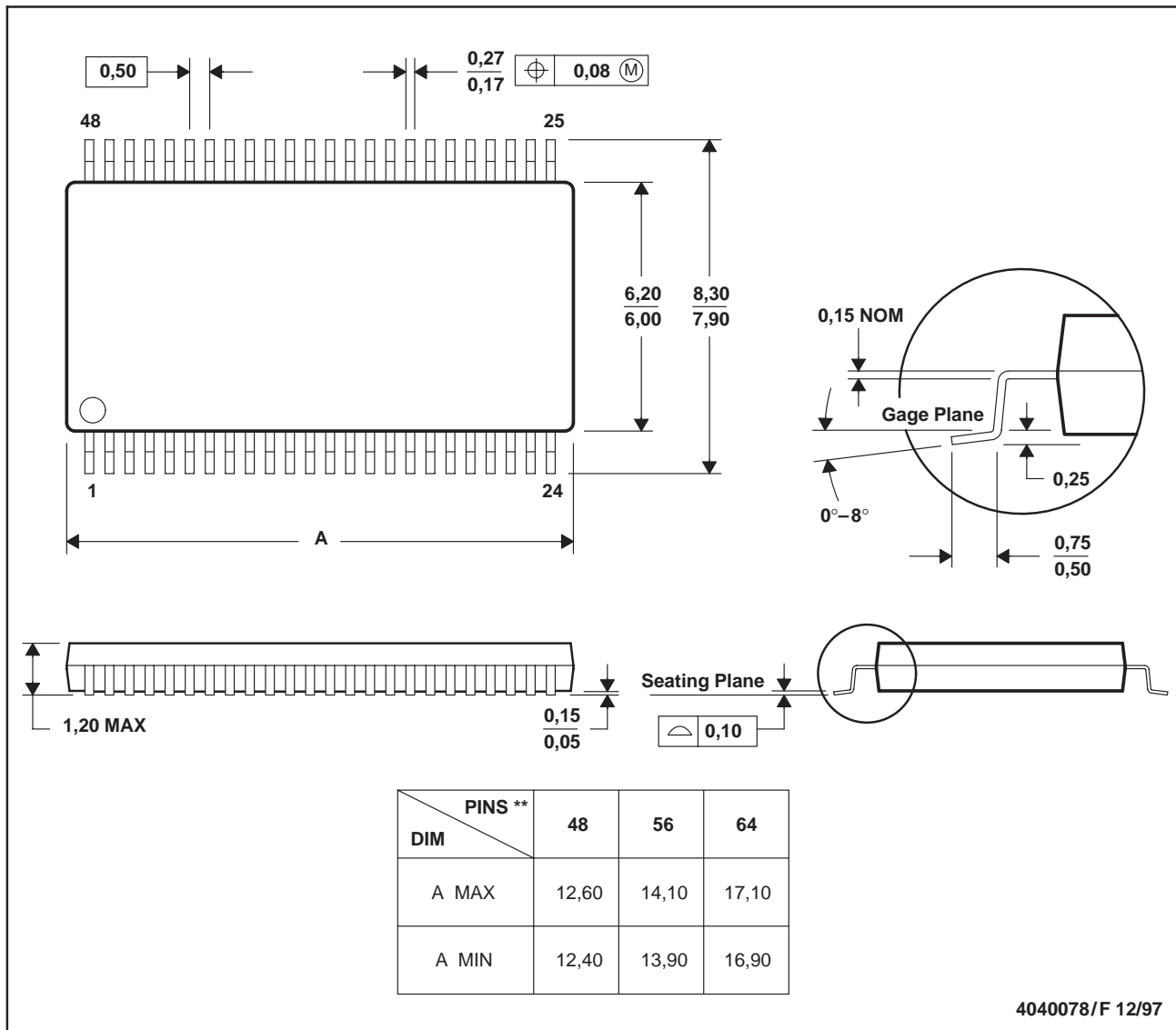
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH16952ADGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74LVCH16952ADGVR	TVSOP	DGV	56	2000	346.0	346.0	41.0
SN74LVCH16952ADLR	SSOP	DL	56	1000	346.0	346.0	49.0

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

**DGG (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold protrusion not to exceed 0,15.  
D. Falls within JEDEC MO-153



**TEXAS  
INSTRUMENTS**

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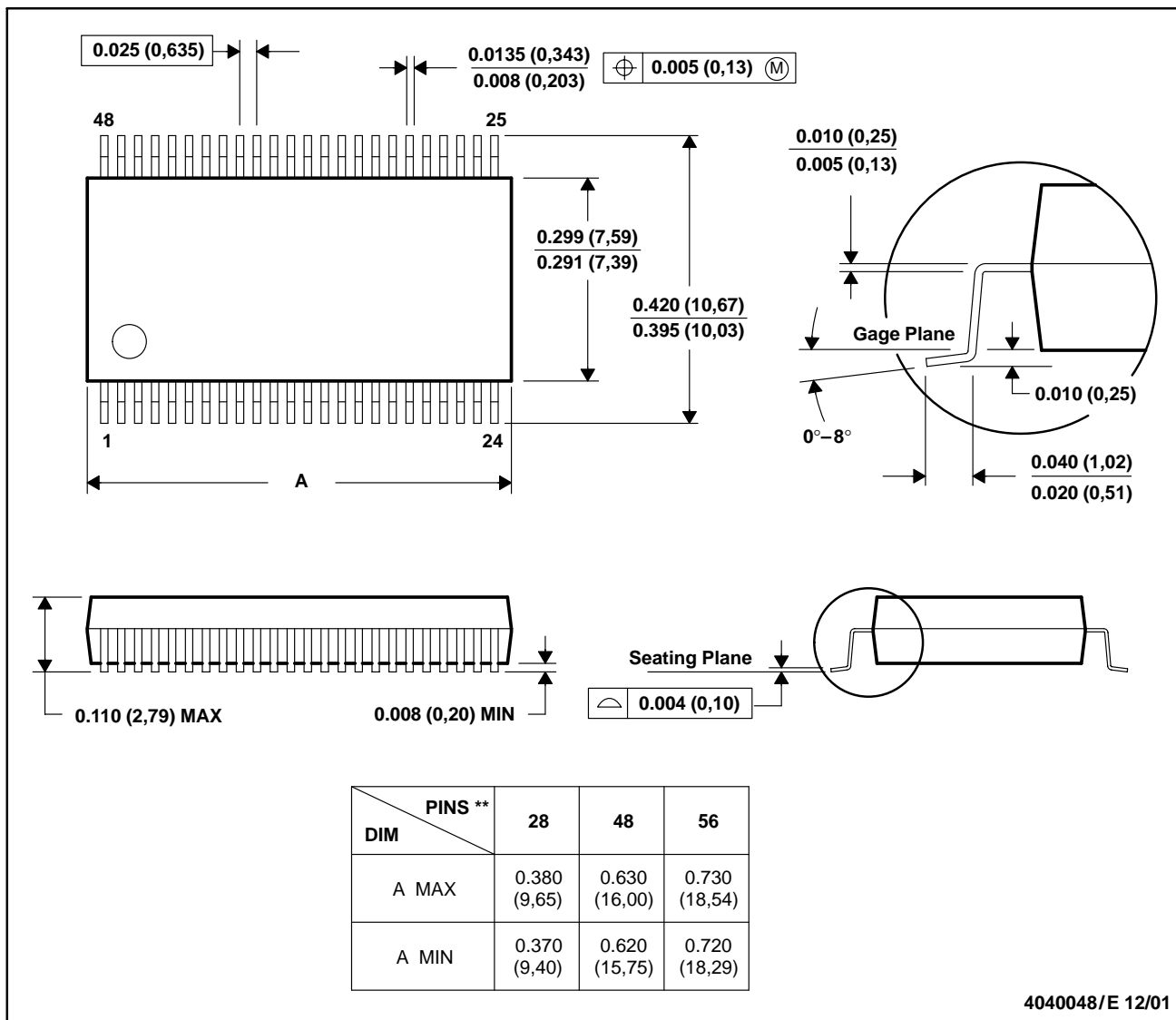
## MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

**DL (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118



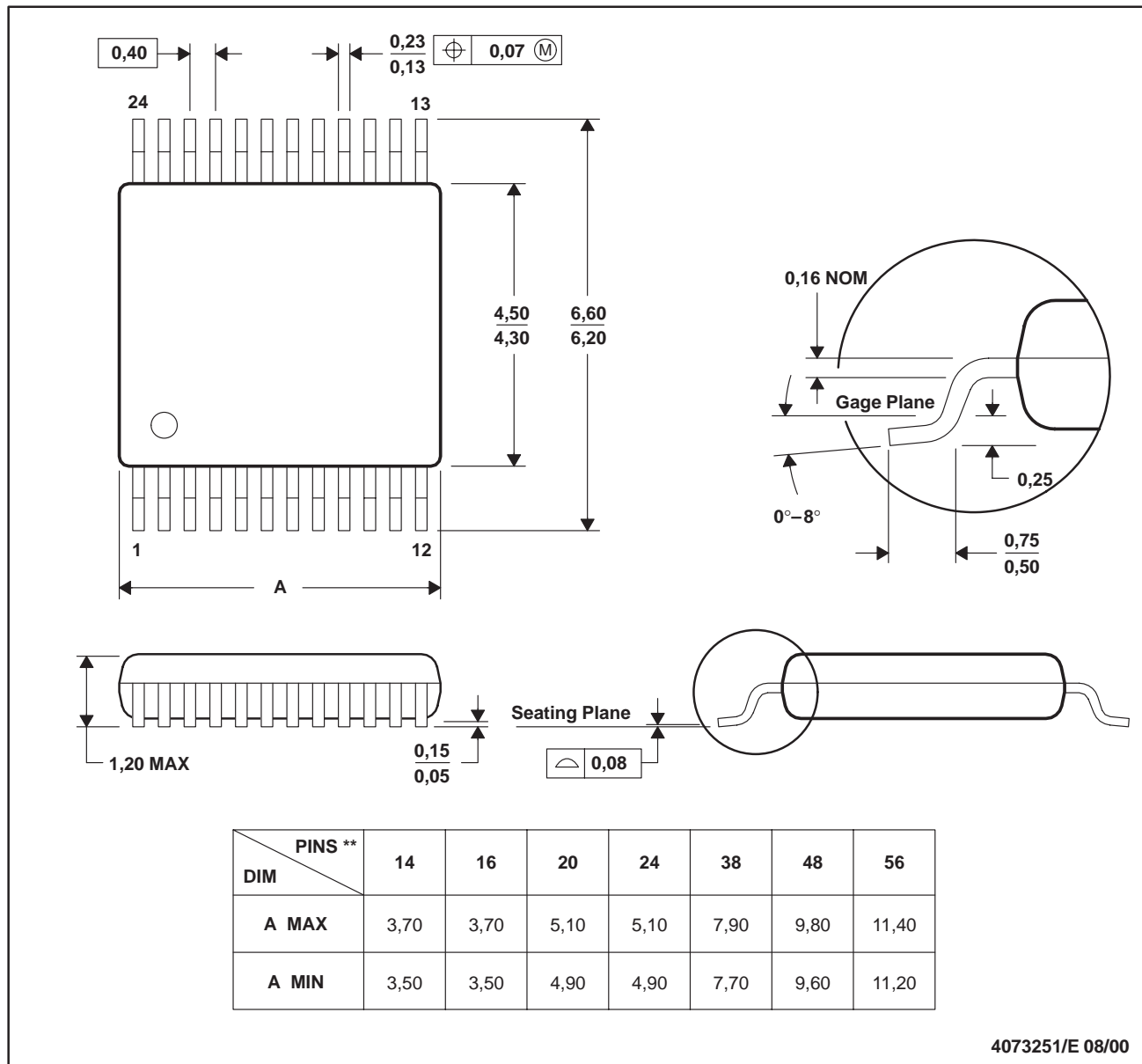
**TEXAS  
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**DGV (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
D. Falls within JEDEC: 24/48 Pins – MO-153  
14/16/20/56 Pins – MO-194

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