

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Texas Instruments](#)
[SN74LS90D](#)

For any questions, you can email us directly:

sales@integrated-circuit.com

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

'90A, 'LS90 . . . Decade Counters

'92A, 'LS92 . . . Divide By-Twelve Counters

'93A, 'LS93 . . . 4-Bit Binary Counters

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'92A, '93A	130 mW
'LS90, 'LS92, 'LS93	45 mW

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

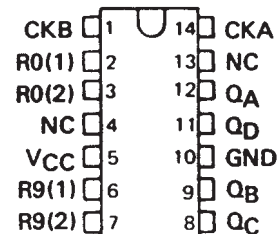
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the Q_D output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q_A .

SN5490A, SN54LS90 . . . J OR W PACKAGE

SN7490A . . . N PACKAGE

SN74LS90 . . . D OR N PACKAGE

(TOP VIEW)

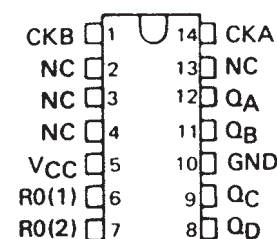


SN5492A, SN54LS92 . . . J OR W PACKAGE

SN7492A . . . N PACKAGE

SN74LS92 . . . D OR N PACKAGE

(TOP VIEW)

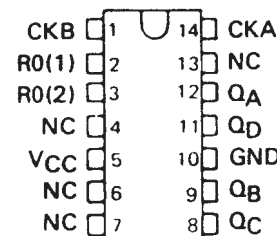


SN5493A, SN54LS93 . . . J OR W PACKAGE

SN7493 . . . N PACKAGE

SN74LS93 . . . D OR N PACKAGE

(TOP VIEW)



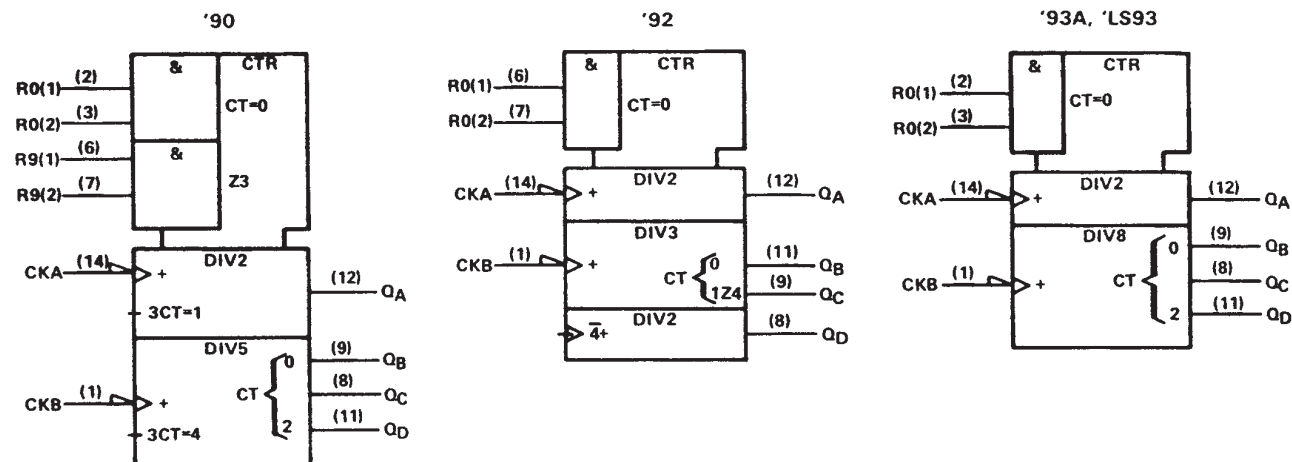
SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93

SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93

DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A - MARCH 1974 - REVISED MARCH 1988

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

**'90A, 'LS90
BCD COUNT SEQUENCE
(See Note A)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**'90A, 'LS90
BI-QUINARY (5-2)
(See Note B)**

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

**'92A, 'LS92
COUNT SEQUENCE
(See Note C)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

**'90A, 'LS90
RESET/COUNT FUNCTION TABLE**

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

**'93A, 'LS93
COUNT SEQUENCE
(See Note C)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

**'92A, 'LS92, '93A, 'LS93
RESET/COUNT FUNCTION TABLE**

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for bi-quinary count.
C. Output Q_A is connected to input CKB.
D. H = high level, L = low level, X = irrelevant



**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

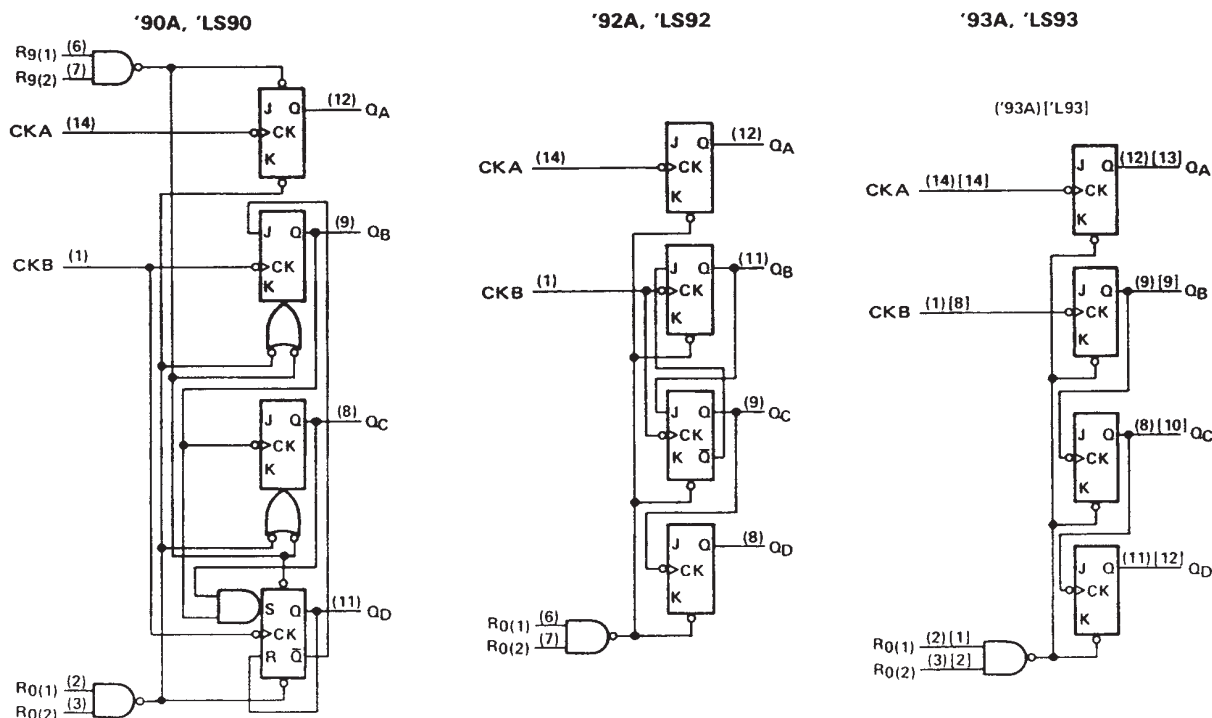
SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93

SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93

DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

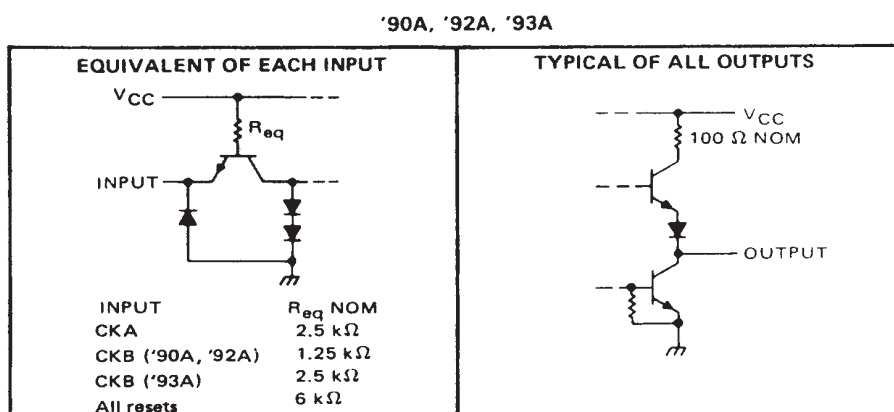
SDLS940A - MARCH 1974 - REVISED MARCH 1988

logic diagrams (positive logic)



The J and K inputs shown without connection are for reference only and are functionally at a high level.
Pin numbers shown in () are for the 'LS93 and '93A and pin numbers shown in [] are for the 54L93.

schematics of inputs and outputs

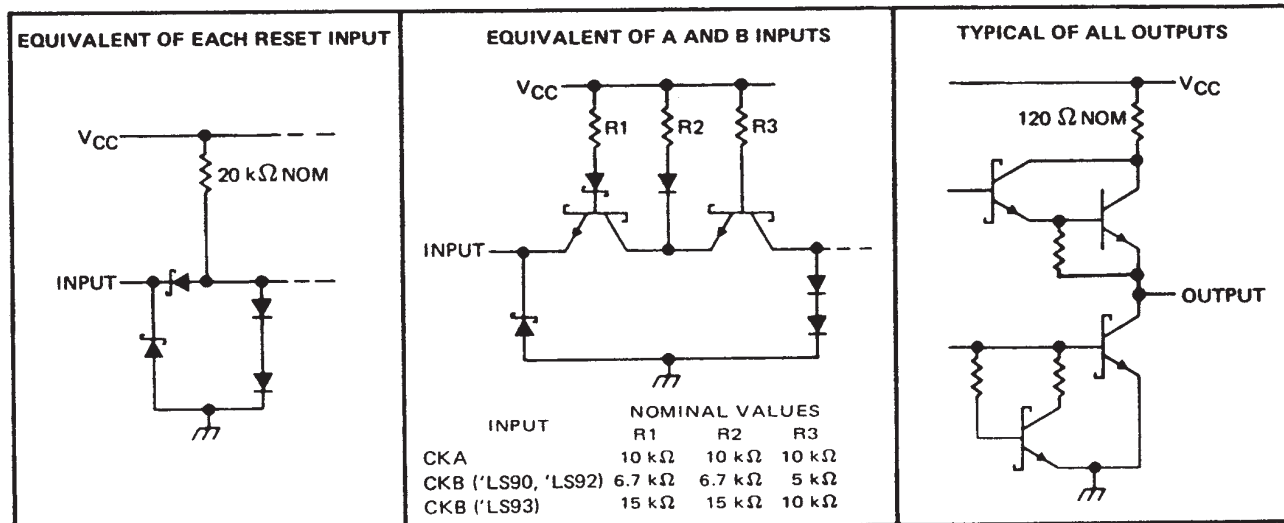


**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

schematics of inputs and outputs (continued)

'LS90, 'LS92, 'LS93



**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93

SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93

DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A - MARCH 1974 - REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A	-55°C to 125°C
SN7490A, SN7492A, SN7493A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_O inputs, and for the '90A circuit, it also applies between the two R_B inputs.

recommended operating conditions

		SN5490A, SN5492A SN5493A			SN7490A, SN7492A SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-800			-800			μ A
Low-level output current, I_{OL}		16			16			mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_W	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{SU}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER [¶]		TEST CONDITIONS [†]			'90A			'92A			'93A			UNIT
					MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$					-1.5			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$			2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA} ¶¶$				0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$					1			1			1	mA
I_{IH}	High-level input current	Any reset	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$				40			40			40	μ A
		CKA					80			80			80	
		CKB					120			120			80	
I_{IL}	Low-level input current	Any reset	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-1.6			-1.6			-1.6	mA
		CKA					-3.2			-3.2			-3.2	
		CKB					-4.8			-4.8			-3.2	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$		SN54'	-20	-57		-20	-57		-20	-57		mA
				SN74'	-18	-57		-18	-57		-18	-57		
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$				29	42		26	39		26	39	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

^{¶¶} Q_A outputs are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A		'92A		'93A		UNIT
				MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
f _{max}	CKA	Q _A	C _L = 15 pF, R _L = 400 Ω, See Figure 1	32	42	32	42	32	42	MHz
	CKB	Q _B		16		16		16		
t _{PLH}	CKA	Q _A		10	16	10	16	10	16	ns
t _{PHL}		12		18	12	18	12	18		
t _{PLH}	CKA	Q _D		32	48	32	48	46	70	ns
t _{PHL}		34		50	34	50	46	70		
t _{PLH}	CKB	Q _B		10	16	10	16	10	16	ns
t _{PHL}		14		21	14	21	14	21		
t _{PLH}	CKB	Q _C		21	32	10	16	21	32	ns
t _{PHL}		23		35	14	21	23	35		
t _{PLH}	CKB	Q _D		21	32	21	32	34	51	ns
t _{PHL}		23		35	23	35	34	51		
t _{PHL}	Set-to-0	Any		26	40	26	40	26	40	ns
t _{PLH}	Set-to-9	Q _A , Q _D		20	30					ns
t _{PHL}		Q _B , Q _C		26	40					

† $f_{\max}$ = maximum count frequency

 t_{PLH} = propagation delay time, low-to-high-level output

 t_{PHL} = propagation delay time, high-to-low-level output


TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93

SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93

DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A - MARCH 1974 - REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: SN54LS' Circuits	-55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS90 SN54LS92 SN54LS93			SN74LS90 SN74LS92 SN74LS93			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μ A
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	30			30			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS90 SN54LS92			SN74LS90 SN74LS92			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}^{\S}$		0.25	0.4		0.25	0.4		V
		$I_{OL} = 8 \text{ mA}^{\P}$					0.35	0.5		
I_I	Input current at maximum input voltage	Any reset	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
		CKA	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			0.2			0.2	
		CKB				0.4			0.4	
I_{IH}	High-level input current	Any reset	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
		CKA				40			40	
		CKB				80			80	
I_{IL}	Low-level input current	Any reset	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
		CKA				-2.4			-2.4	
		CKB				-3.2			-3.2	
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$		-20		-100	-20		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 3	'LS90		9	15		9	15	mA
			'LS92		9	15		9	15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ QA outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54LS93		SN74LS93		UNIT	
				MIN	TYP‡ MAX	MIN	TYP‡ MAX		
V _{IH}	High-level input voltage				2		2	V	
V _{IL}	Low-level input voltage					0.7		0.8	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA				-1.5	-1.5	V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA		2.5	3.4	2.7	3.4	V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA¶		0.25	0.4	0.25	0.4	V
			V _{IL} = V _{IL} max, I _{OL} = 8 mA¶				0.35	0.5	
I _I	Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V				0.1	0.1	mA
		CKA or CKB	V _{CC} = MAX, V _I = 5.5 V				0.2	0.2	
I _{IH}	High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V				20	20	µA
		CKA or CKB					40	80	
I _{IL}	Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V				-0.4	-0.4	mA
		CKA					-2.4	-2.4	
		CKB					-1.6	-1.6	
I _{OS}	Short-circuit output current§		V _{CC} = MAX		-20	-100	-20	-100	mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 3		9	15	9	15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ Q_A outputs are tested at specified I_{OL} plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90		'LS92		'LS93		UNIT
				MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
f _{max}	CKA	Q _A	C _L = 15 pF, R _L = 2 kΩ See Figure 1	32	42	32	42	32	42	MHz
	CKB	Q _B		16		16		16		
t _{PLH}	CKA	Q _A		10	16	10	16	10	16	ns
t _{PHL}				12	18	12	18	12	18	
t _{PLH}	CKA	Q _D		32	48	32	48	46	70	ns
t _{PHL}				34	50	34	50	46	70	
t _{PLH}	CKB	Q _B		10	16	10	16	10	16	ns
t _{PHL}				14	21	14	21	14	21	
t _{PLH}	CKB	Q _C		21	32	10	16	21	32	ns
t _{PHL}				23	35	14	21	23	35	
t _{PLH}	CKB	Q _D		21	32	21	32	34	51	ns
t _{PHL}				23	35	23	35	34	51	
t _{PHL}	Set-to-0	Any		26	40	26	40	26	40	ns
t _{PLH}	Set-to-9	Q _A , Q _D		20	30					ns
t _{PHL}		Q _B , Q _C		26	40					

#f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output



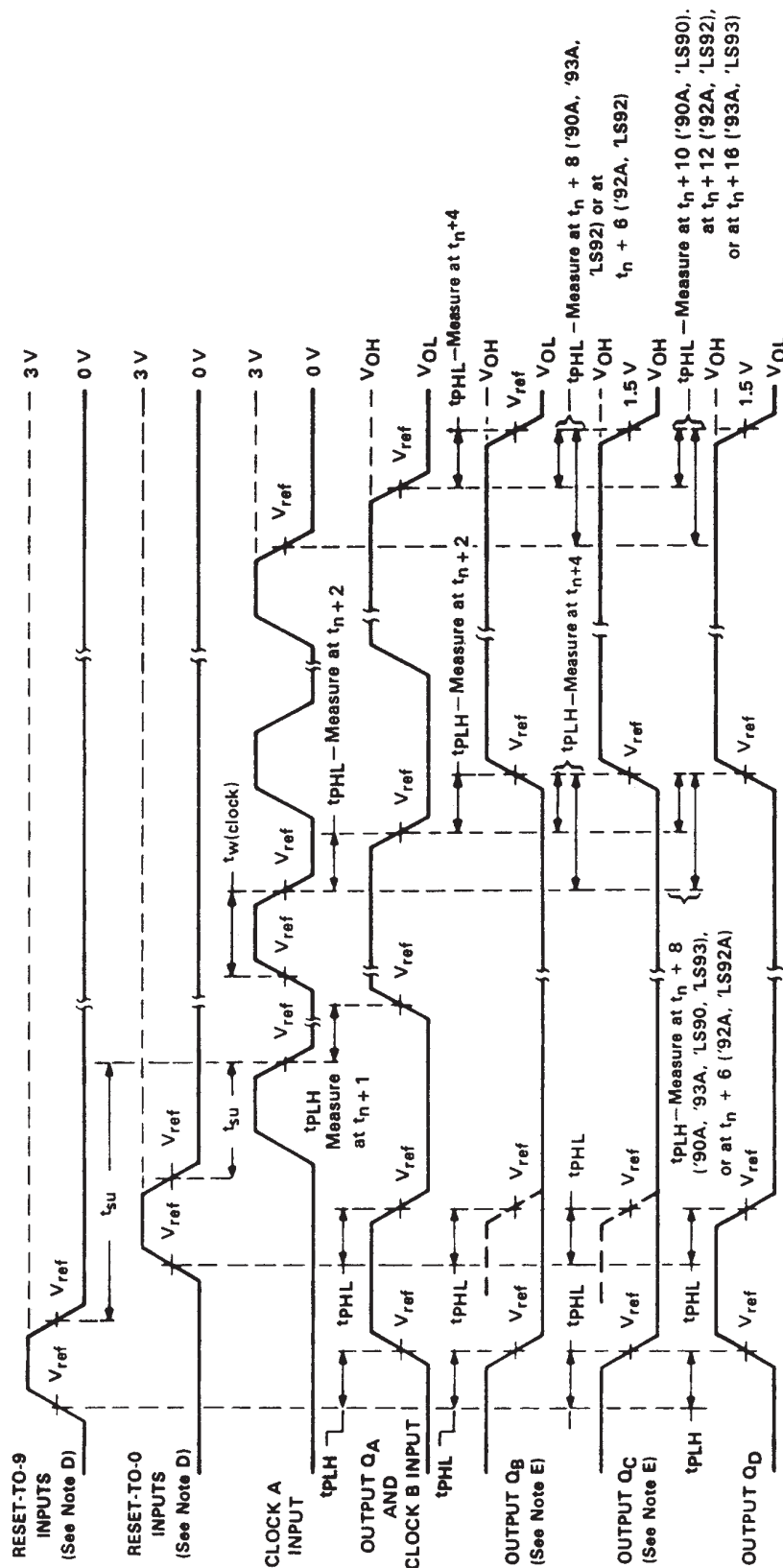
**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A', '92A', '93A', $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90', 'LS92', 'LS93', $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

B. C_I includes probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.

D. Each reset input is tested separately with the other reset at 4.5 V.

E. Reference waveforms are shown with dashed lines.

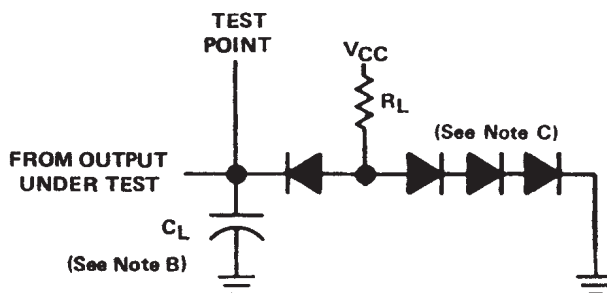
F. For '90A, '92A, and '93A; $V_{\text{ref}} = 1.5$ V. For 'LS90, 'LS92, and 'LS93: $V_{\text{ref}} = 1.3$ V.

FIGURE 1A

**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A - MARCH 1974 - REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

- NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. Each reset input is tested separately with the other reset at 4.5 V.
- E. Reference waveforms are shown with dashed lines.
- F. For '90A, '92A, and '93A; $V_{ref} = 1.5$ V. For 'LS90, 'LS92, and 'LS93; $V_{ref} = 1.3$ V.

FIGURE 1B



**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7603201CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603201CA SNJ54LS90J	Samples
7700101CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7700101CA SNJ54LS93J	Samples
7700101DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7700101DA SNJ54LS93W	Samples
JM38510/31501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31501BCA	Samples
JM38510/31502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31502BCA	Samples
JM38510/31502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31502BDA	Samples
M38510/31501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31501BCA	Samples
M38510/31502BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31502BCA	Samples
M38510/31502BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31502BDA	Samples
SN5490AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SN5492AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SN54LS90J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS90J	Samples
SN54LS93J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS93J	Samples
SN7490AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7492AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7493AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS90-W	ACTIVE	WAFERSALE	YS	0		TBD	Call TI	Call TI			Samples
SN74LS90D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS90	Samples
SN74LS90DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS90	Samples
SN74LS90DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS90	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS90DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS90	Samples
SN74LS90DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS90	Samples
SN74LS90N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS90N	Samples
SN74LS90NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS90N	Samples
SN74LS92D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS92	Samples
SN74LS92DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS92	Samples
SN74LS92N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS92N	Samples
SN74LS92N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS92NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS92N	Samples
SN74LS92NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS92	Samples
SN74LS93D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS93	Samples
SN74LS93DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS93	Samples
SN74LS93N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS93N	Samples
SN74LS93N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS93NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS93N	Samples
SNJ5490AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5490AW	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5492AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5492AW	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	-55 to 125		
SNJ54LS90J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603201CA SNJ54LS90J	Samples
SNJ54LS93J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7700101CA	Samples



Distributor of Texas Instruments: Excellent Integrated System Limited

Datasheet of SN74LS90D - IC DECADE COUNTER 14-SOIC

Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

PACKAGE OPTION ADDENDUM

www.ti.com

17-Dec-2015

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS93W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS93J 7700101DA SNJ54LS93W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



www.ti.com

Distributor of Texas Instruments: Excellent Integrated System Limited

Datasheet of SN74LS90D - IC DECADE COUNTER 14-SOIC

Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

PACKAGE OPTION ADDENDUM

17-Dec-2015

OTHER QUALIFIED VERSIONS OF SN5490A, SN5492A, SN54LS90, SN54LS93, SN7490A, SN7492A, SN74LS90, SN74LS93 :

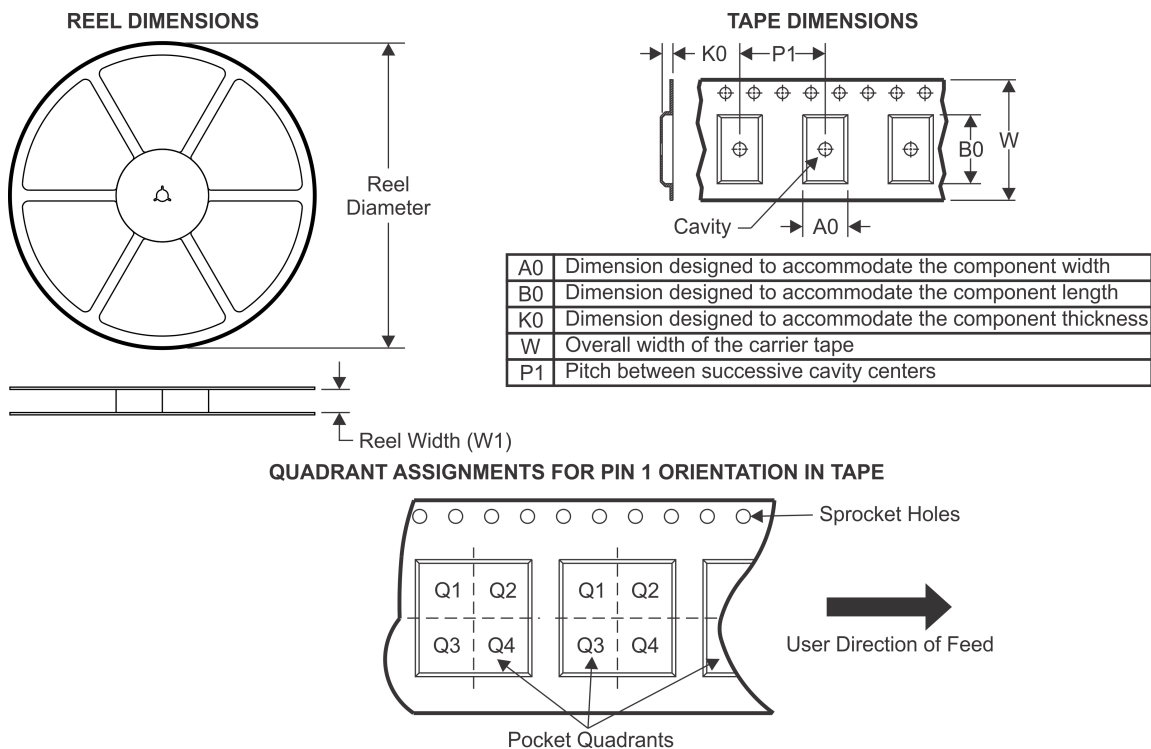
- Catalog: [SN7490A](#), [SN7492A](#), [SN74LS90](#), [SN74LS93](#)
- Military: [SN5490A](#), [SN5492A](#), [SN54LS90](#), [SN54LS93](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

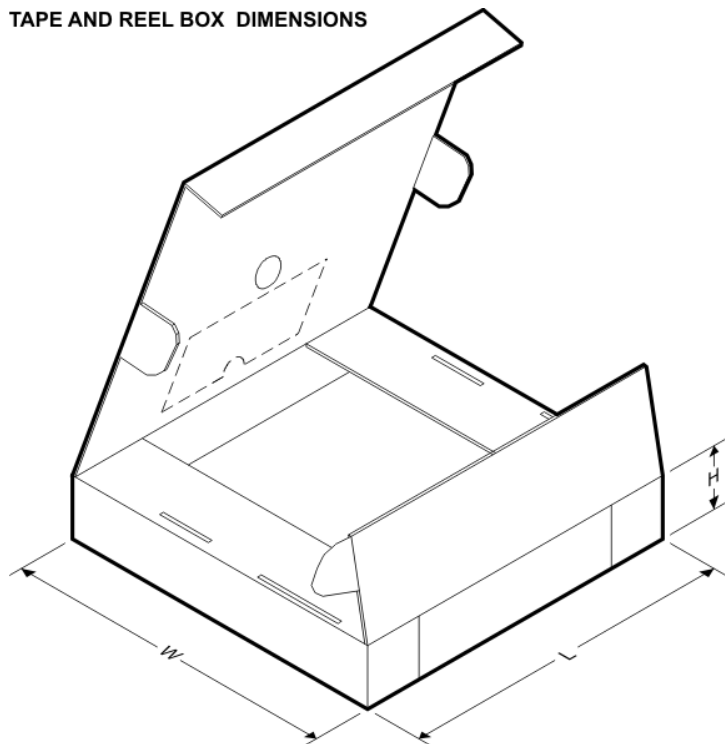
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS90DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS92NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



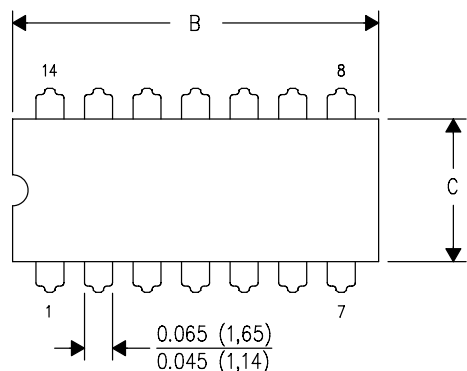
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS90DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS92NSR	SO	NS	14	2000	367.0	367.0	38.0

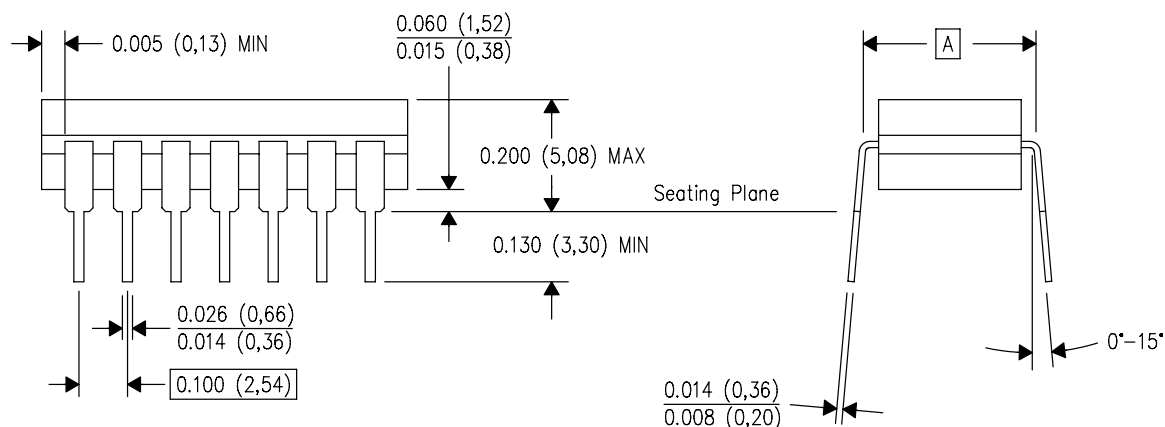
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



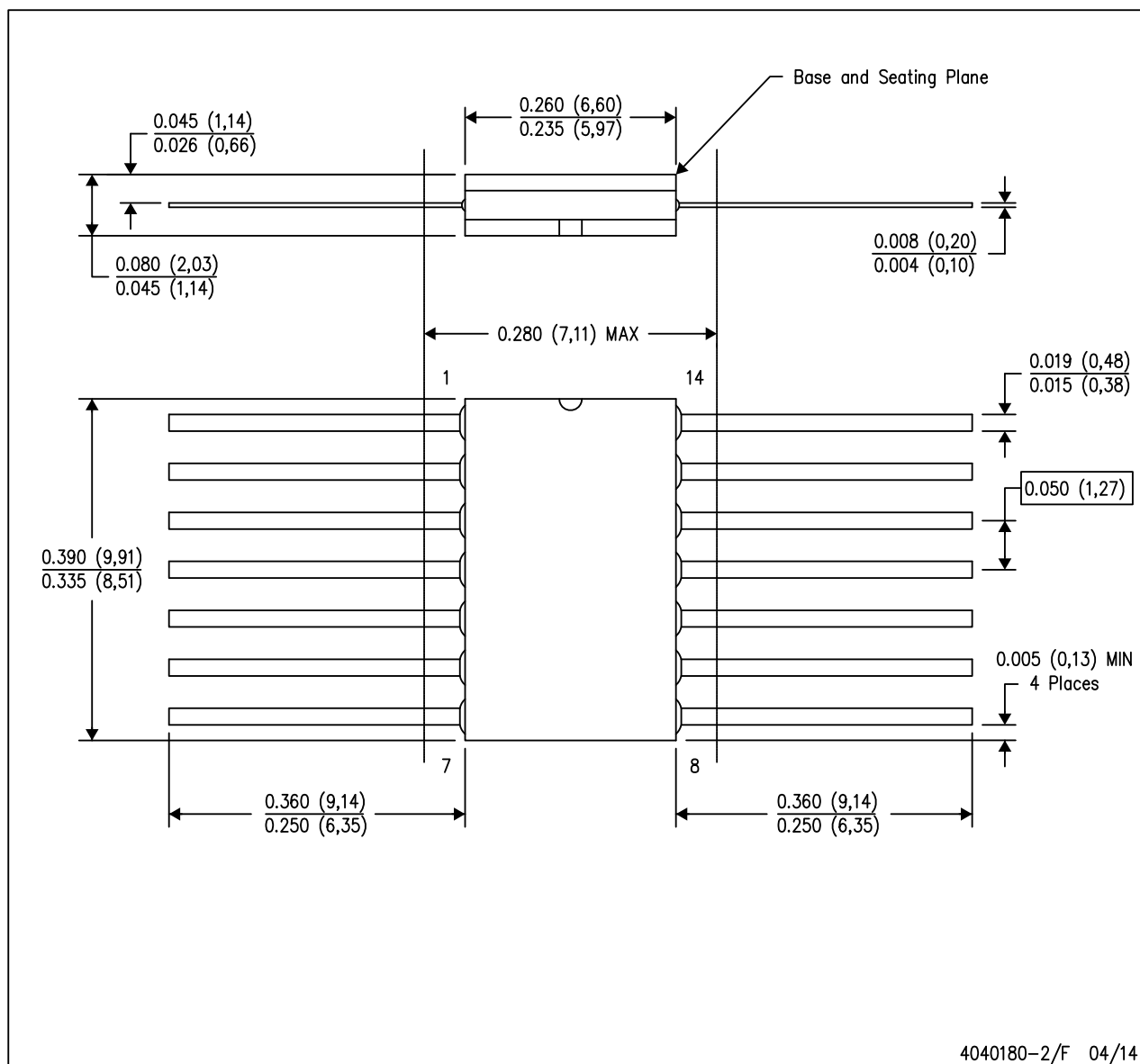
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



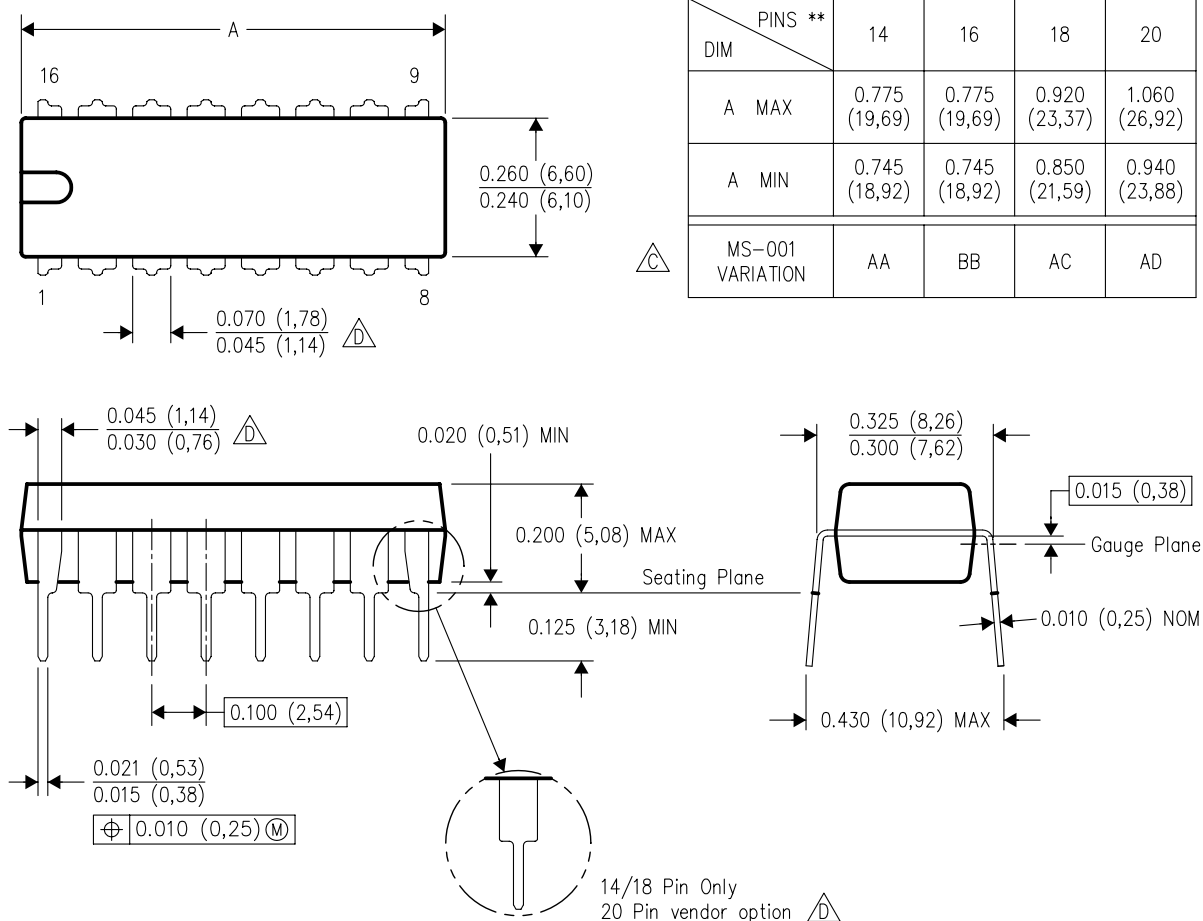
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

MECHANICAL DATA

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



4040049/E 12/2002

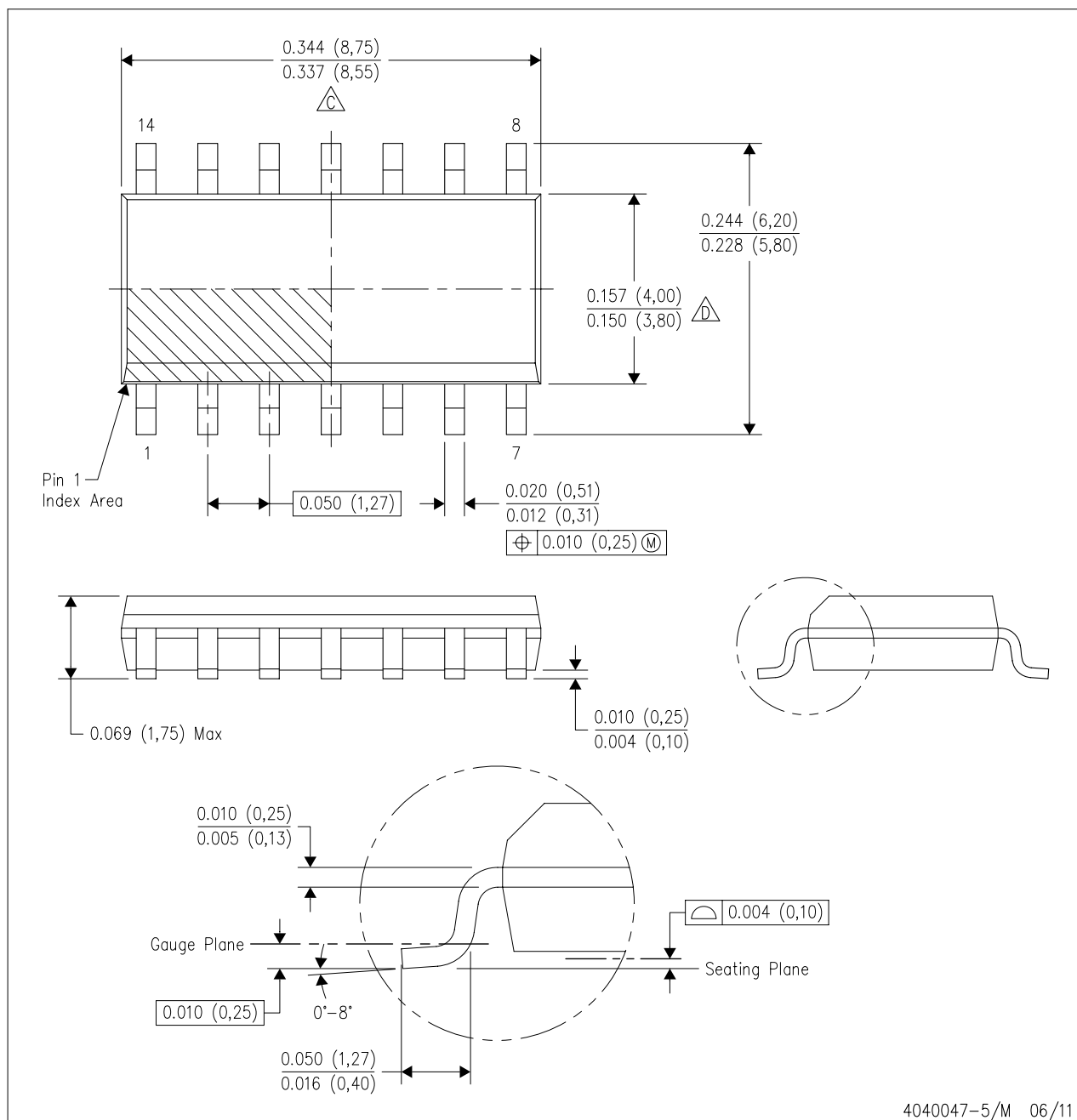
NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

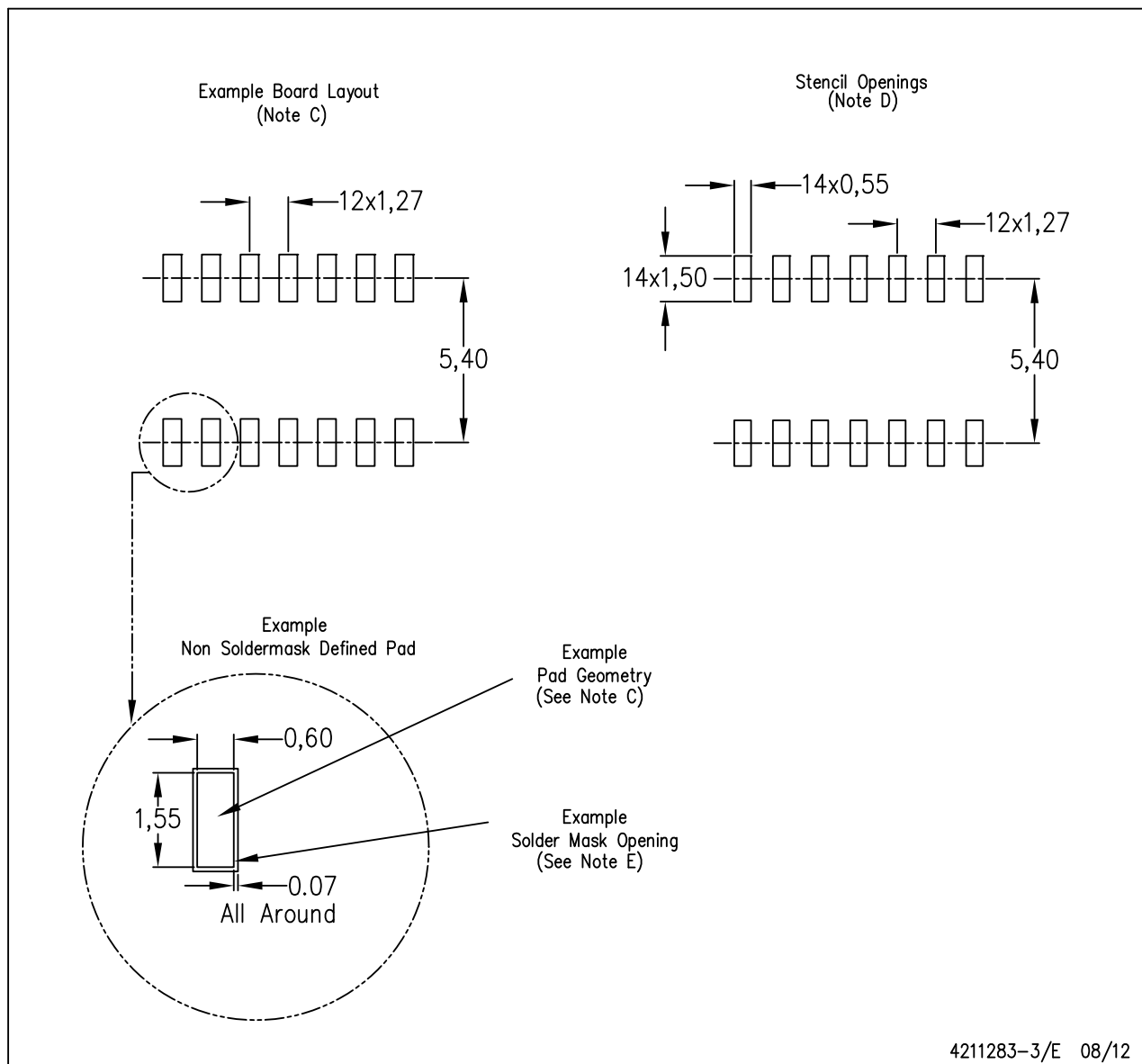
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

LAND PATTERN DATA

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



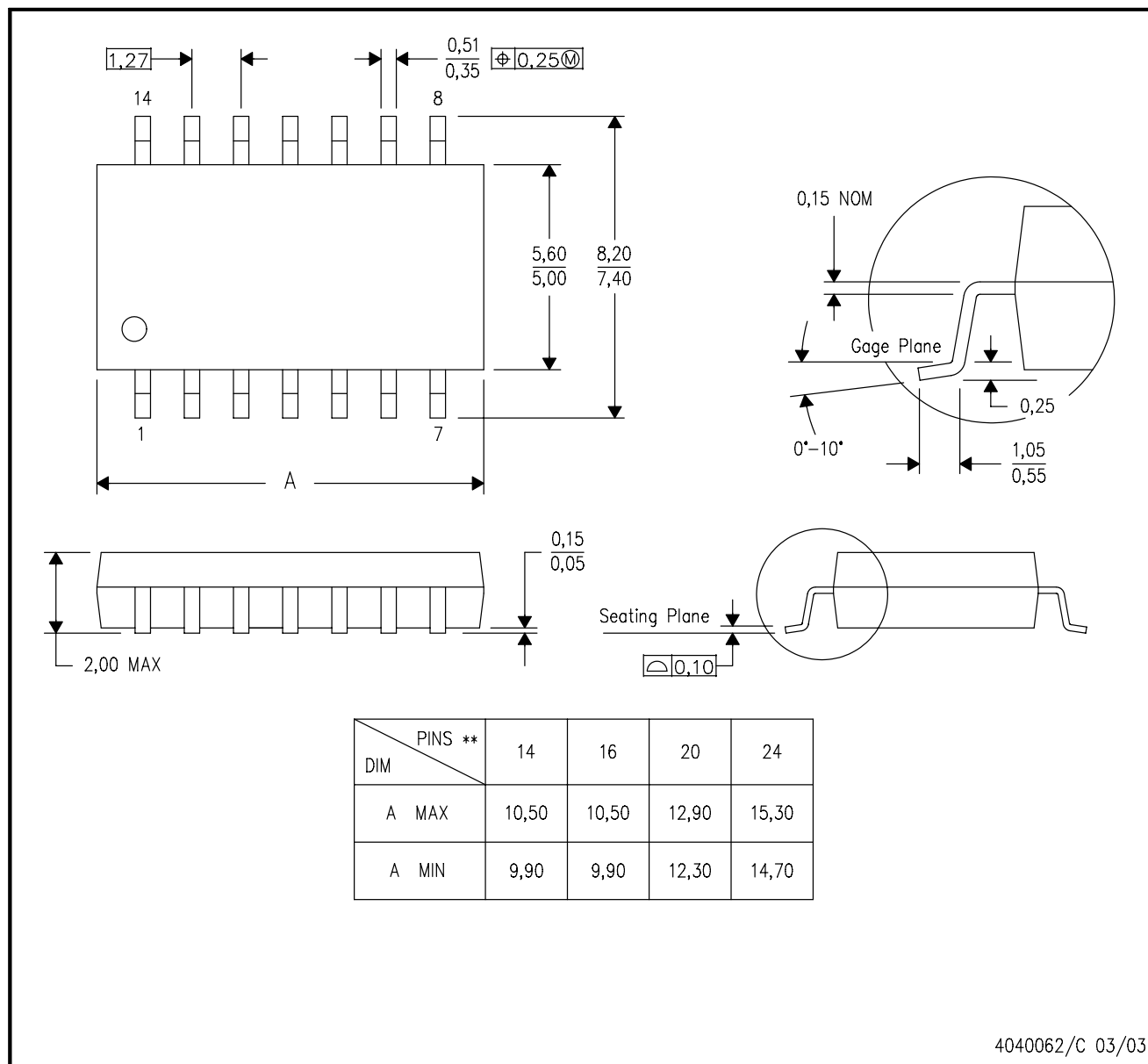
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com