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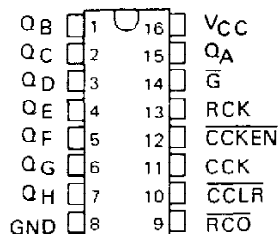
**SN54LS590, SN54LS591, SN74LS590, SN74LS591**  
**8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS**

SDLS003 D2632, JANUARY 1981 - REVISED MARCH 1988

- 8-Bit Counter with Register
- Parallel Register Outputs
- Choice of 3-State ('LS590) or Open-Collector ('LS591) Register Outputs
- Guaranteed Counter Frequency: DC to 20 MHz

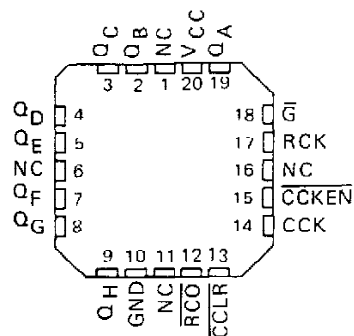
SN54LS590, SN54LS591 . . . J OR W PACKAGE  
 SN74LS590, SN74LS591 . . . N PACKAGE

(TOP VIEW)



SN54LS590, SN54LS591 . . . FK PACKAGE

(TOP VIEW)



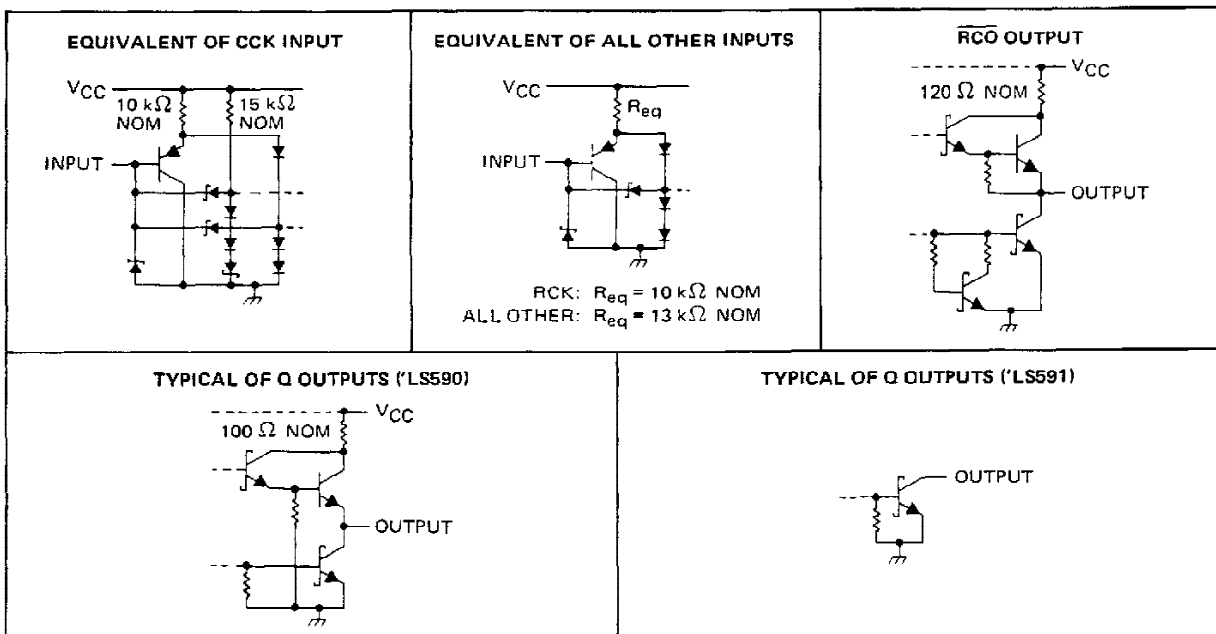
**description**

These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input  $\overline{CCLR}$  and a count enable input  $\overline{CCKEN}$ . For cascading, a ripple carry output  $\overline{RCO}$  is provided. Expansion is easily accomplished for two stages by connecting  $\overline{RCO}$  of the first stage to  $\overline{CCKEN}$  of the second stage. Cascading for larger count chains can be accomplished by connecting  $\overline{RCO}$  of each stage to  $\overline{CCK}$  of the following stage.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

NC - No internal connection

**schematics of inputs and outputs**

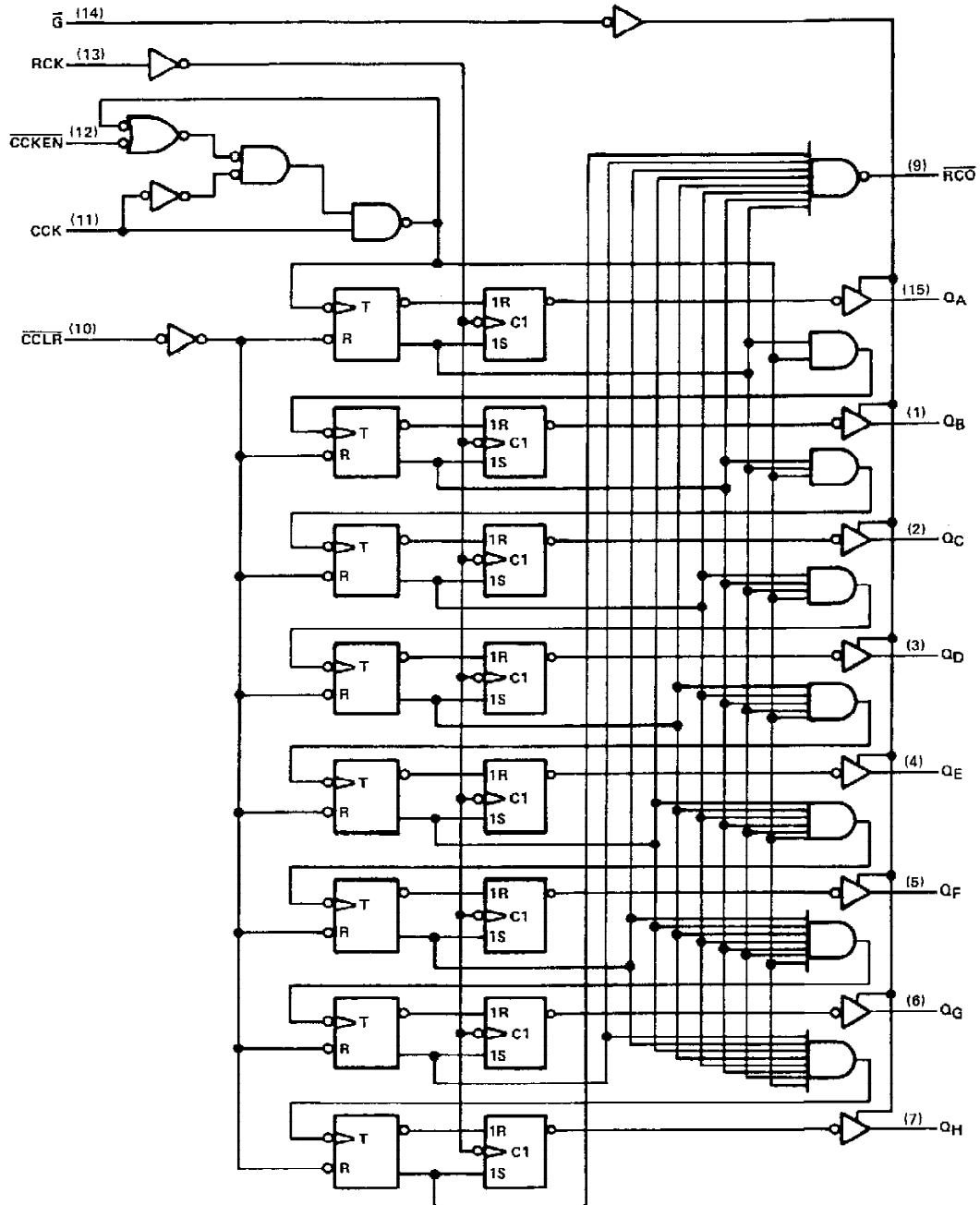


PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



**SN54LS590, SN54LS591, SN74LS590, SN74LS591**  
**8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS**

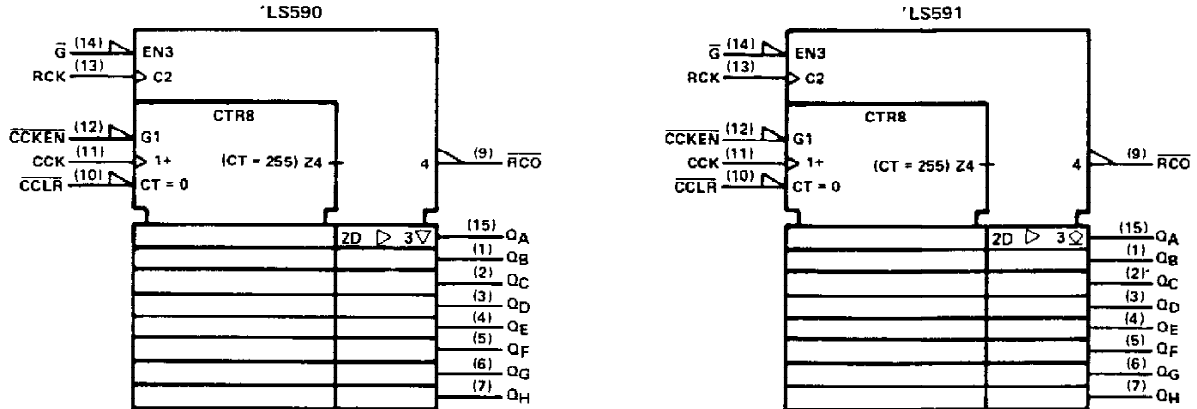
logic diagram (positive logic)



Pin numbers shown are for J, N and W packages.

**SN54LS590, SN54LS591, SN74LS590, SN74LS591**  
**8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS**

**logic symbols†**



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for J, N, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V <sub>CC</sub> (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS590, SN54LS591	-55°C to 125°C
SN74LS590, SN74LS591	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

**recommended operating conditions**

		SN54LS <sup>†</sup>			SN74LS <sup>†</sup>			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V
V <sub>OH</sub>	High-level output voltage	Q, 'LS591 only		5.5	5.5		V	
I <sub>OH</sub>	High-level output current	RCO		-1	-1		mA	
		Q, 'LS590 only		-1	-2.6			
I <sub>OL</sub>	Low-level output current	RCO		8	16		mA	
		Q		12	24			
f <sub>CCK</sub>	Counter clock frequency	0	20	0	20		MHz	
f <sub>RCK</sub>	Register clock frequency	0	25	0	25		MHz	
t <sub>w(CCK)</sub>	Duration of counter clock pulse	25		25			ns	
t <sub>w(CCLR)</sub>	Duration of counter clear pulse	20		20			ns	
t <sub>w(RCK)</sub>	Duration of register clock pulse	20		20			ns	
t <sub>su</sub>	Setup time	CCKEN low before CCK ↑		20	20		ns	
		CCLR inactive before CCK ↑		20	20			
		CCK before RCK ↑ (see Note 2)		40	40			
t <sub>h</sub>	Hold time	CCKEN low after CCK ↑		0	0		ns	
T <sub>A</sub>	Operating free-air temperature	-55	125	0	70		°C	

NOTE 2: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

**SN54LS590, SN54LS591, SN74LS590, SN74LS591**  
**8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT		
		MIN	TYP‡	MIN	TYP‡		MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5		-1.5		V		
V <sub>OH</sub>	'LS590 Q R <sub>CO</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OH</sub> = -1 mA				V	
			I <sub>OH</sub> = -2.6 mA		2.4 3.1			
			I <sub>OH</sub> = -1 mA		2.4 3.2			
I <sub>OH</sub>	'LS591 Q	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>OH</sub> = 5.5 V, V <sub>IL</sub> = MAX	0.1		0.1		mA	
V <sub>OL</sub>	Q R <sub>CO</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OL</sub> = 12 mA		0.25 0.4		V	
			I <sub>OL</sub> = 24 mA		0.35 0.5			
			I <sub>OL</sub> = 8 mA		0.25 0.4			
			I <sub>OL</sub> = 16 mA		0.35 0.5			
I <sub>OZH</sub>	'LS590 Q	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 2.7 V, V <sub>IL</sub> = MAX	20		20		μA	
I <sub>OZL</sub>	'LS590 Q	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 0.4 V, V <sub>IL</sub> = MAX	-20		-20		μA	
I <sub>I</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V	0.1		0.1		mA	
I <sub>IH</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	20		20		μA	
I <sub>IL</sub>	CCK	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-0.8		-0.8		mA	
	All others		-0.2		-0.2			
I <sub>OS</sub> §	'LS590 Q	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0 V	-30 -130		-30 -130		mA	
	R <sub>CO</sub>		-20 -100		-20 -100			
I <sub>CC</sub>	'LS590	V <sub>CC</sub> = MAX, All possible inputs grounded, All outputs open	I <sub>CCH</sub>	33 55		33 55		mA
			I <sub>CCL</sub>	44 65		44 65		
			I <sub>CCZ</sub>	46 65		46 65		
	'LS591		I <sub>CCH</sub>	35 55		35 55		
			I <sub>CCL</sub>	42 65		42 65		
			I <sub>CCZ</sub>					

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS590			'LS591			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>	R <sub>CK</sub>	Q	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF	20	35		20	35		MHz
t <sub>PLH</sub>	CCK↑	R <sub>CO</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 30 pF	14	22		16	24		ns
t <sub>PHL</sub>	CCK↑	R <sub>CO</sub>		20	30		25	38		ns
t <sub>PLH</sub>	CCLR↓	R <sub>CO</sub>		30	45		32	48		ns
t <sub>PLH</sub>	R <sub>CK</sub> ↑	Q	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF	12	18		25	38		ns
t <sub>PHL</sub>	R <sub>CK</sub> ↑	Q		22	33		28	42		ns
t <sub>PZH</sub>	G <sub>↓</sub>	Q		25	38					ns
t <sub>PZL</sub>	G <sub>↓</sub>	Q		30	45					ns
t <sub>PHZ</sub>	G <sub>↑</sub>	Q	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF	20	30					ns
t <sub>PLZ</sub>	G <sub>↑</sub>	Q		25	38					ns
t <sub>PLH</sub>	G <sub>↑</sub>	Q					34	50		ns
t <sub>PHL</sub>	G <sub>↓</sub>	Q	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF				32	48		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87517012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87517012A SNJ54LS590FK	Samples
5962-8751701EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J	Samples
5962-8751701EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J	Samples
SN54LS590J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS590J	Samples
SN54LS590J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS590J	Samples
SN74LS590D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS590	Samples
SN74LS590D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS590	Samples
SN74LS590DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS590DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS590DRE4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS590DRE4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS590DRG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS590DRG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS590N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS590N	Samples
SN74LS590N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS590N	Samples
SN74LS590N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS590N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS590NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS590	Samples
SN74LS590NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS590	Samples
SNJ54LS590FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87517012A	Samples



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54LS590FK	
SNJ54LS590FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87517012A SNJ54LS590FK	Samples
SNJ54LS590J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J	Samples
SNJ54LS590J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



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**OTHER QUALIFIED VERSIONS OF SN54LS590, SN74LS590 :**

- Catalog: [SN74LS590](#)
- Military: [SN54LS590](#)

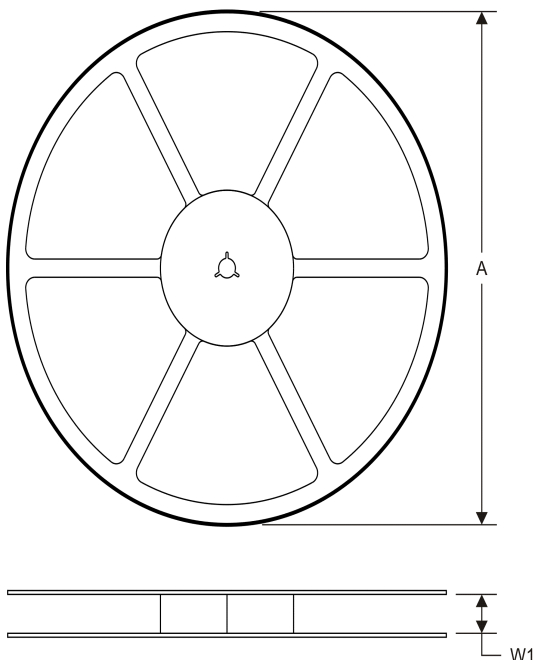
**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

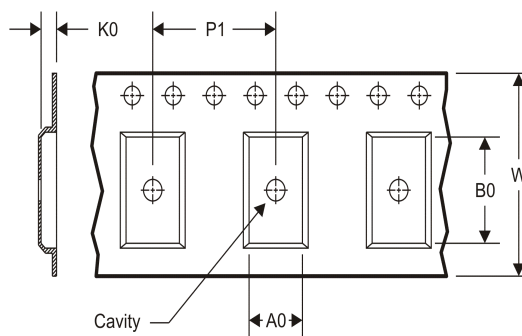


**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS590NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



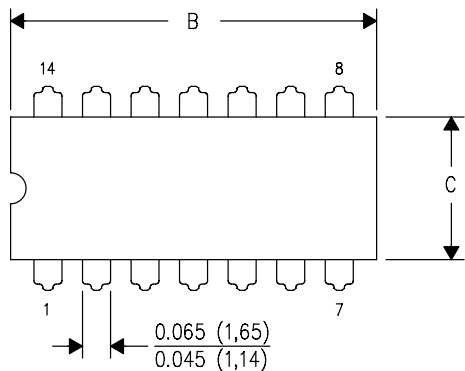
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS590NSR	SO	NS	16	2000	367.0	367.0	38.0

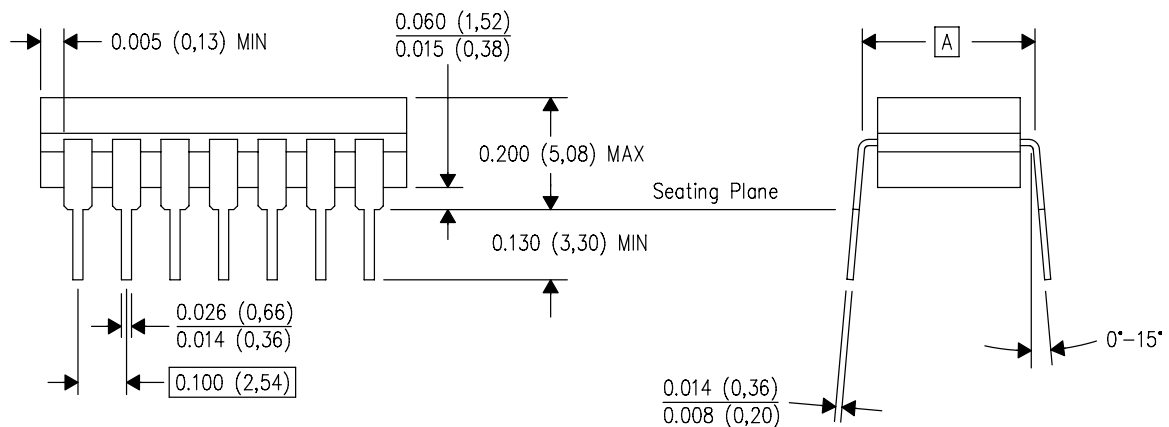
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



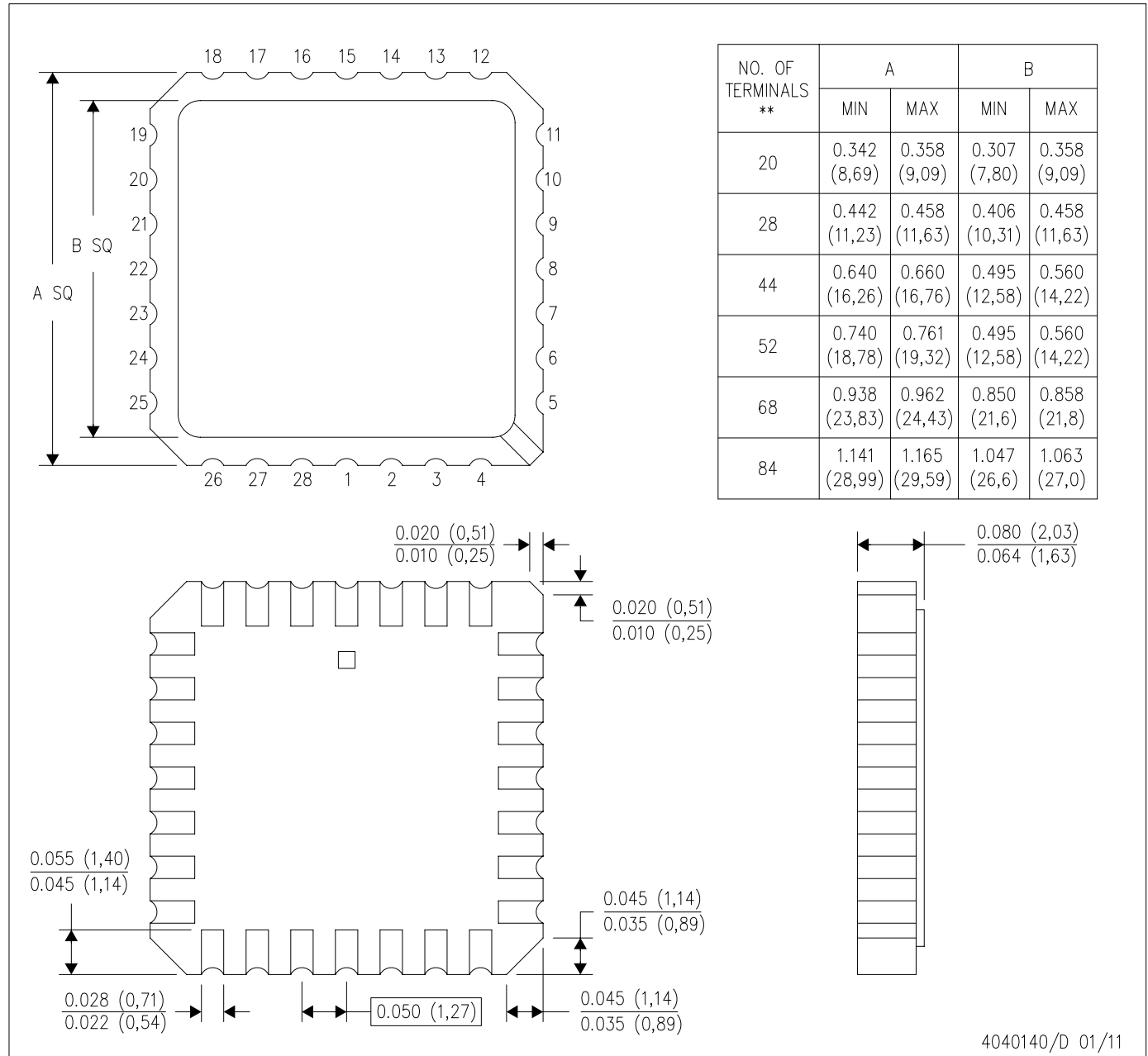
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 01/11

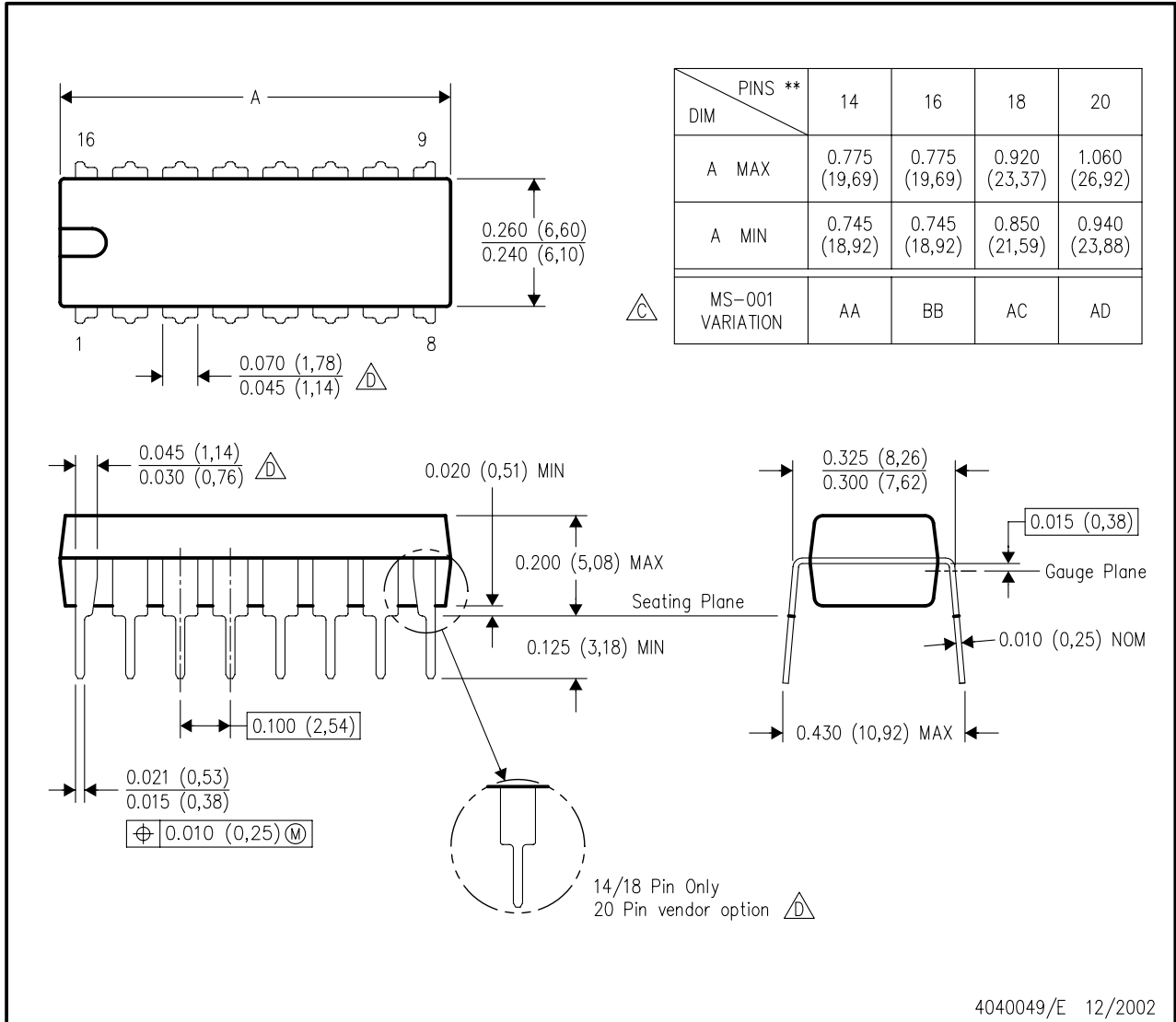
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

**MECHANICAL DATA**

**N (R-PDIP-T\*\*)**

16 PINS SHOWN

**PLASTIC DUAL-IN-LINE PACKAGE**



4040049/E 12/2002

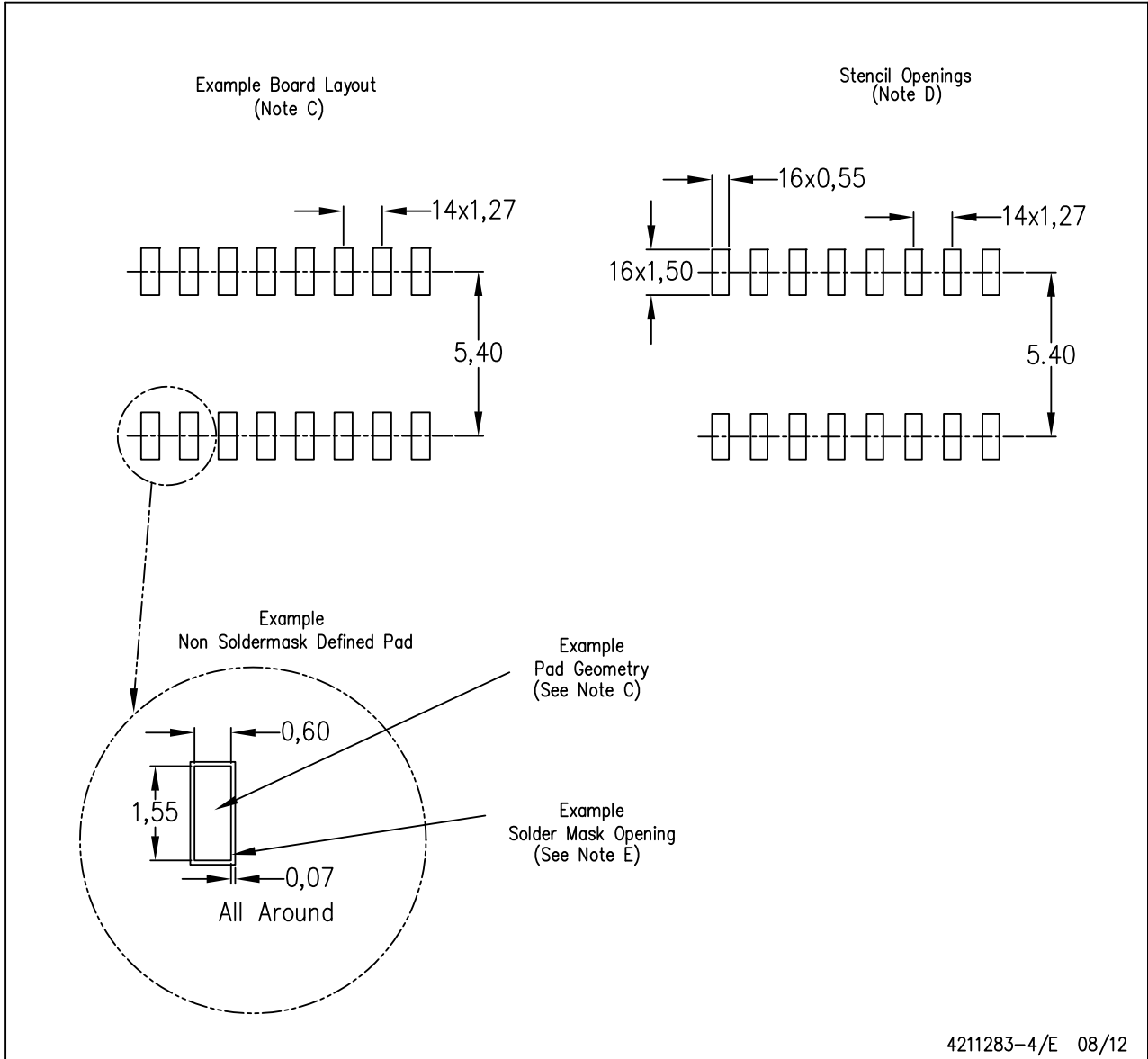
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



**LAND PATTERN DATA**

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



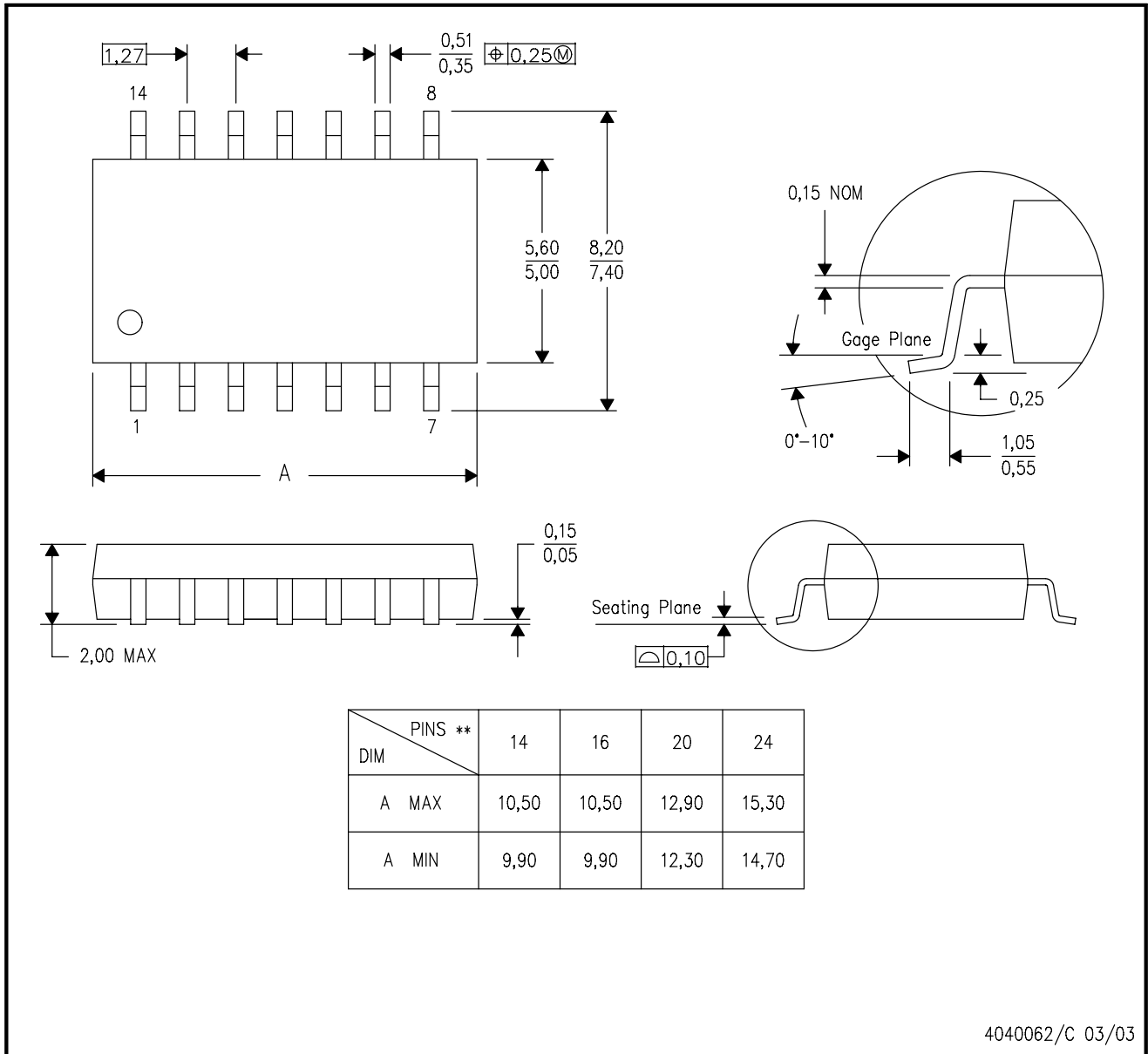
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**MECHANICAL DATA**

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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