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[Texas Instruments](#)  
[SN74CBT16232DGGR](#)

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## FEATURES

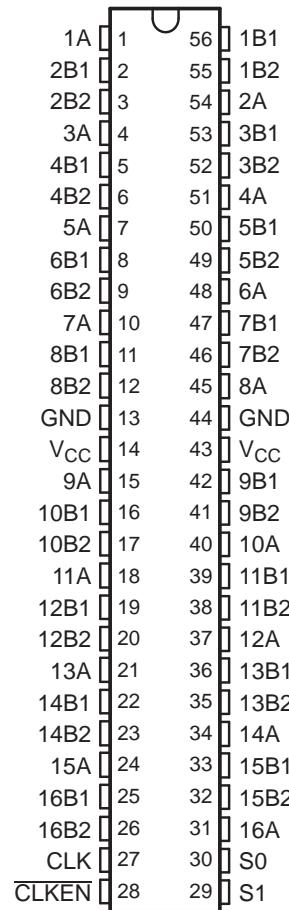
- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels

## DESCRIPTION/ ORDERING INFORMATION

The SN74CBT16232 is a synchronous 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path.

Two select (S0 and S1) inputs control the data flow. A clock (CLK) and a clock enable (CLKEN) synchronize the device operation. When CLKEN is high, the bus switch remains in the last clocked function.

**DGG OR DL PACKAGE  
(TOP VIEW)**



## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT16232DL	CBT16232
		Tape and reel	SN74CBT16232DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16232DGGR	CBT16232

- 1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).
- 2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



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## SN74CBT16232

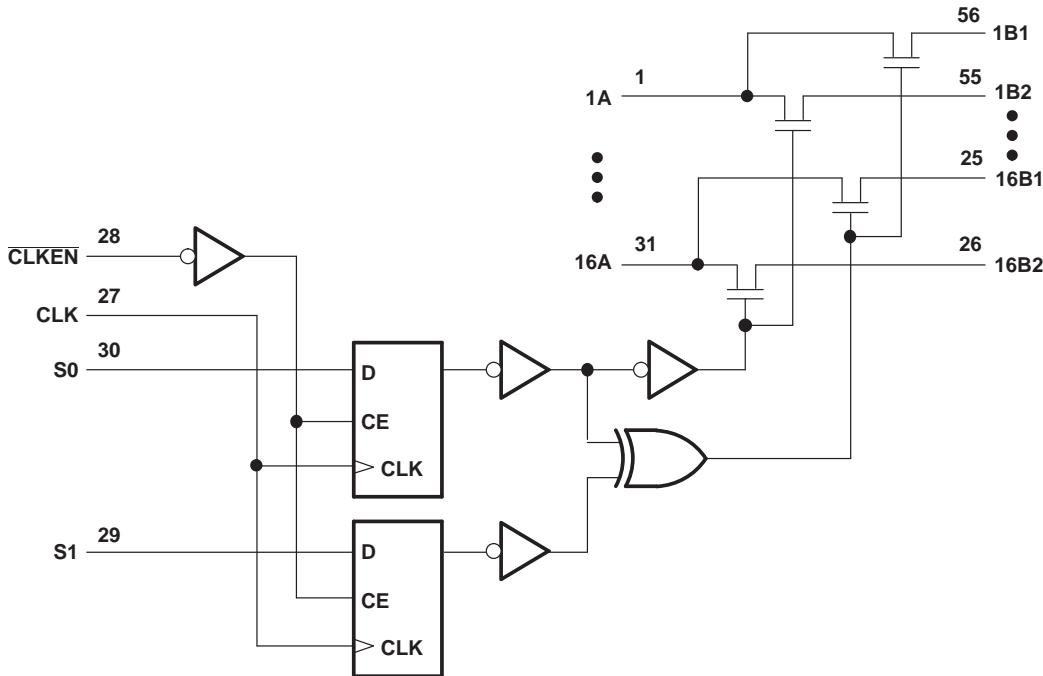
### SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS009N – MAY 1995 – REVISED JUNE 2007

#### FUNCTION TABLE

INPUTS				FUNCTION
S1	S0	CLK	$\bar{CLKEN}$	
X	X	X	H	Last state
L	L	↑	L	Disconnect
L	H	↑	L	A = B1 and A = B2
H	L	↑	L	A = B1
H	H	↑	L	A = B2

#### LOGIC DIAGRAM (POSITIVE LOGIC)



#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
	Continuous channel current		128	mA
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DGG package	64	°C/W
			56	
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$T_A$	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5$ V, $I_I = -18$ mA					-1.2	V
$I_I$		$V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND					±1	µA
$I_{CC}$		$V_{CC} = 5.5$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND					3	µA
$\Delta I_{CC}$ <sup>(2)</sup>	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND					2.5	mA
$C_I$	Control inputs	$V_I = 3$ V or 0					4.5	pF
$C_{io(OFF)}$	A port	$V_O = 3$ V or 0, $\overline{CLKEN} = 0$ , S0 and S1 = GND				6.5		pF
	B port					4		
$r_{on}$ <sup>(3)</sup>		$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V	$V_I = 2.4$ V, $I_I = 15$ mA			14	20	Ω
		$V_{CC} = 4.5$ V	$V_I = 0$	$I_I = 64$ mA		5	7	
				$I_I = 30$ mA		5	7	
			$V_I = 2.4$ V, $I_I = 15$ mA			10	15	

(1) All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(2) This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			$V_{CC} = 4$ V		$V_{CC} = 5$ V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency			150		150	MHz
$t_w$	Pulse duration	CLK high or low	3.3		3.3		ns
$t_{su}$	Setup time	S0, S1 before $CLK\uparrow$	2.2		1.9		ns
		$\overline{CLKEN}$ before $CLK\uparrow$	2.4		1.9		
$t_h$	Hold time	S0, S1 after $CLK\uparrow$	0.5		1		ns
		$\overline{CLKEN}$ after $CLK\uparrow$	1.9		1.8		

## SN74CBT16232

### SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS009N – MAY 1995 – REVISED JUNE 2007

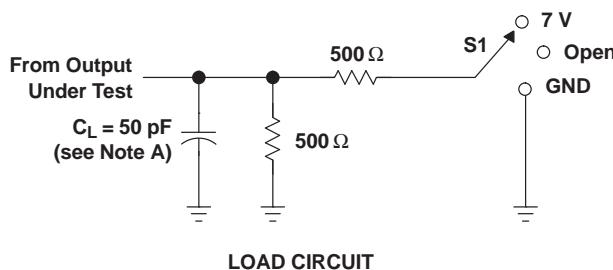
#### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

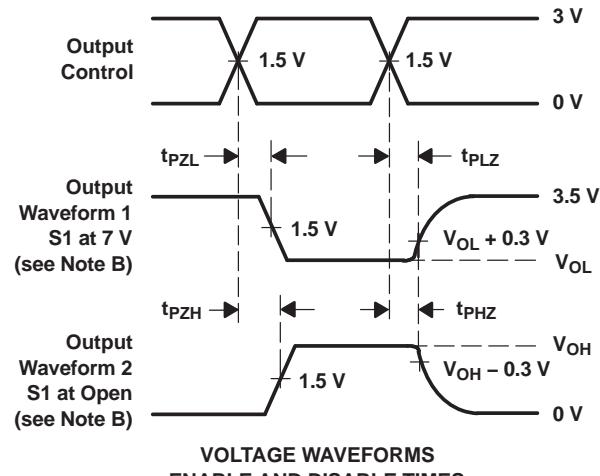
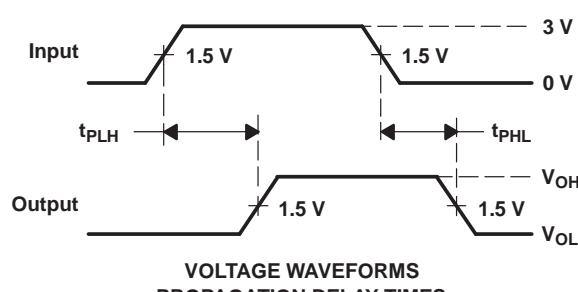
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			150		150		MHz
$t_{pd}^{(1)}$	A or B	B or A		0.35		0.25	ns
$t_{pd}$	CLK	A or B		6.7	2	5.8	ns
$t_{en}$	CLK	A, B1, B2		7.2	1.8	6.2	ns
		B1 and B2		8.5	3.1	7.9	
$t_{dis}$	CLK	A or B		6.3	1.9	6.2	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- The outputs are measured one at a time with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CBT16232DGGR4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16232DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

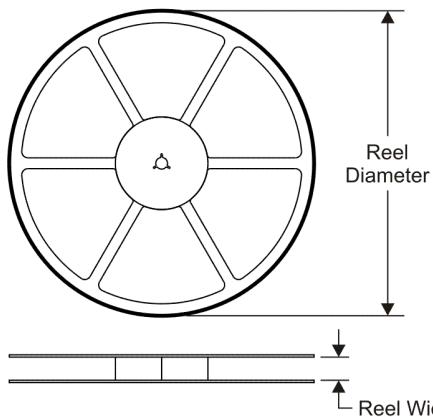
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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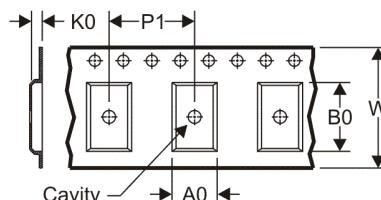
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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

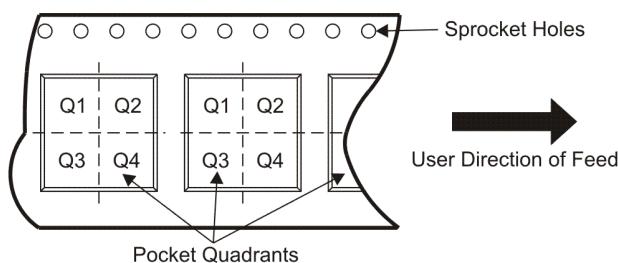


**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

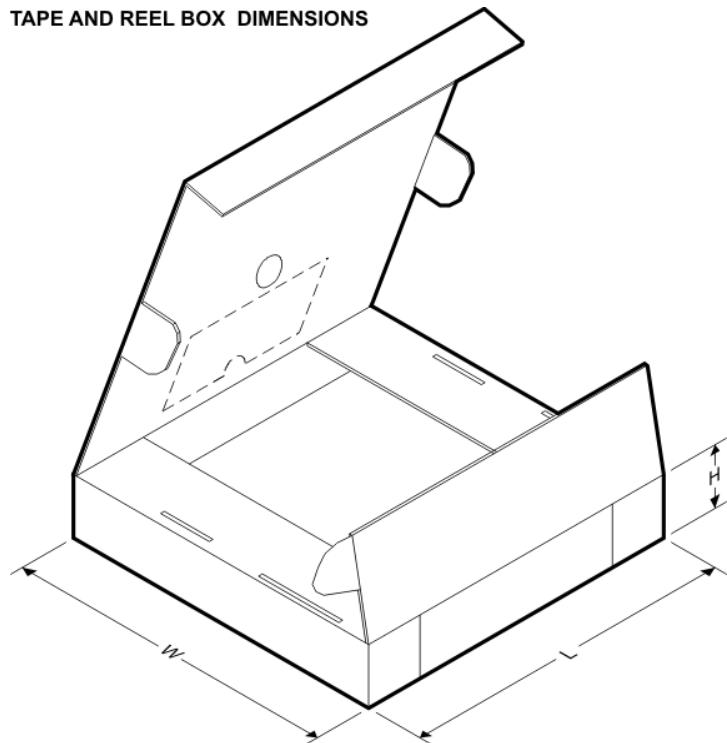
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16232DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBT16232DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

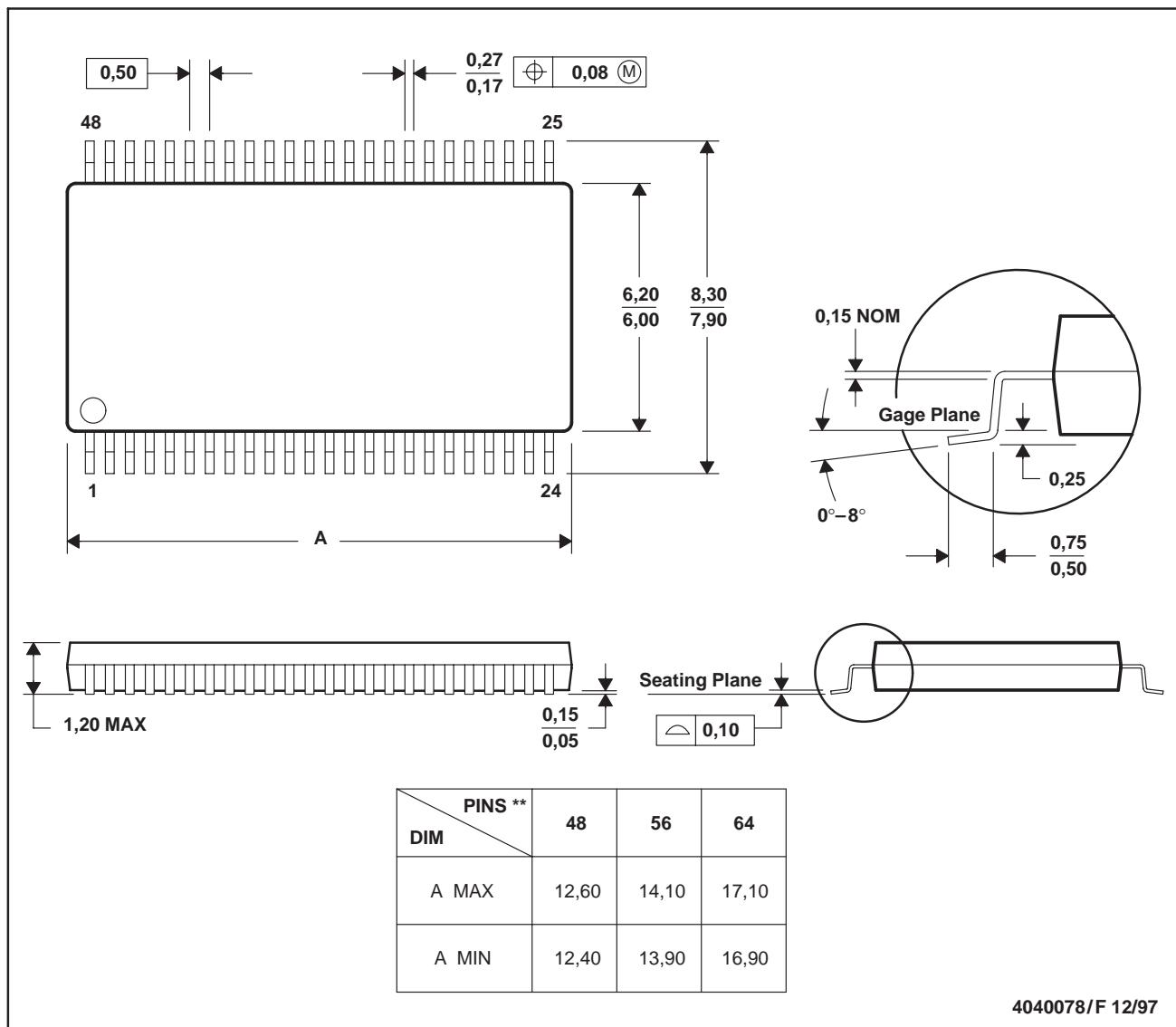
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16232DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74CBT16232DLR	SSOP	DL	56	1000	346.0	346.0	49.0

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

**DGG (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



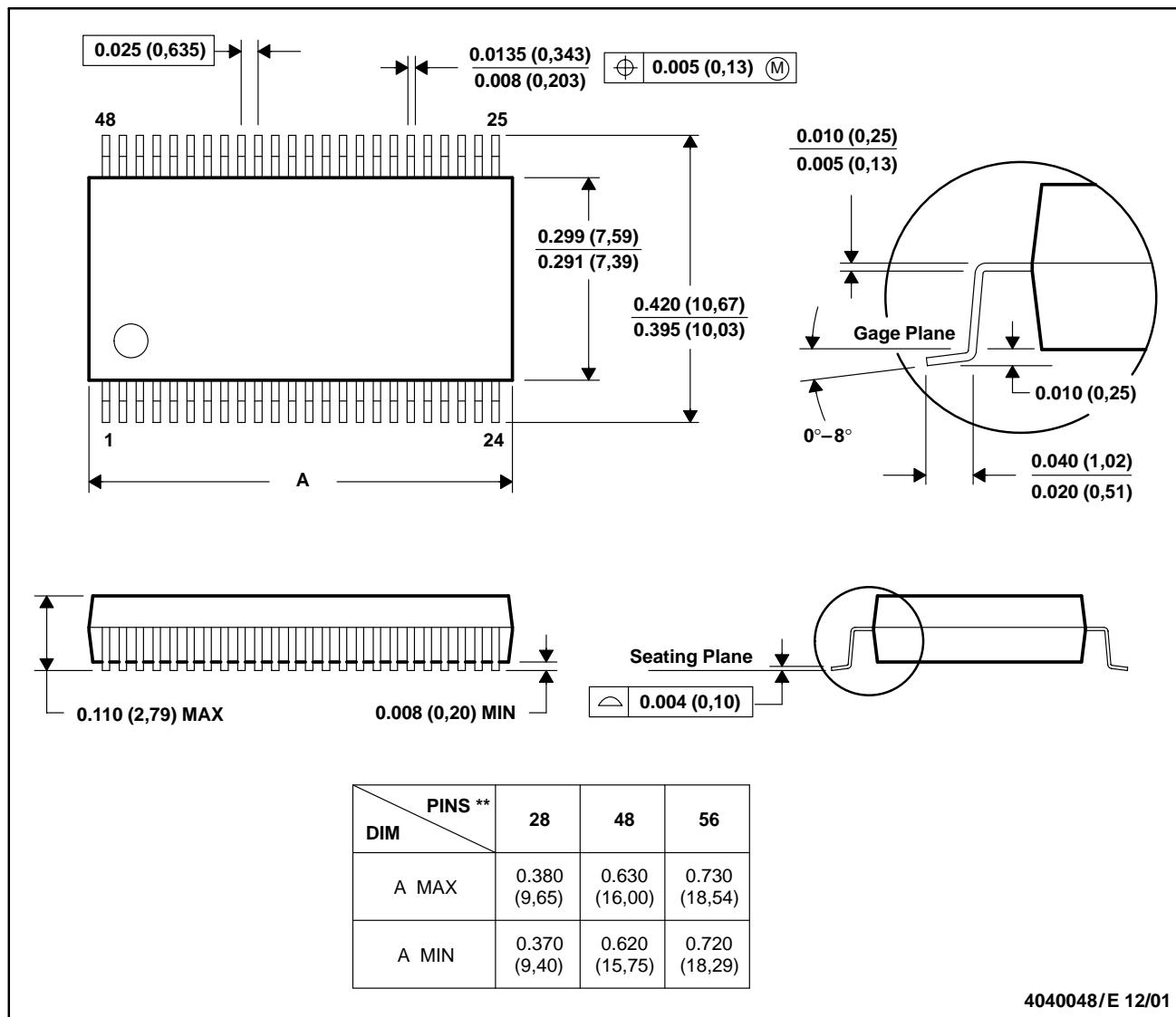
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

MSS001C – JANUARY 1995 – REVISED DECEMBER 2001

**DL (R-PDSO-G\*\*)**

48 PINS SHOWN

**PLASTIC SMALL-OUTLINE PACKAGE**



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 D. Falls within JEDEC MO-118

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