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bq4014/bq4014Y

256Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Industry-standard 32-pin 256K x 8 pinout
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4014 is a nonvolatile 2,097,152-bit static RAM organized as 262,144 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

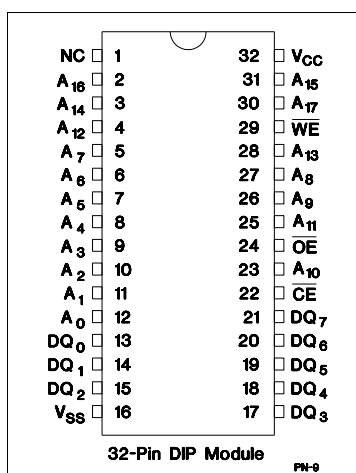
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation. At this time the integral energy

source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4014 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4014 requires no external circuitry and is compatible with the industry-standard 2Mb SRAM pinout.

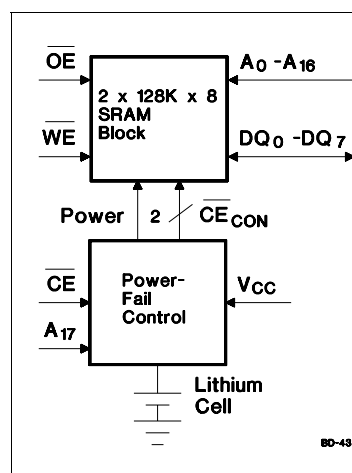
Pin Connections



Pin Names

A ₀ -A ₁₇	Address inputs
DQ ₀ -DQ ₇	Data input/output
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{OE}}$	Output enable input
$\overline{\text{WE}}$	Write enable input
NC	No connect
V _{CC}	+5 volt supply input
V _{SS}	Ground

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4014 -85	85	-5%	bq4014Y -85	85	-10%
bq4014 -120	120	-5%	bq4014Y -120	120	-10%

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Functional Description

When power is valid, the bq4014 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4014 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the VCC supply for a power-fail-detect threshold V_{PFD} . The bq4014 monitors for $V_{PFD} = 4.62V$ typical for use in systems with 5% supply tolerance. The bq4014Y monitors for $V_{PFD} = 4.37V$ typical for use in systems with 10% supply tolerance.

When VCC falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT} , write-protection takes place.

As VCC falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid VCC is applied.

When VCC returns to a level above the internal backup cell voltage, the supply is switched back to VCC. After VCC ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4014 have an extremely long shelf life and provide data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of VCC, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	\overline{CE}	\overline{WE}	\overline{OE}	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D _{OUT}	Active
Write	L	L	X	D _{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V _{CC}	DC voltage applied on VCC relative to VSS	-0.3 to 7.0	V	
V _T	DC voltage applied on any pin excluding VCC relative to VSS	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
T _{OPR}	Operating temperature	0 to +70	°C	
T _{STG}	Storage temperature	-40 to +70	°C	
T _{BIAS}	Temperature under bias	-10 to +70	°C	
T _{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

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Recommended DC Operating Conditions ($T_A = 0$ to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4014Y
		4.75	5.0	5.5	V	bq4014
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	$V_{CC} + 0.3$	V	

Note: Typical values indicate operation at $T_A = 25^\circ\text{C}$.

DC Electrical Characteristics ($T_A = 0$ to 70°C , $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	μA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	μA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	$I_{OH} = -1.0$ mA
V_{OL}	Output low voltage	-	-	0.4	V	$I_{OL} = 2.1$ mA
I_{SB1}	Standby supply current	-	5	12	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	5	mA	$\overline{CE} \geq V_{CC} - 0.2\text{V}$, $0\text{V} \leq V_{IN} \leq 0.2\text{V}$, or $V_{IN} \geq V_{CC} - 0.2$
I_{CC}	Operating supply current	-	75	110	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O} = 0\text{mA}$, $A17 < V_{IL}$ or $A17 > V_{IH}$
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4014
		4.30	4.37	4.50	V	bq4014Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$.

Capacitance ($T_A = 25^\circ\text{C}$, $F = 1\text{MHz}$, $V_{CC} = 5.0\text{V}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	40	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	40	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

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AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

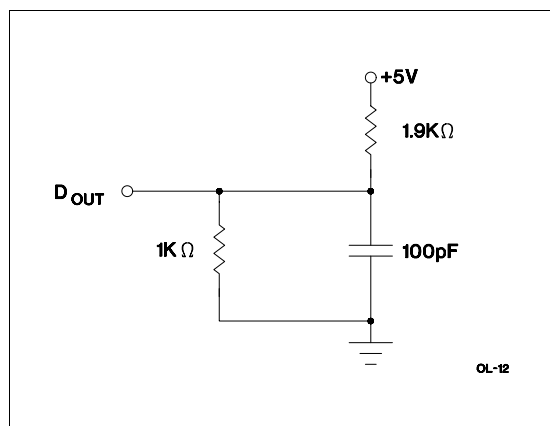


Figure 1. Output Load A

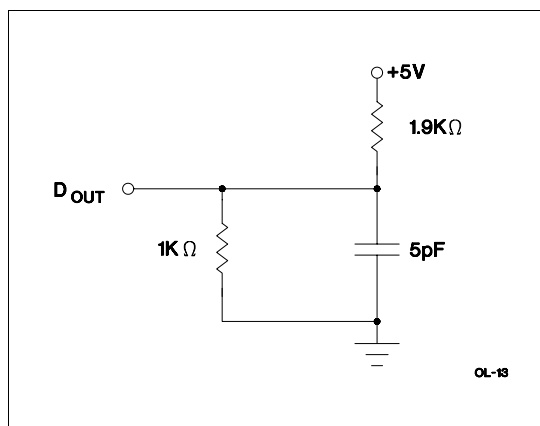


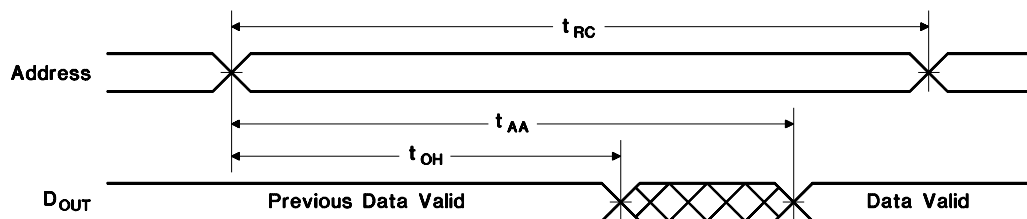
Figure 2. Output Load B

Read Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85		-120		Unit	Conditions
		Min.	Max.	Min.	Max.		
t _{RC}	Read cycle time	85	-	120	-	ns	
t _{AA}	Address access time	-	85	-	120	ns	Output load A
t _{ACE}	Chip enable access time	-	85	-	120	ns	Output load A
t _{OE}	Output enable to output valid	-	45	-	60	ns	Output load A
t _{CLZ}	Chip enable to output in low Z	5	-	5	-	ns	Output load B
t _{OLZ}	Output enable to output in low Z	0	-	0	-	ns	Output load B
t _{CHZ}	Chip disable to output in high Z	0	35	0	45	ns	Output load B
t _{OHZ}	Output disable to output in high Z	0	25	0	35	ns	Output load B
t _{OH}	Output hold from address change	10	-	10	-	ns	Output load A

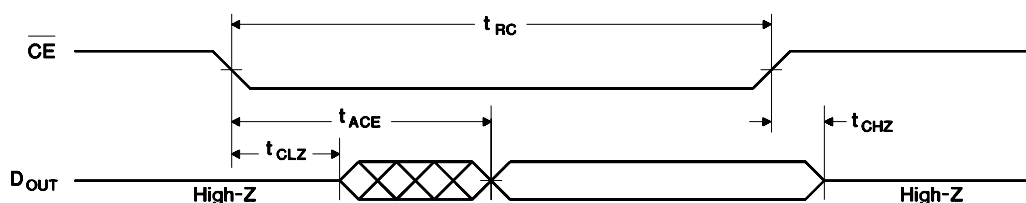
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Read Cycle No. 1 (Address Access) ^{1,2}



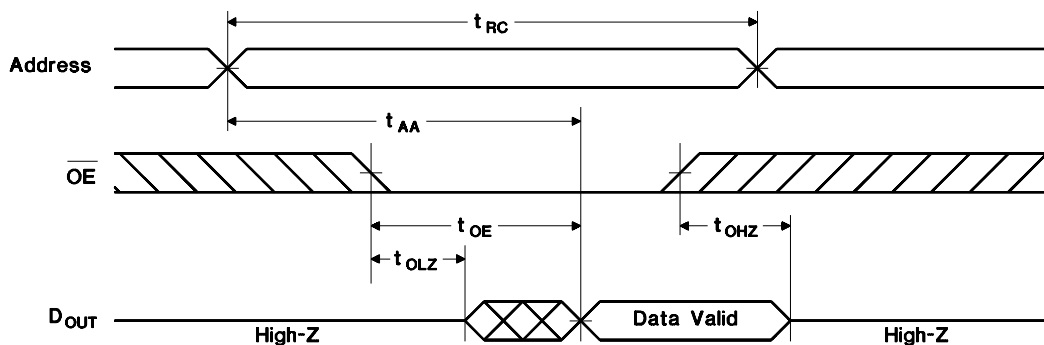
RC-1

Read Cycle No. 2 ($\overline{\text{CE}}$ Access) ^{1,3,4}



RC-2

Read Cycle No. 3 ($\overline{\text{OE}}$ Access) ^{1,5}



RC-3

- Notes:**
1. $\overline{\text{WE}}$ is held high for a read cycle.
 2. Device is continuously selected: $\overline{\text{CE}} = \overline{\text{OE}} = \text{V}_{\text{IL}}$.
 3. Address is valid prior to or coincident with $\overline{\text{CE}}$ transition low.
 4. $\overline{\text{OE}} = \text{V}_{\text{IL}}$.
 5. Device is continuously selected: $\overline{\text{CE}} = \text{V}_{\text{IL}}$.

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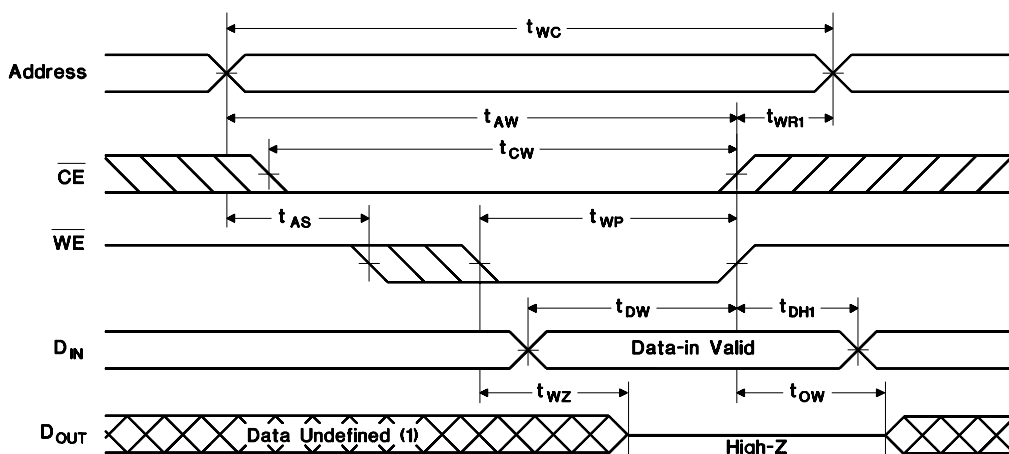
Write Cycle (TA = 0 to 70°C, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-85		-120		Units	Conditions/Notes
		Min.	Max.	Min.	Max.		
tWC	Write cycle time	85	-	120	-	ns	
tCW	Chip enable to end of write	75	-	100	-	ns	(1)
tAW	Address valid to end of write	75	-	100	-	ns	(1)
tAS	Address setup time	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
tWP	Write pulse width	65	-	85	-	ns	Measured from beginning of write to end of write. (1)
tWR1	Write recovery time (write cycle 1)	5	-	5	-	ns	Measured from \overline{WE} going high to end of write cycle. (3)
tWR2	Write recovery time (write cycle 2)	15	-	15	-	ns	Measured from \overline{CE} going high to end of write cycle. (3)
tDW	Data valid to end of write	35	-	45	-	ns	Measured to first low-to-high transition of either CE or WE.
tDH1	Data hold time (write cycle 1)	0	-	0	-	ns	Measured from \overline{WE} going high to end of write cycle. (4)
tDH2	Data hold time (write cycle 2)	10	-	10	-	ns	Measured from \overline{CE} going high to end of write cycle. (4)
tWZ	Write enabled to output in high Z	0	30	0	40	ns	I/O pins are in output state. (5)
tOW	Output active from end of write	0	-	0	-	ns	I/O pins are in output state. (5)

- Notes:**
1. A write ends at the earlier transition of \overline{CE} going high and \overline{WE} going high.
 2. A write occurs during the overlap of a low \overline{CE} and a low \overline{WE} . A write begins at the later transition of CE going low and WE going low.
 3. Either tWR1 or tWR2 must be met.
 4. Either tDH1 or tDH2 must be met.
 5. If \overline{CE} goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in high-impedance state.

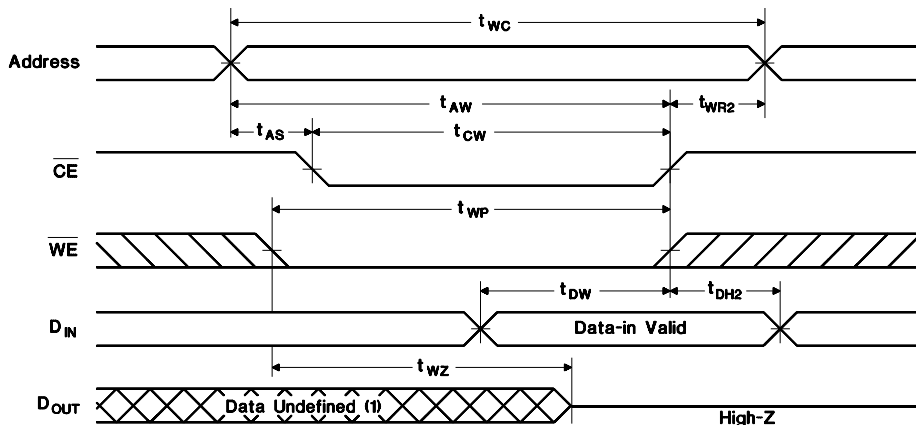
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Write Cycle No. 1 (WE-Controlled) ^{1,2,3}



WC-3

Write Cycle No. 2 (CE-Controlled) ^{1,2,3,4,5}



WC-4

- Notes:**
1. \overline{CE} or \overline{WE} must be high during address transition.
 2. Because I/O may be active (\overline{OE} low) during this period, data input signals of opposite polarity to the outputs must not be applied.
 3. If \overline{OE} is high, the I/O pins remain in a state of high impedance.
 4. Either t_{WR1} or t_{WR2} must be met.
 5. Either t_{DH1} or t_{DH2} must be met.

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Power-Down/Power-Up Cycle ($T_A = 0$ to 70°C)

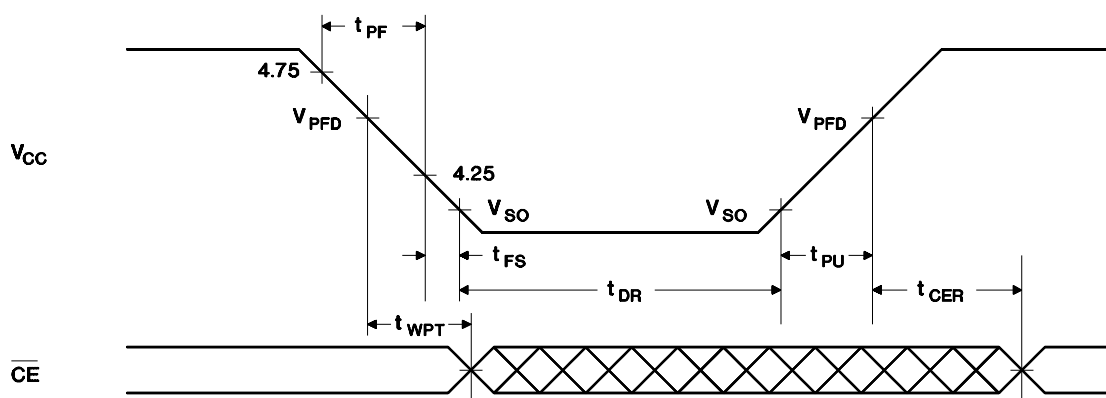
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	μs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	μs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	μs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	$T_A = 25^\circ\text{C}$. (2)
t_{WPT}	Write-protect time	40	100	150	μs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Notes: 1. Typical values indicate operation at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$.

2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing



PD-8

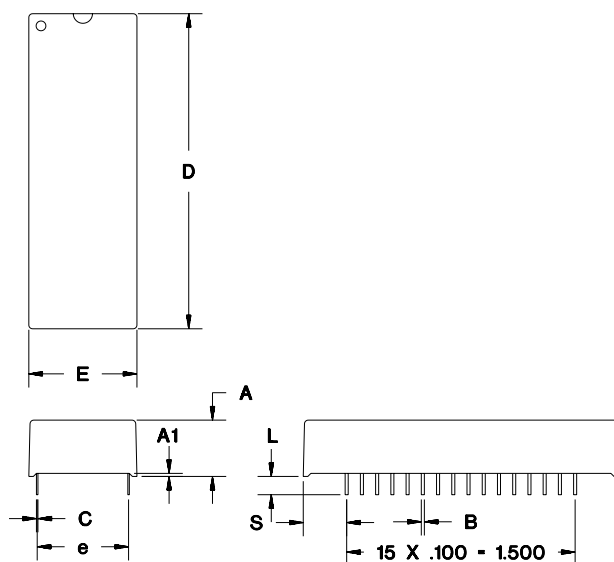
Sept. 1992

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Data Sheet Revision History (Sept. 1992 Changes From Sept. 1990)

Clarification of I_{CC} test conditions, page 3.

MB: 32-Pin B-Type Module



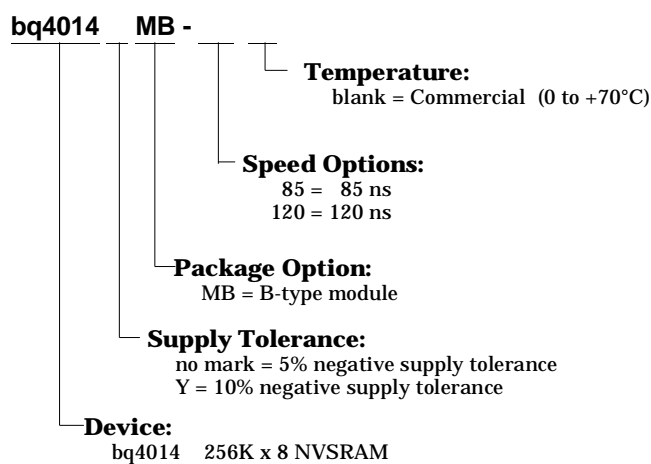
32-Pin MB (B-Type Module)

Dimension	Minimum	Maximum
A	0.365	0.375
A1	0.015	-
B	0.017	0.023
C	0.008	0.013
D	2.070	2.100
E	0.710	0.740
e	0.590	0.630
G	0.090	0.110
L	0.120	0.150
S	0.275	0.310

All dimensions are in inches.

bq4014/bq4014Y

Ordering Information





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ4014MB-120	OBSOLETE	DIP MODULE	MB	32		TBD	Call TI	Call TI	0 to 70		
BQ4014MB-85	OBSOLETE	DIP MODULE	MB	32		TBD	Call TI	Call TI	0 to 70		
BQ4014YMB-85	LIFEBUY	DIP MODULE	MB	32		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

5-Feb-2014

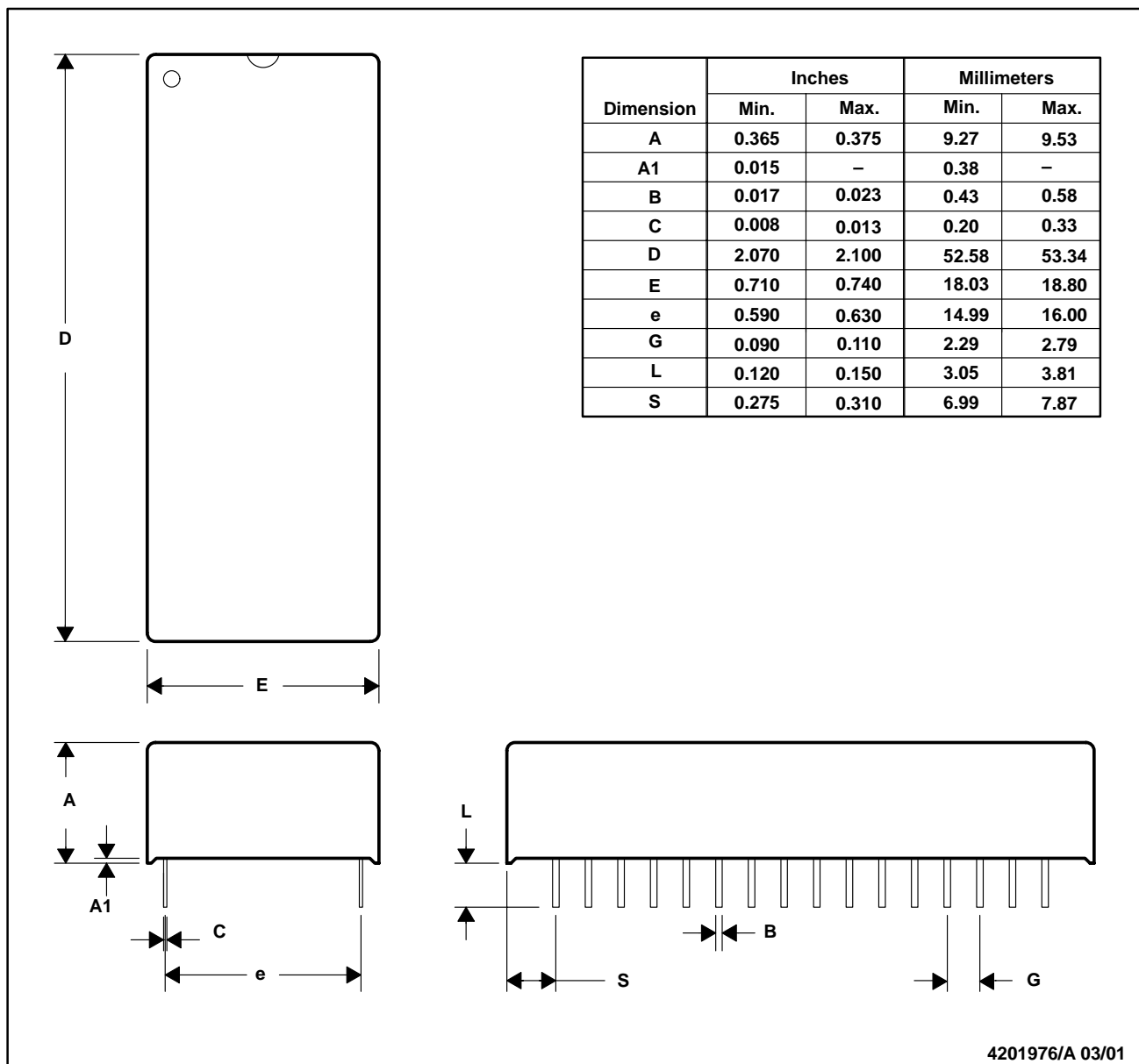
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MECHANICAL DATA

MPDI062 – MAY 2001

MB (R-PDIP-T32)

PLASTIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.



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