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[Texas Instruments](#)  
[SN74AVC16646DGVR](#)

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## FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- DOC™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With  $I_{OH}$  and  $I_{OL}$  of  $\pm 24$  mA at 2.5-V  $V_{CC}$

- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages

## DESCRIPTION

A Dynamic Output Control (DOC™) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

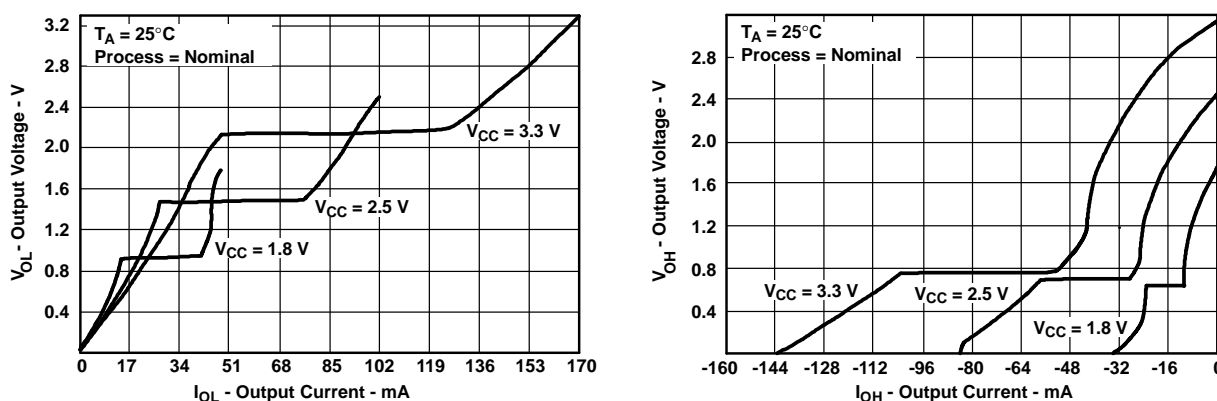


Figure 1. Output Voltage vs Output Current

This 16-bit bus transceiver and register is operational at 1.2-V to 3.6-V  $V_{CC}$ , but is designed specifically for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74AVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 2 illustrates the four fundamental bus-management functions that can be performed with the SN74AVC16646.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data.



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**SN74AVC16646**  
**16-BIT BUS TRANSCEIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

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**DESCRIPTION (CONTINUED)**

The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function still is enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

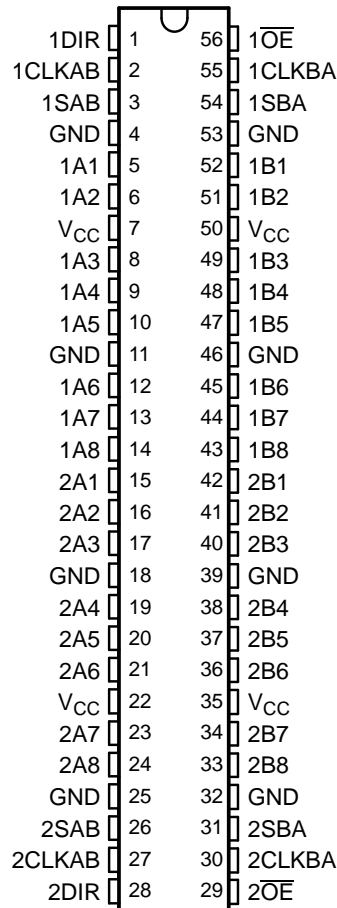
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC16646 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**TERMINAL ASSIGNMENTS**

**DGG OR DGV PACKAGE**  
**(TOP VIEW)**



**FUNCTION TABLE**  
**(EACH 8-BIT TRANSCIVER/REGISTER)**

| INPUTS          |     |        |        |     |     | DATA I/Os                  |                            | OPERATION OR FUNCTION                 |
|-----------------|-----|--------|--------|-----|-----|----------------------------|----------------------------|---------------------------------------|
| $\overline{OE}$ | DIR | CLKAB  | CLKBA  | SAB | SBA | A1-A8                      | B1-B8                      |                                       |
| X               | X   | ↑      | X      | X   | X   | Input                      | Unspecified <sup>(1)</sup> | Store A, B unspecified <sup>(1)</sup> |
| X               | X   | X      | ↑      | X   | X   | Unspecified <sup>(1)</sup> | Input                      | Store B, A unspecified <sup>(1)</sup> |
| H               | X   | ↑      | ↑      | X   | X   | Input                      | Input                      | Store A and B data                    |
| H               | X   | H or L | H or L | X   | X   | Input disabled             | Input disabled             | Isolation, hold storage               |
| L               | L   | X      | X      | X   | L   | Output                     | Input                      | Real-time B data to A bus             |
| L               | L   | X      | H or L | X   | H   | Output                     | Input                      | Stored B data to A bus                |
| L               | H   | X      | X      | L   | X   | Input                      | Output                     | Real-time A data to B bus             |
| L               | H   | H or L | X      | H   | X   | Input                      | Output                     | Stored A data to B bus                |

(1) The data-output functions may be enabled or disabled by various signals at  $\overline{OE}$  and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

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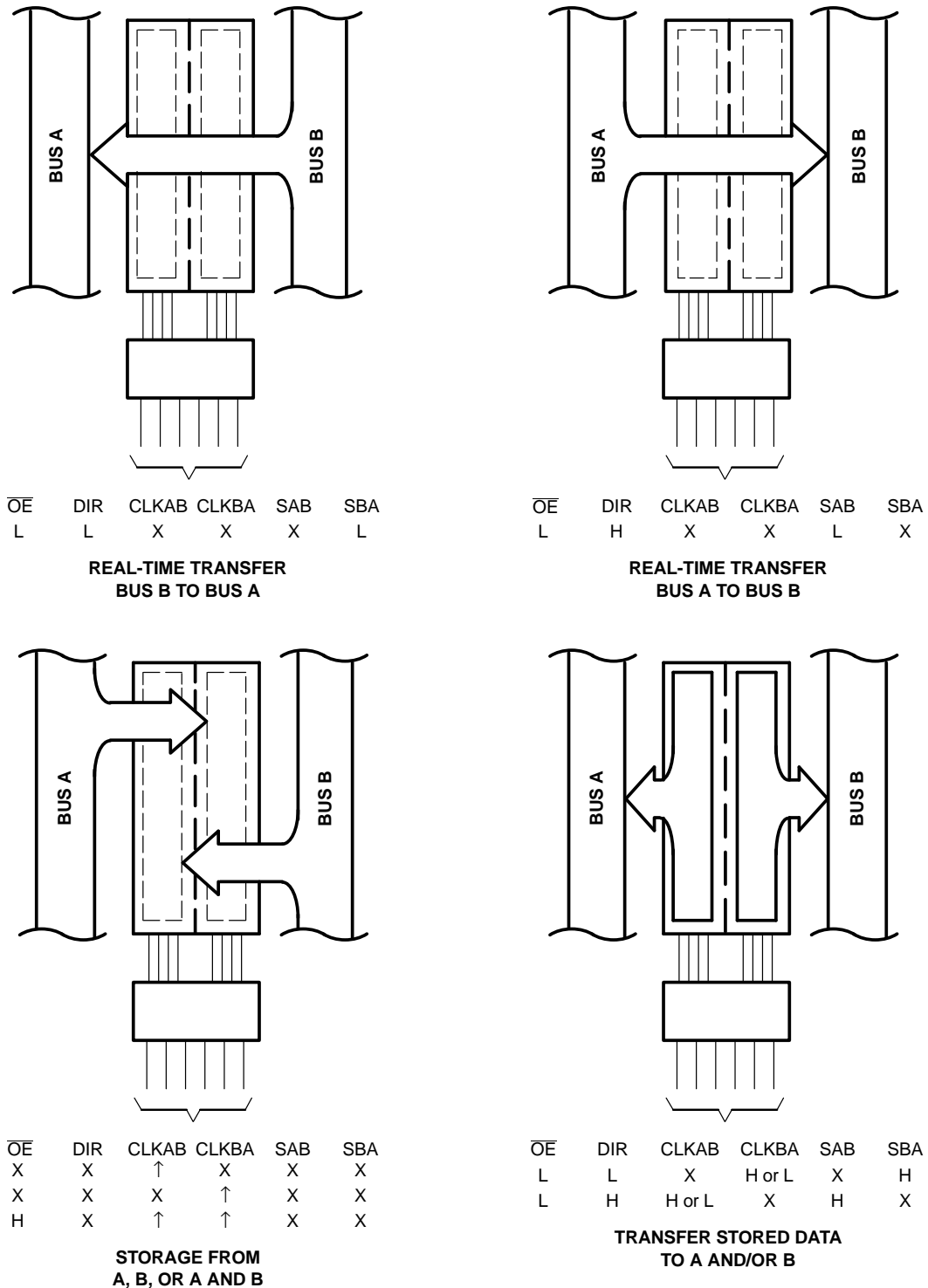
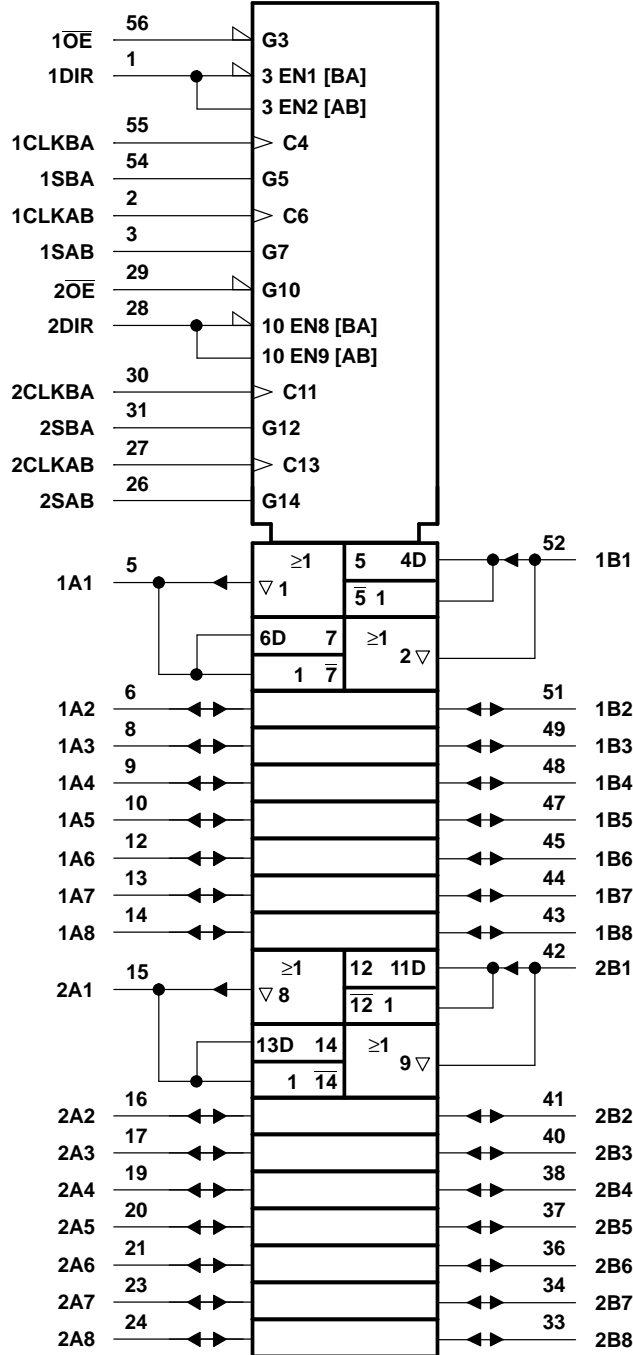


Figure 2. Bus-Management Functions

**LOGIC SYMBOL<sup>(1)</sup>**



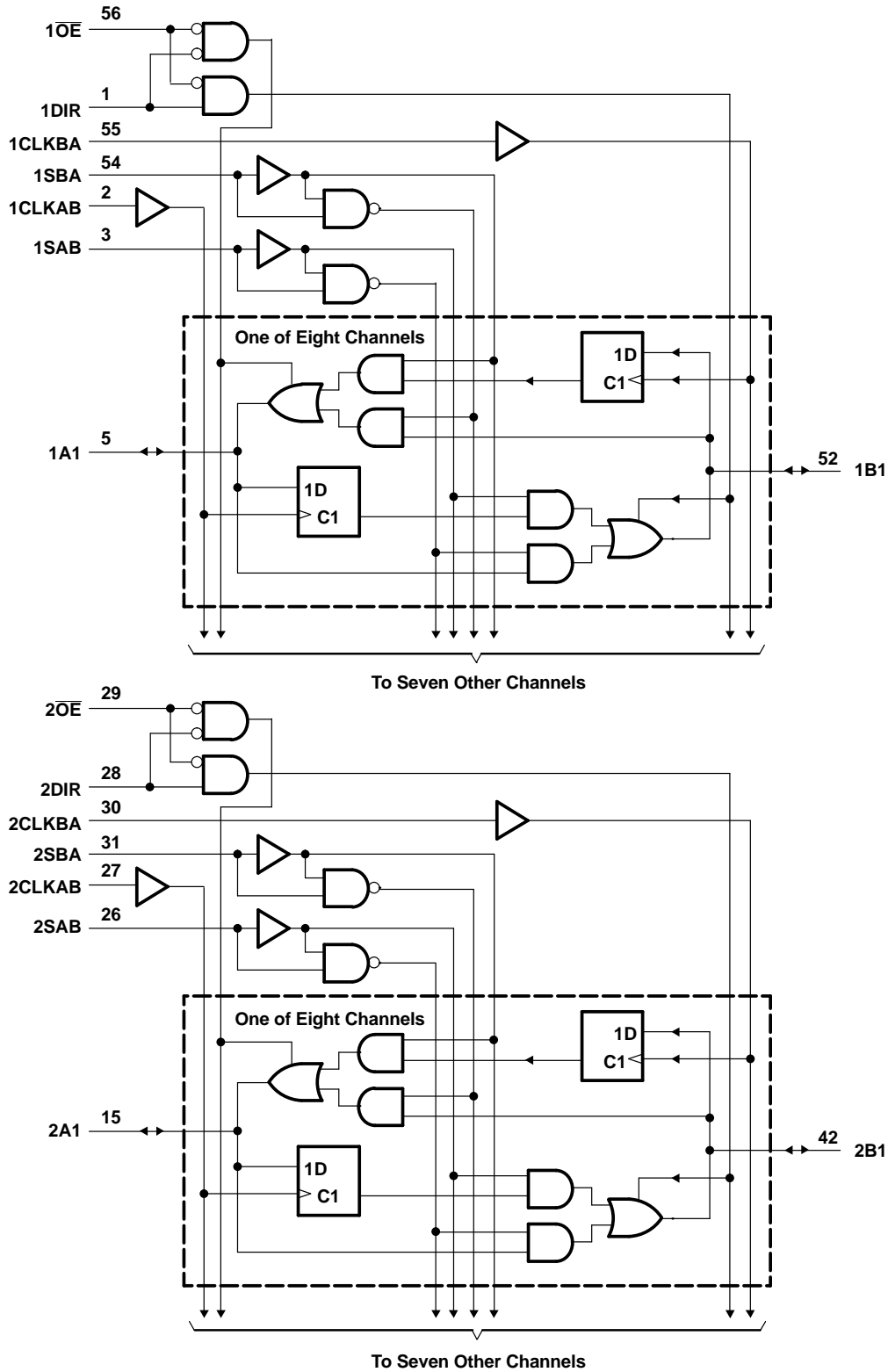
(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**LOGIC DIAGRAM (POSITIVE LOGIC)**



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |                                                                                                                      | MIN                | MAX                   | UNIT    |
|------------------|----------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------|---------|
| V <sub>CC</sub>  | Supply voltage range                                                                                                 | -0.5               | 4.6                   | V       |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                                                                                   | -0.5               | 4.6                   | V       |
| V <sub>O</sub>   | Voltage range applied to any input/output when the output is in the high-impedance or power-off state <sup>(2)</sup> | -0.5               | 4.6                   | V       |
| V <sub>O</sub>   | Voltage range applied to any input/output when the output is in the high or low state <sup>(2)(3)</sup>              | -0.5               | V <sub>CC</sub> + 0.5 | V       |
| I <sub>IK</sub>  | Input clamp current                                                                                                  | V <sub>I</sub> < 0 |                       | -50 mA  |
| I <sub>OK</sub>  | Output clamp current                                                                                                 | V <sub>O</sub> < 0 |                       | -50 mA  |
| I <sub>O</sub>   | Continuous output current                                                                                            |                    |                       | ±50 mA  |
|                  | Continuous current through each V <sub>CC</sub> or GND                                                               |                    |                       | ±100 mA |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(4)</sup>                                                                             | DGG package        |                       | 64 °C/W |
|                  |                                                                                                                      | DGV package        |                       | 48 °C/W |
| T <sub>stg</sub> | Storage temperature range                                                                                            | -65                | 150                   | °C      |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51.



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**16-BIT BUS TRANSCEIVER AND REGISTER**  
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**Recommended Operating Conditions<sup>(1)</sup>**

|                  |                                                 |                                    | MIN                    | MAX             | UNIT |
|------------------|-------------------------------------------------|------------------------------------|------------------------|-----------------|------|
| V <sub>CC</sub>  | Supply voltage                                  | Operating                          | 1.2                    | 3.6             | V    |
| V <sub>IH</sub>  | High-level input voltage                        | V <sub>CC</sub> = 1.2 V            | V <sub>CC</sub>        |                 | V    |
|                  |                                                 | V <sub>CC</sub> = 1.4 V to 1.6 V   | 0.65 × V <sub>CC</sub> |                 |      |
|                  |                                                 | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> |                 |      |
|                  |                                                 | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |                 |      |
|                  |                                                 | V <sub>CC</sub> = 3 V to 3.6 V     | 2                      |                 |      |
| V <sub>IL</sub>  | Low-level input voltage                         | V <sub>CC</sub> = 1.2 V            | GND                    |                 | V    |
|                  |                                                 | V <sub>CC</sub> = 1.4 V to 1.6 V   | 0.35 × V <sub>CC</sub> |                 |      |
|                  |                                                 | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.35 × V <sub>CC</sub> |                 |      |
|                  |                                                 | V <sub>CC</sub> = 2.3 V to 2.7 V   | 0.7                    |                 |      |
|                  |                                                 | V <sub>CC</sub> = 3 V to 3.6 V     | 0.8                    |                 |      |
| V <sub>I</sub>   | Input voltage                                   |                                    | 0                      | 3.6             | V    |
| V <sub>O</sub>   | Output voltage                                  | Active state                       | 0                      | V <sub>CC</sub> | V    |
|                  |                                                 | 3-state                            | 0                      | 3.6             |      |
| I <sub>OHS</sub> | Static high-level output current <sup>(2)</sup> | V <sub>CC</sub> = 1.4 V to 1.6 V   | –2                     |                 | mA   |
|                  |                                                 | V <sub>CC</sub> = 1.65 V to 1.95 V | –4                     |                 |      |
|                  |                                                 | V <sub>CC</sub> = 2.3 V to 2.7 V   | –8                     |                 |      |
|                  |                                                 | V <sub>CC</sub> = 3 V to 3.6 V     | –12                    |                 |      |
| I <sub>OLS</sub> | Static low-level output current <sup>(2)</sup>  | V <sub>CC</sub> = 1.4 V to 1.6 V   | 2                      |                 | mA   |
|                  |                                                 | V <sub>CC</sub> = 1.65 V to 1.95 V | 4                      |                 |      |
|                  |                                                 | V <sub>CC</sub> = 2.3 V to 2.7 V   | 8                      |                 |      |
|                  |                                                 | V <sub>CC</sub> = 3 V to 3.6 V     | 12                     |                 |      |
| Δt/Δv            | Input transition rise or fall rate              | V <sub>CC</sub> = 1.4 V to 3.6 V   | 5                      |                 | ns/V |
| T <sub>A</sub>   | Operating free-air temperature                  |                                    | –40                    | 85              | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Dynamic drive capability is equivalent to standard outputs with I<sub>OH</sub> and I<sub>OL</sub> of ±24 mA at 3.3-V V<sub>CC</sub>. See Figure 1 for V<sub>OL</sub> vs I<sub>OL</sub> and V<sub>OH</sub> vs I<sub>OH</sub> characteristics. Refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                      |                | TEST CONDITIONS                                                           | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX   | UNIT |
|--------------------------------|----------------|---------------------------------------------------------------------------|-----------------|-----------------------|--------------------|-------|------|
| V <sub>OH</sub>                |                | I <sub>OHS</sub> = -100 μA                                                | 1.2 V to 3.6 V  | V <sub>CC</sub> - 0.2 |                    |       | V    |
|                                |                | I <sub>OHS</sub> = -2 mA, V <sub>IH</sub> = 0.91 V                        | 1.4 V           | 1.05                  |                    |       |      |
|                                |                | I <sub>OHS</sub> = -4 mA, V <sub>IH</sub> = 1.07 V                        | 1.65 V          | 1.2                   |                    |       |      |
|                                |                | I <sub>OHS</sub> = -8 mA, V <sub>IH</sub> = 1.7 V                         | 2.3 V           | 1.75                  |                    |       |      |
|                                |                | I <sub>OHS</sub> = -12 mA, V <sub>IH</sub> = 2 V                          | 3 V             | 2.3                   |                    |       |      |
| V <sub>OL</sub>                |                | I <sub>OLS</sub> = 100 μA                                                 | 1.2 V to 3.6 V  |                       |                    | 0.2   | V    |
|                                |                | I <sub>OLS</sub> = 2 mA, V <sub>IL</sub> = 0.49 V                         | 1.4 V           |                       |                    | 0.4   |      |
|                                |                | I <sub>OLS</sub> = 4 mA, V <sub>IL</sub> = 0.57 V                         | 1.65 V          |                       |                    | 0.45  |      |
|                                |                | I <sub>OLS</sub> = 8 mA, V <sub>IL</sub> = 0.7 V                          | 2.3 V           |                       |                    | 0.55  |      |
|                                |                | I <sub>OLS</sub> = 12 mA, V <sub>IL</sub> = 0.8 V                         | 3 V             |                       |                    | 0.7   |      |
| I <sub>I</sub>                 | Control inputs | V <sub>I</sub> = V <sub>CC</sub> or GND                                   | 3.6 V           |                       |                    | ±2.5  | μA   |
| I <sub>off</sub>               |                | V <sub>I</sub> or V <sub>O</sub> = 3.6 V                                  | 0               |                       |                    | ±10   | μA   |
| I <sub>OZ</sub> <sup>(2)</sup> |                | V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> = V <sub>CC</sub> | 3.6 V           |                       |                    | ±12.5 | μA   |
| I <sub>CC</sub>                |                | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0               | 3.6 V           |                       |                    | 40    | μA   |
| C <sub>i</sub>                 | CLK inputs     | V <sub>I</sub> = V <sub>CC</sub> or GND                                   | 2.5 V           |                       |                    | 3     | pF   |
|                                |                |                                                                           | 3.3 V           |                       |                    | 3     |      |
|                                | Control inputs |                                                                           | 2.5 V           |                       |                    | 3.5   |      |
|                                |                |                                                                           | 3.3 V           |                       |                    | 3.5   |      |
| C <sub>io</sub>                | A or B ports   | V <sub>O</sub> = V <sub>CC</sub> or GND                                   | 2.5 V           |                       |                    | 8     | pF   |
|                                |                |                                                                           | 3.3 V           |                       |                    | 8     |      |

(1) Typical values are measured at T<sub>A</sub> = 25°C.

(2) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) through [Figure 6](#))

|                    |                 |                                    | V <sub>CC</sub> = 1.2 V |     | V <sub>CC</sub> = 1.5 V ± 0.1 V |     | V <sub>CC</sub> = 1.8 V ± 0.15 V |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |     | UNIT |
|--------------------|-----------------|------------------------------------|-------------------------|-----|---------------------------------|-----|----------------------------------|-----|---------------------------------|-----|---------------------------------|-----|------|
|                    |                 |                                    | MIN                     | MAX | MIN                             | MAX | MIN                              | MAX | MIN                             | MAX | MIN                             | MAX |      |
| f <sub>clock</sub> | Clock frequency |                                    |                         |     |                                 |     | 150                              |     | 250                             |     |                                 | 350 | MHz  |
| t <sub>w</sub>     | Pulse duration  | CLKAB or CLKBA high or low         |                         |     |                                 |     | 3.3                              |     | 2                               |     |                                 | 1.4 | ns   |
| t <sub>su</sub>    | Setup time      | A before CLKAB↑ or B before CLKBA↑ | 2.1                     |     | 1.6                             |     | 1.2                              |     | 0.9                             |     |                                 | 0.8 | ns   |
| t <sub>h</sub>     | Hold time       | A after CLKAB↑ or B after CLKBA↑   | 1.3                     |     | 1                               |     | 0.8                              |     | 0.6                             |     |                                 | 0.6 | ns   |

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## 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3 through Figure 6)

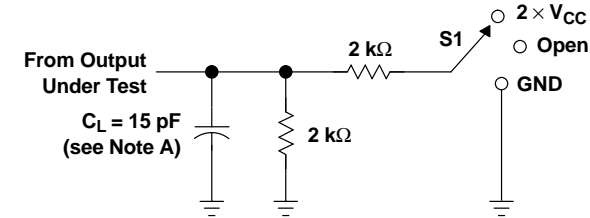
| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | $V_{CC} = 1.2\text{ V}$ | $V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$ |     | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | UNIT |
|-----------|-----------------|-------------|-------------------------|------------------------------------------|-----|-------------------------------------------|-----|------------------------------------------|-----|------------------------------------------|-----|------|
|           |                 |             | TYP                     | MIN                                      | MAX | MIN                                       | MAX | MIN                                      | MAX | MIN                                      | MAX |      |
| $f_{max}$ |                 |             |                         |                                          |     | 150                                       |     | 250                                      |     | 350                                      |     | MHz  |
| $t_{pd}$  | A or B          | B or A      | 4.2                     | 1.6                                      | 4.8 | 1.5                                       | 4.3 | 1.2                                      | 3.1 | 0.9                                      | 2.6 | ns   |
|           | CLKAB or CLKBA  | A or B      | 5.9                     | 2.2                                      | 7.4 | 1.9                                       | 6.1 | 1.3                                      | 4   | 1                                        | 3.3 |      |
|           | SAB or SBA      |             | 8.2                     | 2.6                                      | 10  | 2.4                                       | 6.3 | 1.8                                      | 5.1 | 1.5                                      | 4   |      |
| $t_{en}$  | $\overline{OE}$ | A or B      | 6.5                     | 2.2                                      | 8   | 1.9                                       | 7   | 1.4                                      | 4.6 | 1.1                                      | 4   | ns   |
| $t_{dis}$ | $\overline{OE}$ | A or B      | 6.7                     | 2.6                                      | 8   | 2.6                                       | 7.2 | 1.4                                      | 4.3 | 1.4                                      | 4.2 | ns   |
| $t_{en}$  | DIR             | A or B      | 6.9                     | 2.2                                      | 8.7 | 1.9                                       | 7.4 | 1.4                                      | 5   | 1.1                                      | 4.3 | ns   |
| $t_{dis}$ | DIR             | A or B      | 7.5                     | 2.6                                      | 8.7 | 2.6                                       | 7.6 | 1.4                                      | 4.5 | 1.4                                      | 4.3 | ns   |

### Operating Characteristics

$T_A = 25^\circ\text{C}$

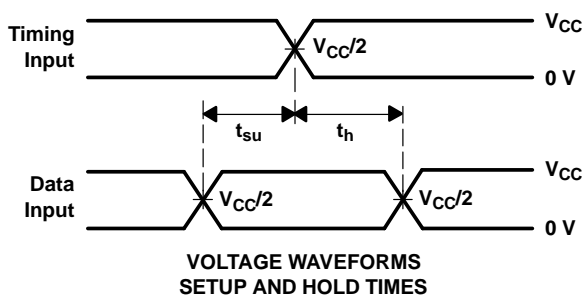
| PARAMETER                              |                  | TEST CONDITIONS              | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|----------------------------------------|------------------|------------------------------|-------------------------|-------------------------|-------------------------|------|
|                                        |                  |                              | TYP                     | TYP                     | TYP                     |      |
| $C_{pd}$ Power dissipation capacitance | Outputs enabled  | $C_L = 0, f = 10\text{ MHz}$ | 62                      | 73                      | 120                     | pF   |
|                                        | Outputs disabled |                              | 25                      | 29                      | 34                      |      |

**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 1.2\text{ V AND } 1.5\text{ V} \pm 0.1\text{ V}$

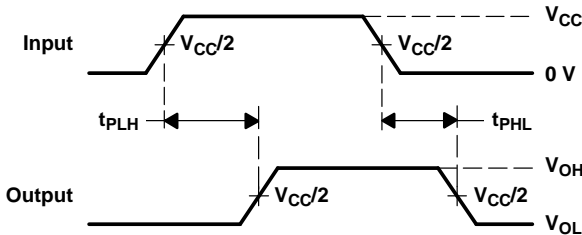


**LOAD CIRCUIT**

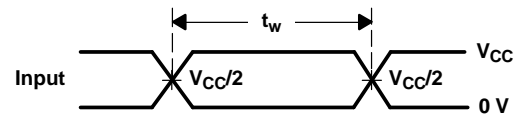
| TEST              | S1                |
|-------------------|-------------------|
| $t_{pd}$          | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |



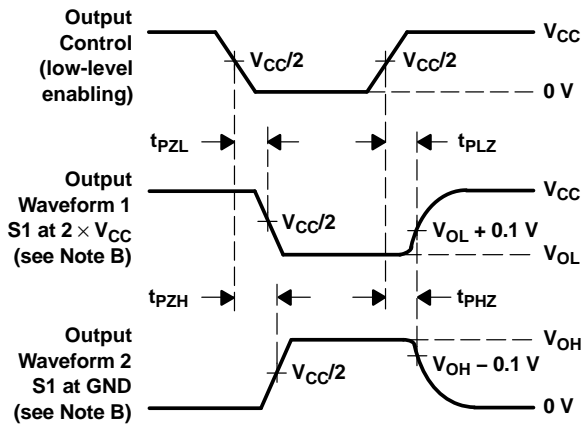
**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

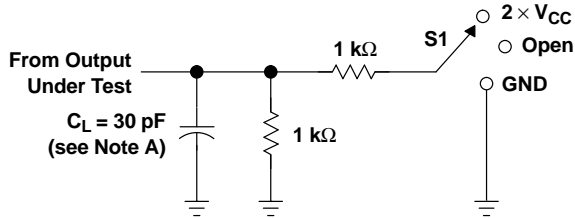
**Figure 3. Load Circuit and Voltage Waveforms**

**SN74AVC16646**  
**16-BIT BUS TRANSCIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

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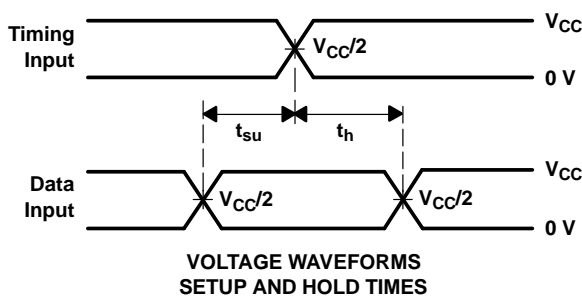
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 1.8 V \pm 0.15 V$

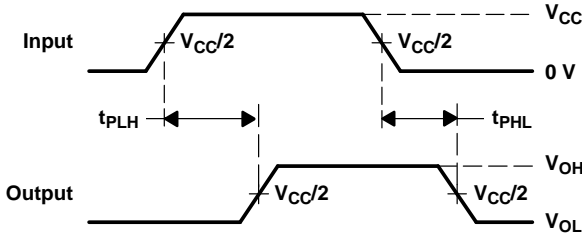


**LOAD CIRCUIT**

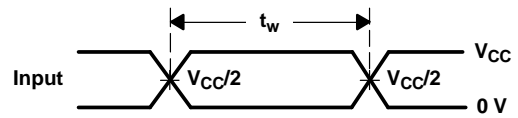
| TEST              | S1                |
|-------------------|-------------------|
| $t_{pd}$          | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |



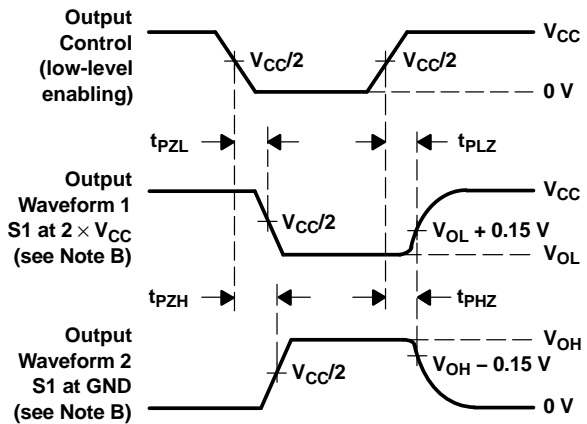
**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS**  
**PULSE DURATION**

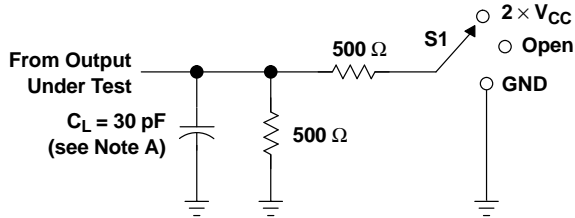


**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

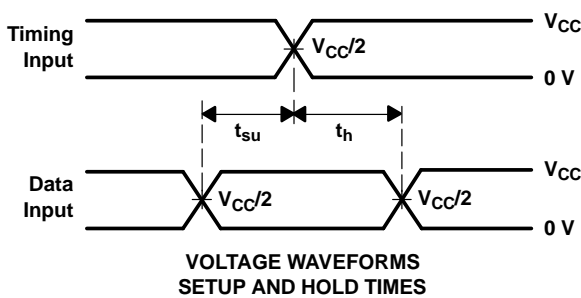
**Figure 4. Load Circuit and Voltage Waveforms**

**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

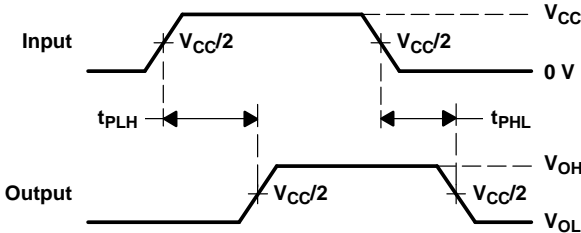


| TEST              | S1                |
|-------------------|-------------------|
| $t_{pd}$          | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |

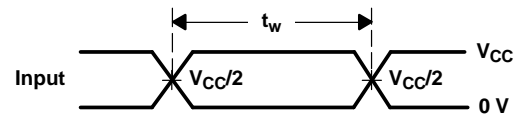
**LOAD CIRCUIT**



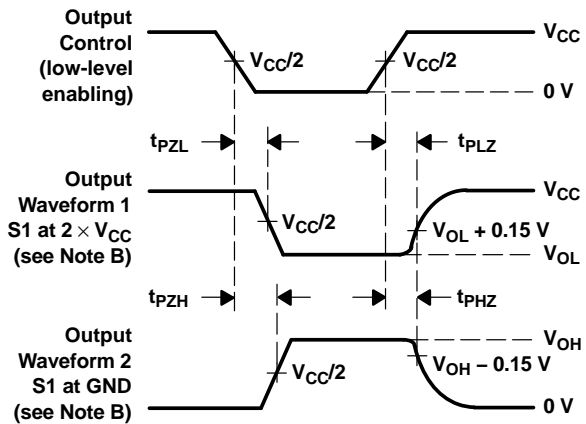
**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

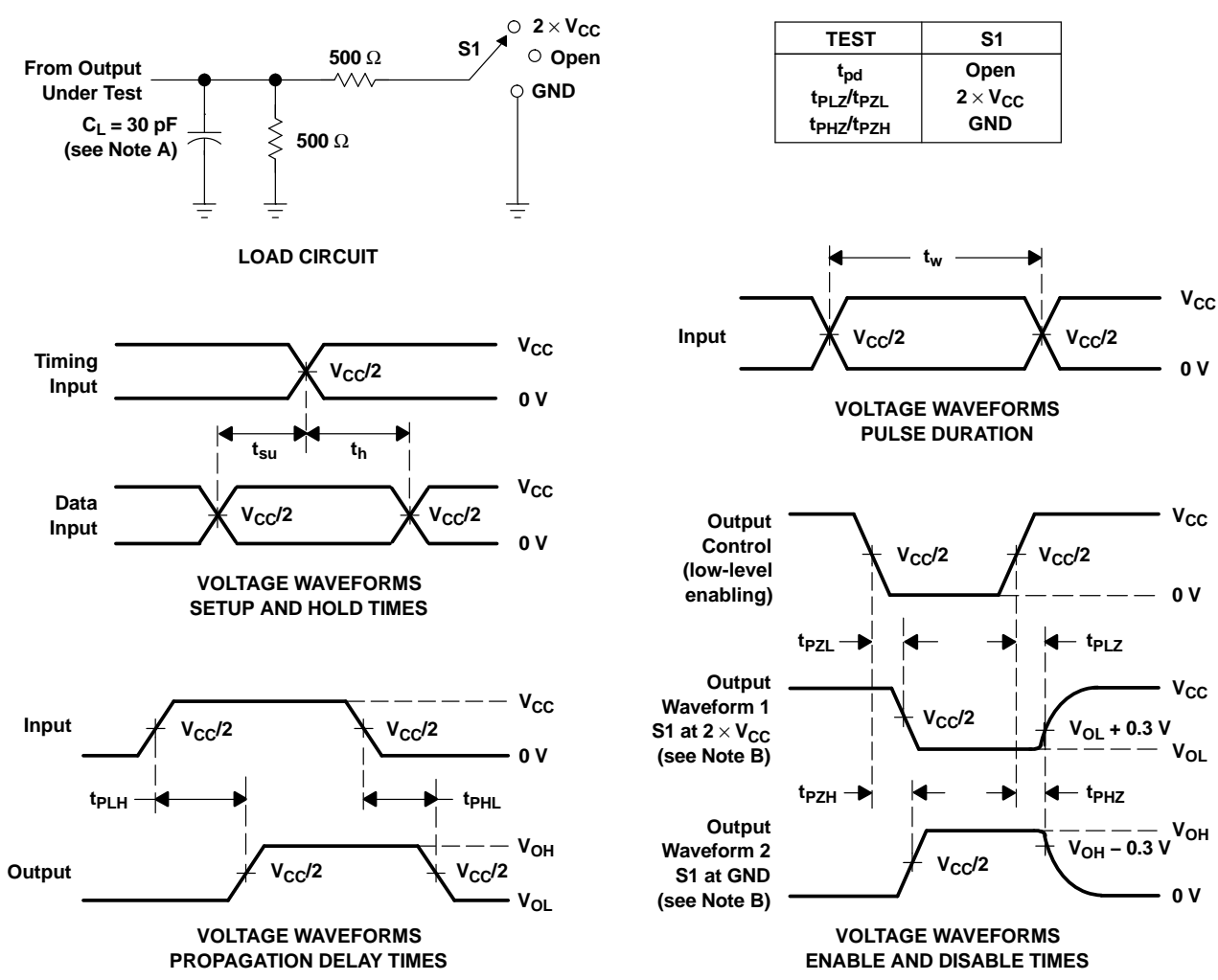
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 5. Load Circuit and Voltage Waveforms**

**SN74AVC16646**  
**16-BIT BUS TRANSCIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

SCES181F—DECEMBER 1998—REVISED JUNE 2005

**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 6. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74AVC16646DGGRE4 | ACTIVE                | TSSOP        | DGG             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74AVC16646DGGRG4 | ACTIVE                | TSSOP        | DGG             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74AVC16646DGVRE4 | ACTIVE                | TVSOP        | DGV             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74AVC16646DGVRG4 | ACTIVE                | TVSOP        | DGV             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AVC16646DGGR | ACTIVE                | TSSOP        | DGG             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AVC16646DGVR | ACTIVE                | TVSOP        | DGV             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

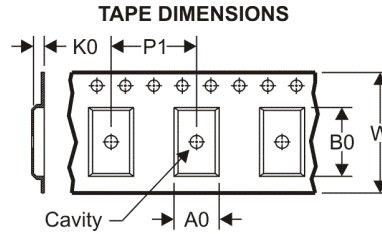
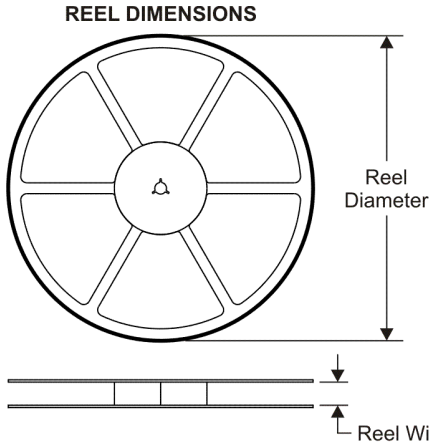
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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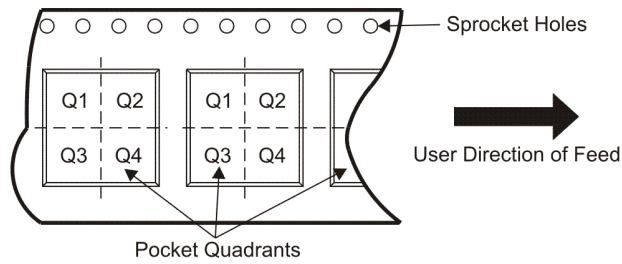


**TAPE AND REEL INFORMATION**



|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

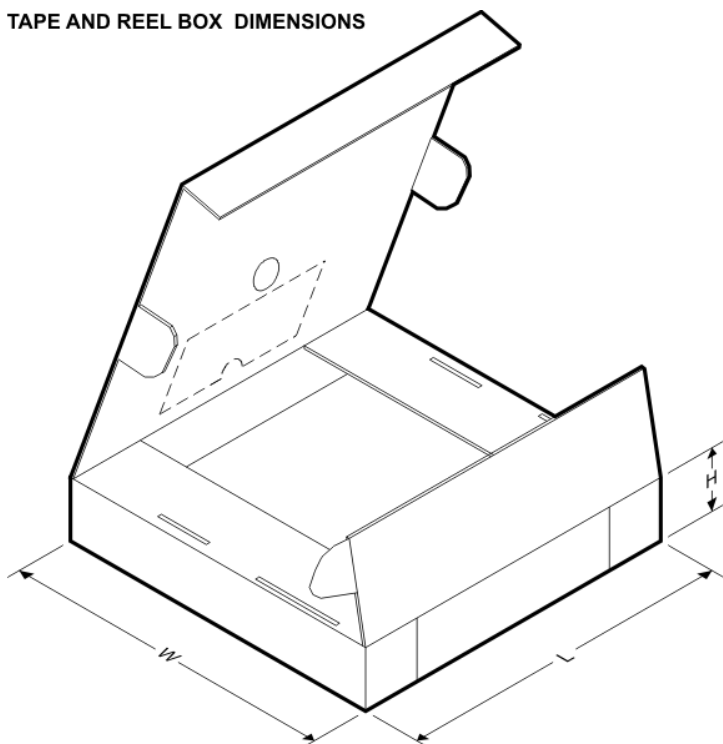
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AVC16646DGGR | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74AVC16646DGVR | TVSOP        | DGV             | 56   | 2000 | 330.0              | 24.4               | 6.8     | 11.7    | 1.6     | 12.0    | 24.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

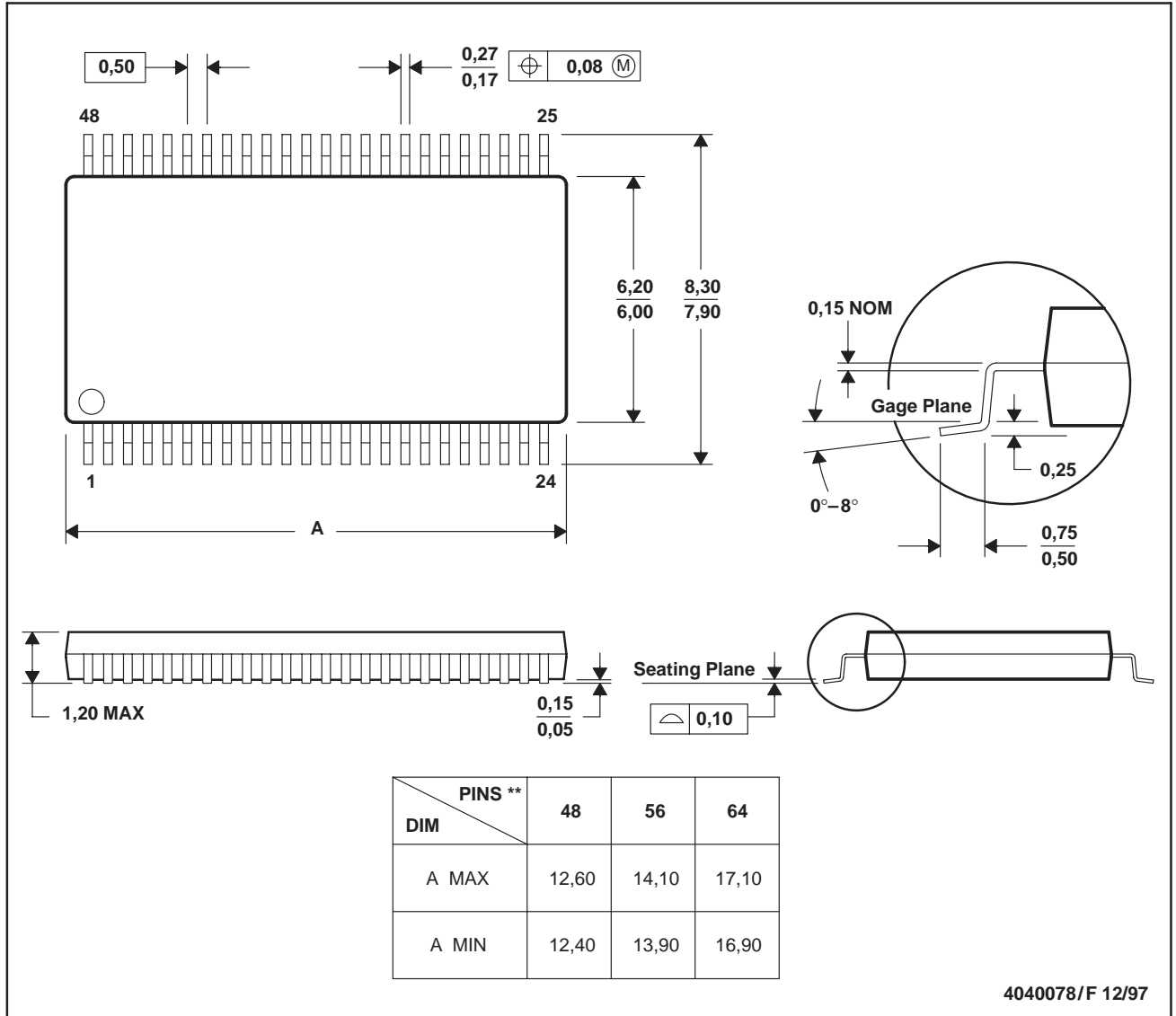
| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AVC16646DGGR | TSSOP        | DGG             | 56   | 2000 | 346.0       | 346.0      | 41.0        |
| SN74AVC16646DGVR | TVSOP        | DGV             | 56   | 2000 | 346.0       | 346.0      | 41.0        |

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

**DGG (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



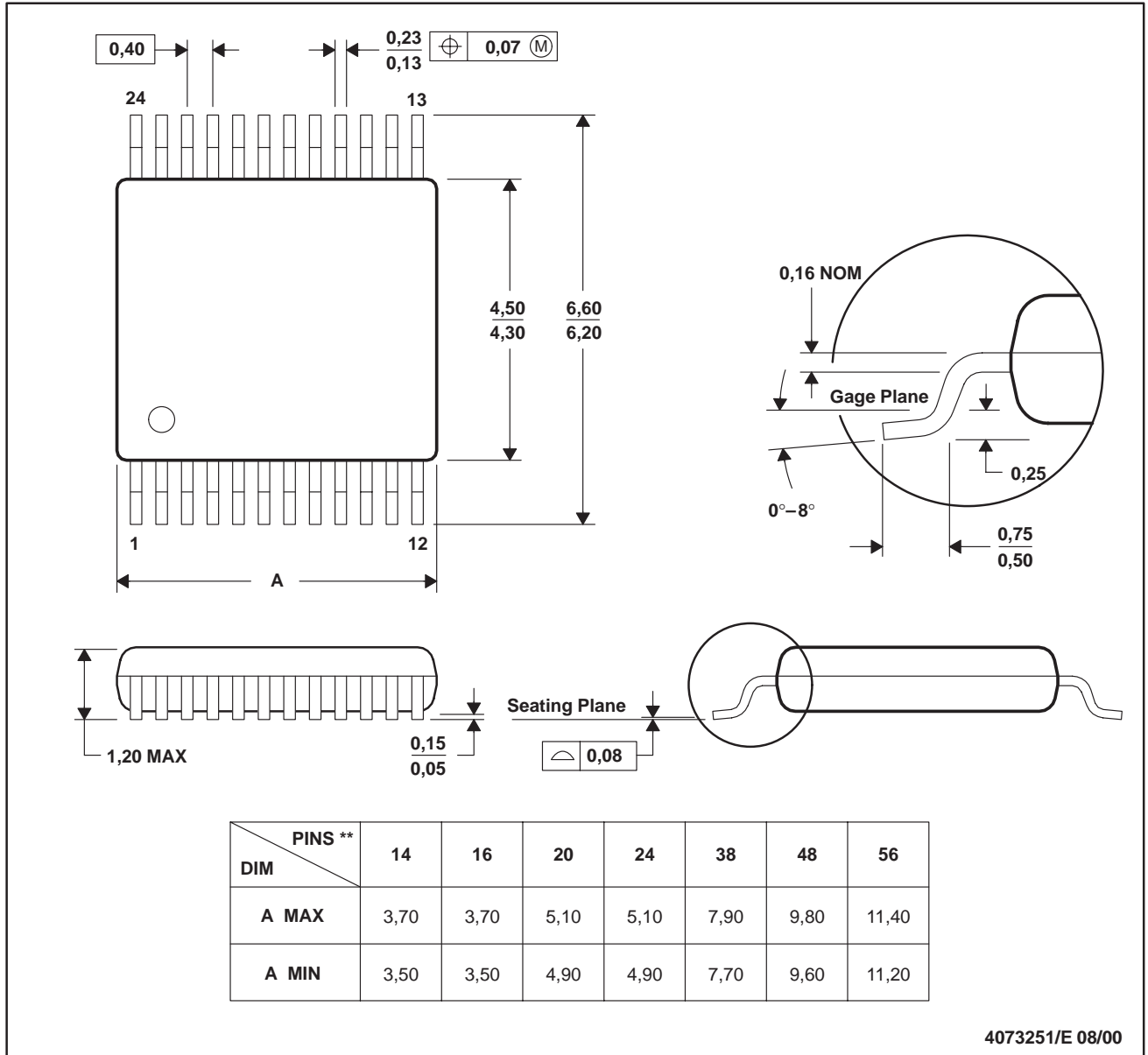
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

**DGV (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

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