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CD54HC194, CD74HC194, CD74HCT194

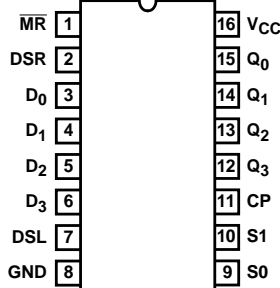
High-Speed CMOS Logic 4-Bit Bidirectional Universal Shift Register

Features

- Four Operating Modes
 - Shift Right, Shift Left, Hold and Reset
- Synchronous Parallel or Serial Operation
- Typical $f_{MAX} = 60\text{MHz}$ at $V_{CC} = 5\text{V}$, $C_L = 15\text{pF}$, $T_A = 25^\circ\text{C}$
- Asynchronous Master Reset
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5\text{V}$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8\text{V}$ (Max), $V_{IH} = 2\text{V}$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu\text{A}$ at V_{OL} , V_{OH}

Pinout

CD54HC194 (CERDIP)
CD74HC194 (PDIP, SOIC, SOP, TSSOP)
CD74HCT194 (PDIP)
TOP VIEW



Description

The 'HC194 and CD74HCT194 are 4-bit shift registers with Asynchronous Master Reset (\overline{MR}). In the parallel mode (S_0 and S_1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP). During parallel loading serial data flow is inhibited. Shift left and shift right are accomplished synchronously on the positive clock edge with serial data entered at the shift left (DSL) serial input for the shift left mode, and at the shift right (DSR) serial input for the shift right mode. Clearing the register is accomplished by a Low applied to the Master Reset (\overline{MR}) pin.

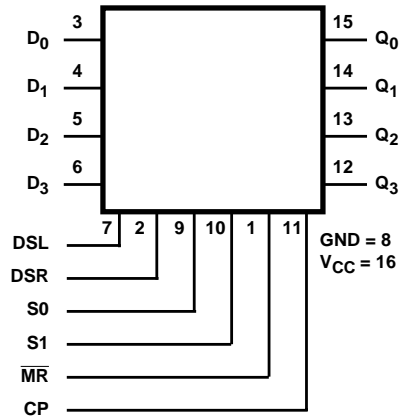
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC194F3A	-55 to 125	16 Ld CERDIP
CD74HC194E	-55 to 125	16 Ld PDIP
CD74HC194M	-55 to 125	16 Ld SOIC
CD74HC194MT	-55 to 125	16 Ld SOIC
CD74HC194M96	-55 to 125	16 Ld SOIC
CD74HC194NSR	-55 to 125	16 Ld SOP
CD74HC194PW	-55 to 125	16 Ld TSSOP
CD74HC194PWR	-55 to 125	16 Ld TSSOP
CD74HC194PWT	-55 to 125	16 Ld TSSOP
CD74HCT194E	-55 to 125	16 Ld PDIP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CD54HC194, CD74HC194, CD74HCT194

Functional Diagram



TRUTH TABLE

OPERATING MODE	INPUTS							OUTPUT			
	CP	MR	S1	S0	DSR	DSL	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset (Clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (Do Nothing)	X	H	I	I	X	X	X	q ₀	q ₁	q ₂	q ₃
Shift Left	↑	H	h	I	X	I	X	q ₁	q ₂	q ₃	L
	↑	H	h	I	X	h	X	q ₁	q ₂	q ₃	H
Shift Right	↑	H	I	h	I	X	X	L	q ₀	q ₁	q ₂
	↑	H	I	h	h	X	X	H	q ₀	q ₁	q ₂
Parallel Load	↑	H	h	h	X	X	d _n	d ₀	d ₁	d ₂	d ₃

H = High Voltage Level,

h = High Voltage Level One Set-up Time Prior To The Low to High Clock Transition,

L = Low Voltage Level,

I = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition,

d_n (q_n) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low To High Clock Transition,

X = Don't Care,

↑ = Transition from Low to High Level

CD54HC194, CD74HC194, CD74HCT194

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	$\pm 50mA$

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 2):	
E (PDIP) Package	67°C/W
M (SOIC) Package	73°C/W
NS (SOP) Package	64°C/W
PW (TSSOP) Package	108°C/W
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range (T_A)	-55°C to 125°C
Supply Voltage Range, V_{CC}	
HC Types	2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V

CD54HC194, CD74HC194, CD74HCT194

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	± 0.1	-	± 1	-	± 1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 3)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case ($V_I = 2.4V$, $V_{CC} = 5.5V$) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
CP	0.6
\overline{MR}	0.55
DSL, DSR, D_n	0.25
S_n	1.10

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360 μA max at 25°C.

CD54HC194, CD74HC194, CD74HCT194

Prerequisite For Switching Function

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
Max. Clock Frequency (Figure 1)	f _{MAX}	-	2	6	-	5	-	4	-	MHz
			4.5	30	-	24	-	20	-	MHz
			6	35	-	28	-	23	-	MHz
MR Pulse Width (Figure 2)	t _W	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Clock Pulse Width (Figure 1)	t _W	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Set-up Time Data to Clock (Figure 3)	t _{SU}	-	2	70	-	90	-	105	-	ns
			4.5	14	-	18	-	21	-	ns
			6	12	-	15	-	19	-	ns
Removal Time, MR to Clock (Figure 2)	t _{REM}	-	2	60	-	75	-	90	-	ns
			4.5	12	-	15	-	18	-	ns
			6	10	-	13	-	15	-	ns
Set-Up Time S1, S0 to Clock (Figure 4)	t _{SU}	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Set-up Time DSL, DSR to Clock (Figure 4)	t _{SU}	-	2	70	-	90	-	105	-	ns
			4.5	14	-	18	-	21	-	ns
			6	12	-	15	-	18	-	ns
Hold Time S1, S0 to Clock (Figure 4)	t _H	-	2	0	-	0	-	0	-	ns
			4.5	0	-	0	-	0	-	ns
			6	0	-	0	-	0	-	ns
Hold Time Data to Clock (Figure 3)	t _H	-	2	0	-	0	-	0	-	ns
			4.5	0	-	0	-	0	-	ns
			6	0	-	0	-	0	-	ns
HCT TYPES										
Max. Clock Frequency (Figure 1)	f _{MAX}	-	4.5	27	-	22	-	18	-	MHz
MR Pulse Width (Figure 2)	t _W	-	4.5	16	-	20	-	24	-	ns
Clock Pulse Width (Figure 1)	t _W	-	4.5	16	-	20	-	24	-	ns
Set-up Time, Data to Clock (Figure 3)	t _{SU}	-	4.5	14	-	18	-	21	-	ns
Removal Time MR to Clock (Figure 2)	t _{REM}	-	4.5	12	-	15	-	18	-	ns

Prerequisite For Switching Function (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
Set-up Time S1, S0 to Clock (Figure 4)	t _{SU}	-	4.5	20	-	25	-	30	-	ns
Set-up Time DSL, DSR to Clock (Figure 4)	t _{SU}	-	4.5	14	-	18	-	21	-	ns
Hold Time S1, S0 to Clock (Figure 4)	t _H	-	4.5	0	-	0	-	0	-	ns
Hold Time Data to Clock (Figure 3)	t _H	-	4.5	0	-	0	-	0	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, Clock to Output (Figure 1)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
			6	-	30	37	45	ns
Propagation Delay, Clock to Q	t _{PLH} , t _{PHL}	-	5	14	-	-	-	ns
Output Transition Time (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Propagation Delay, MR to Output (Figure 2)	t _{PHL}	C _L = 50pF	2	-	140	175	210	ns
			4.5	-	28	35	42	ns
			6	-	24	30	36	ns
Input Capacitance	C _{IN}	-	-	-	10	10	10	pF
Maximum Clock Frequency	f _{MAX}	-	5	60	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	55	-	-	-	pF
HCT TYPES								
Propagation Delay, Clock to Output (Figure 1)	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	37	46	56	ns
Propagation Delay, Clock to Q	t _{PLH} , t _{PHL}	-	5	15	-	-	-	ns
Output Transition Times (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	15	19	22	ns
Propagation Delay, MR to Output (Figure 2)	t _{PHL}	C _L = 50pF	4.5	-	40	50	60	ns
Input Capacitance	C _{IN}	-	-	-	10	10	10	pF
Maximum Clock Frequency	f _{MAX}	-	5	50	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	60	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

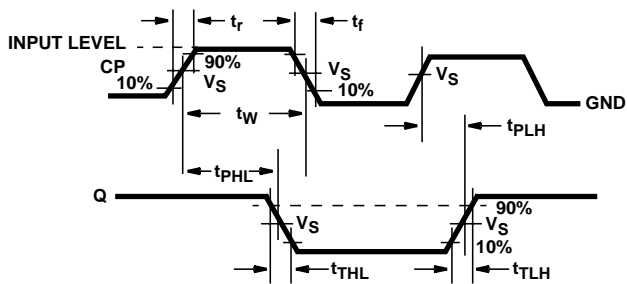


FIGURE 1. CLOCK PREREQUISITE TIMES AND PROPAGATION AND OUTPUT TRANSITION TIMES

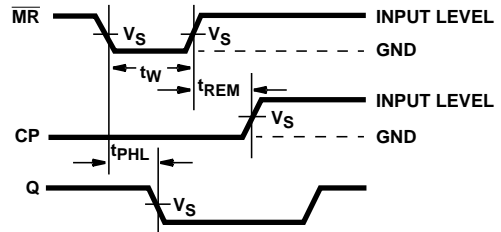


FIGURE 2. MASTER RESET PREREQUISITE TIMES AND PROPAGATION DELAYS

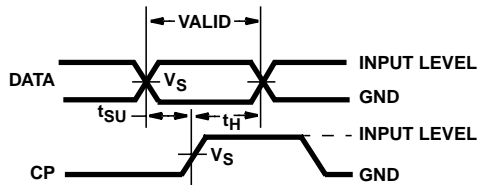


FIGURE 3. DATA PREREQUISITE TIMES

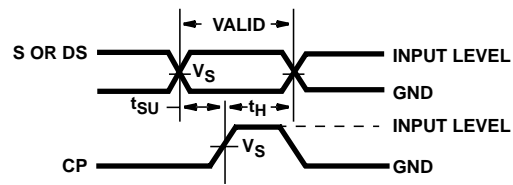


FIGURE 4. PARALLEL LOAD OR SHIFT-LEFT/SHIFT-RIGHT PREREQUISITE TIMES

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8682601EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8682601EA CD54HC194F3A	Samples
CD54HC194F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8682601EA CD54HC194F3A	Samples
CD74HC194E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC194E	Samples
CD74HC194M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC194M	Samples
CD74HC194M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC194M	Samples
CD74HC194PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ194	Samples
CD74HC194PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ194	Samples
CD74HC194PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ194	Samples
CD74HC194PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ194	Samples
CD74HCT194E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT194E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC194, CD74HC194 :

● Catalog: [CD74HC194](#)

● Military: [CD54HC194](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

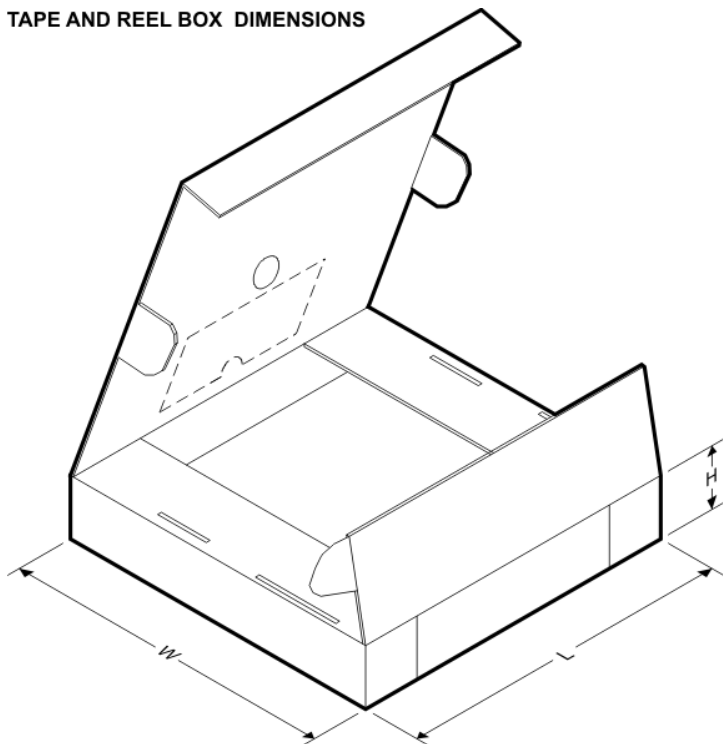
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC194M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC194PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC194PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



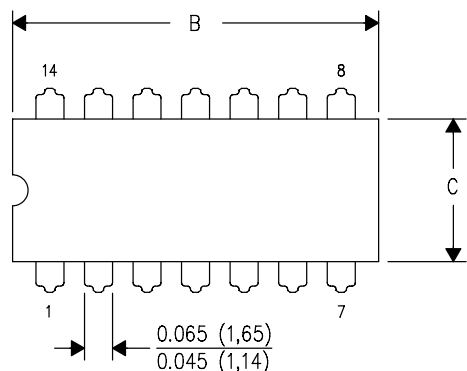
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC194M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC194PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC194PWT	TSSOP	PW	16	250	367.0	367.0	35.0

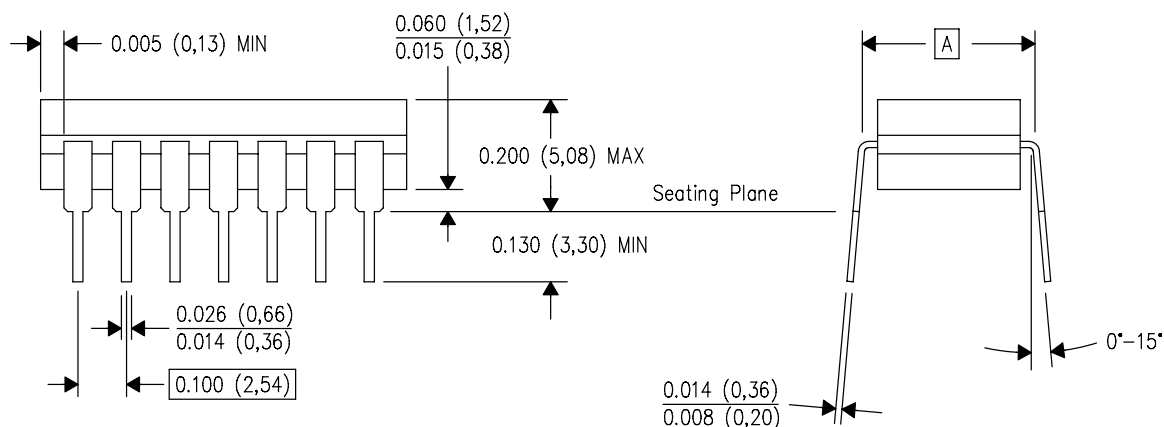
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

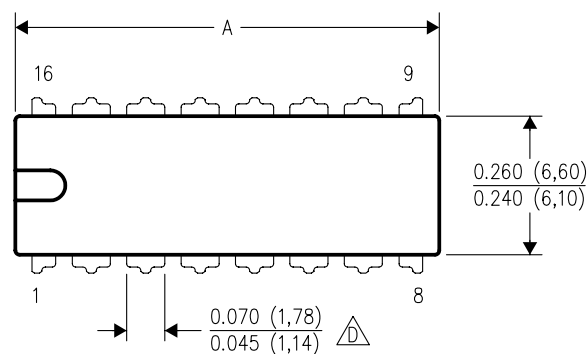
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

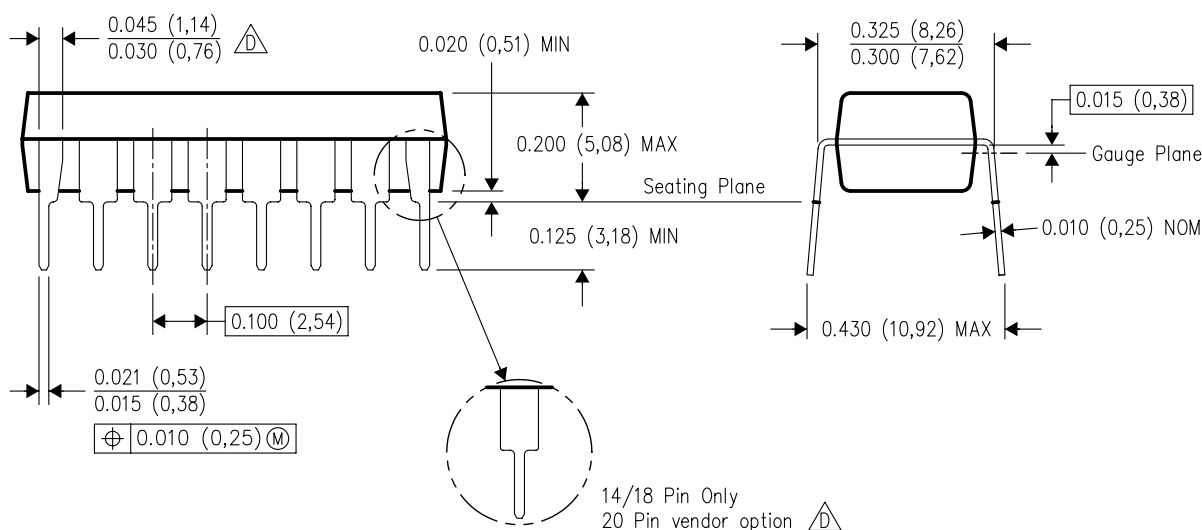
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



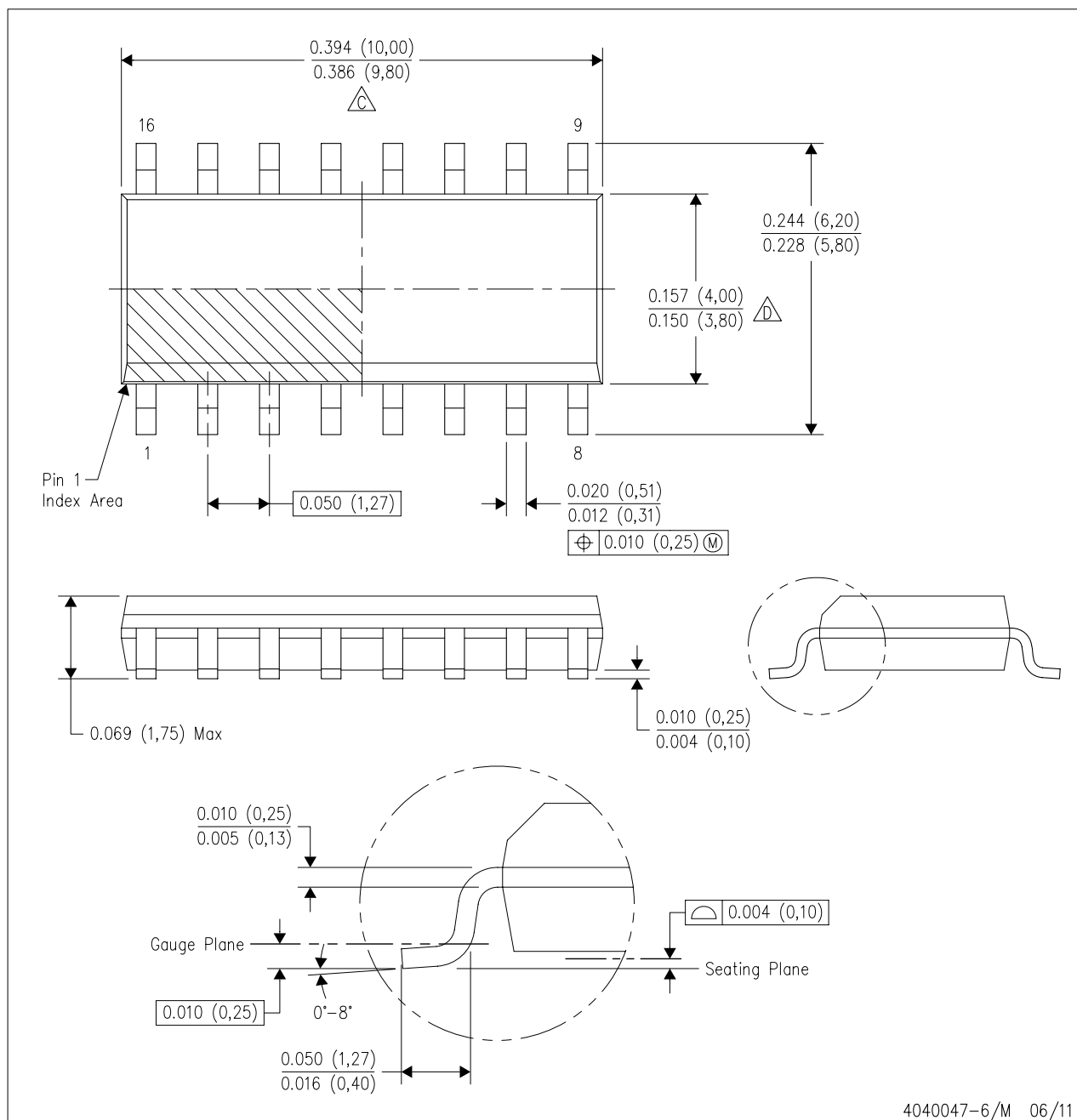
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



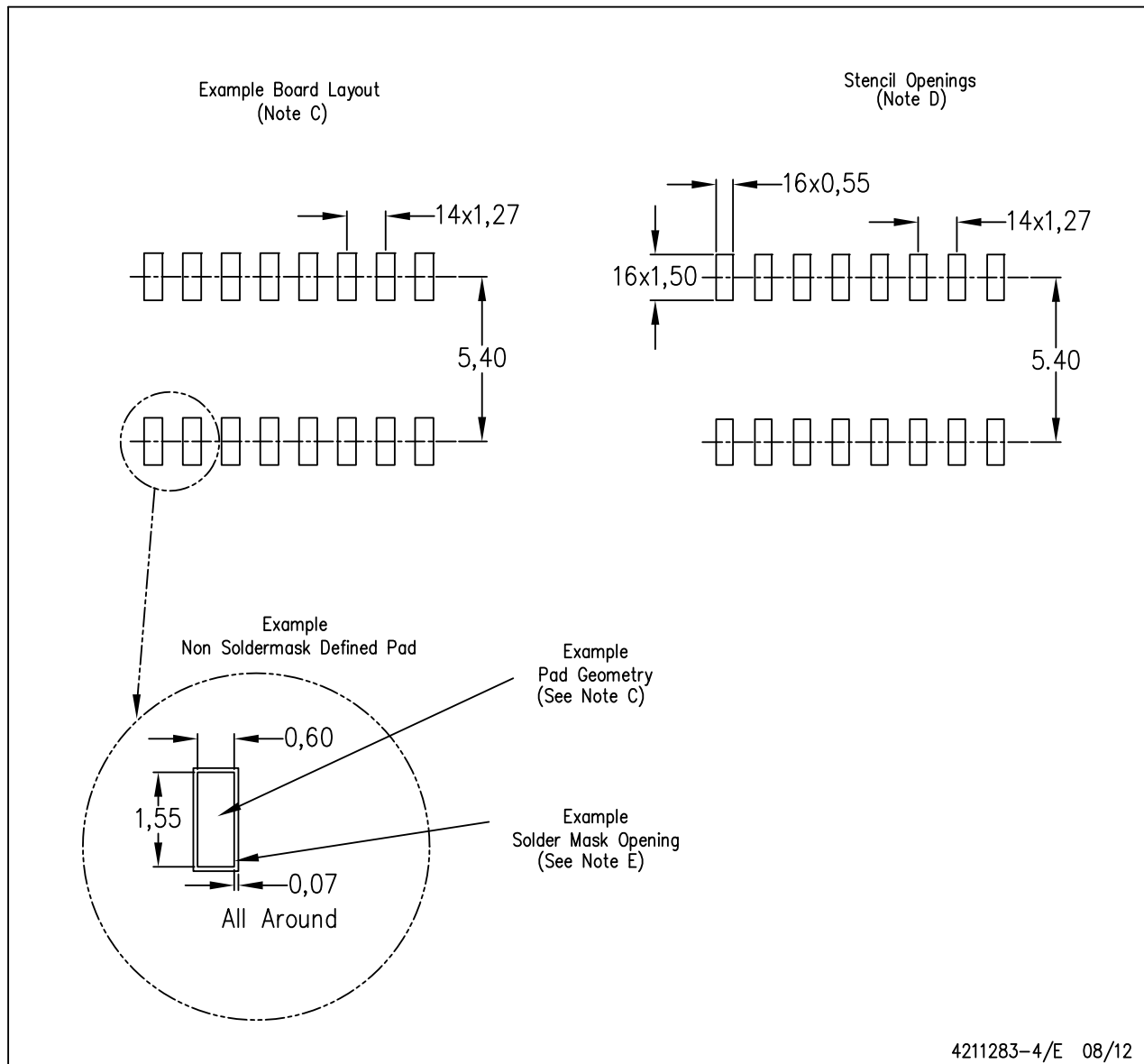
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

LAND PATTERN DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

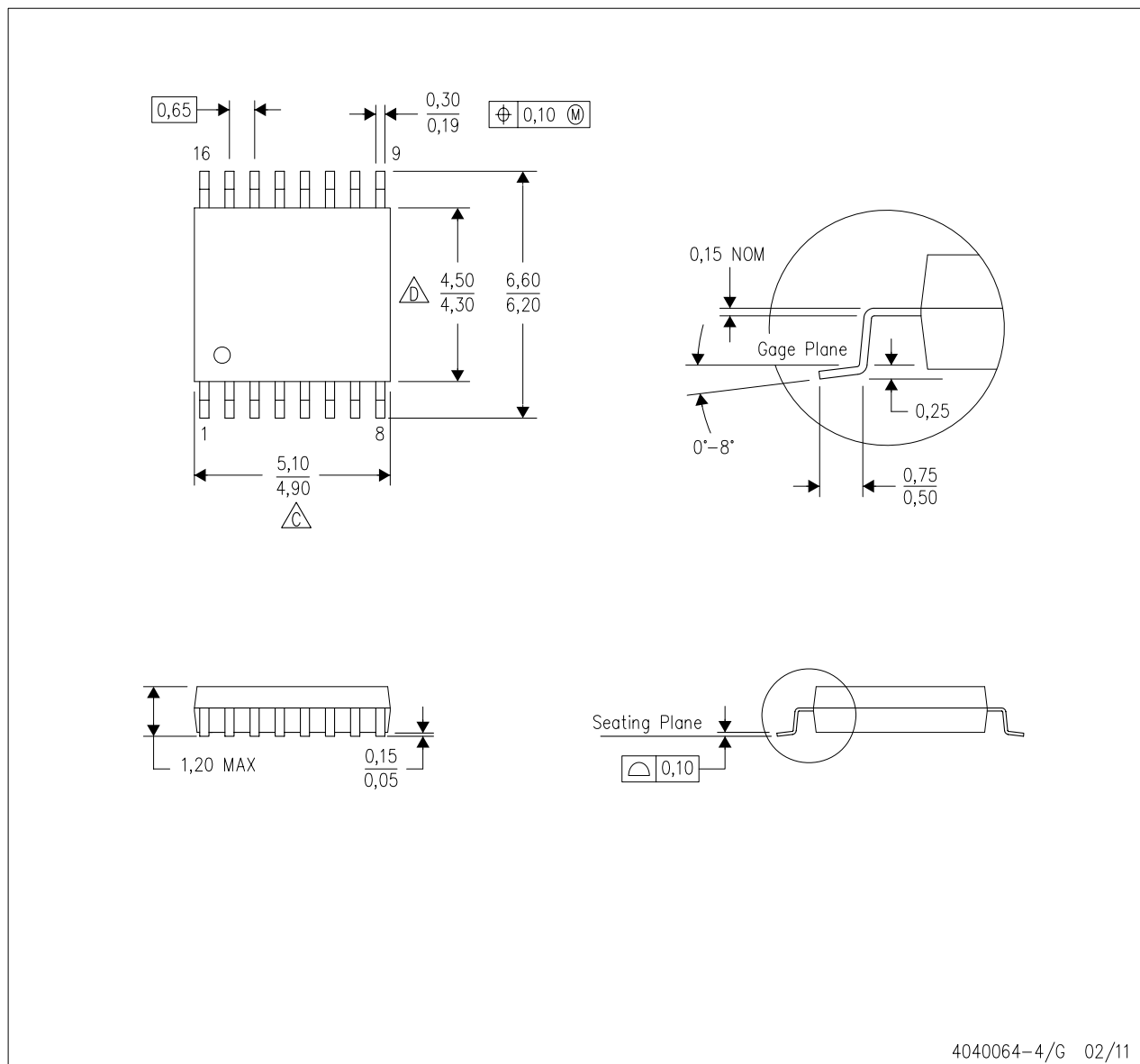


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

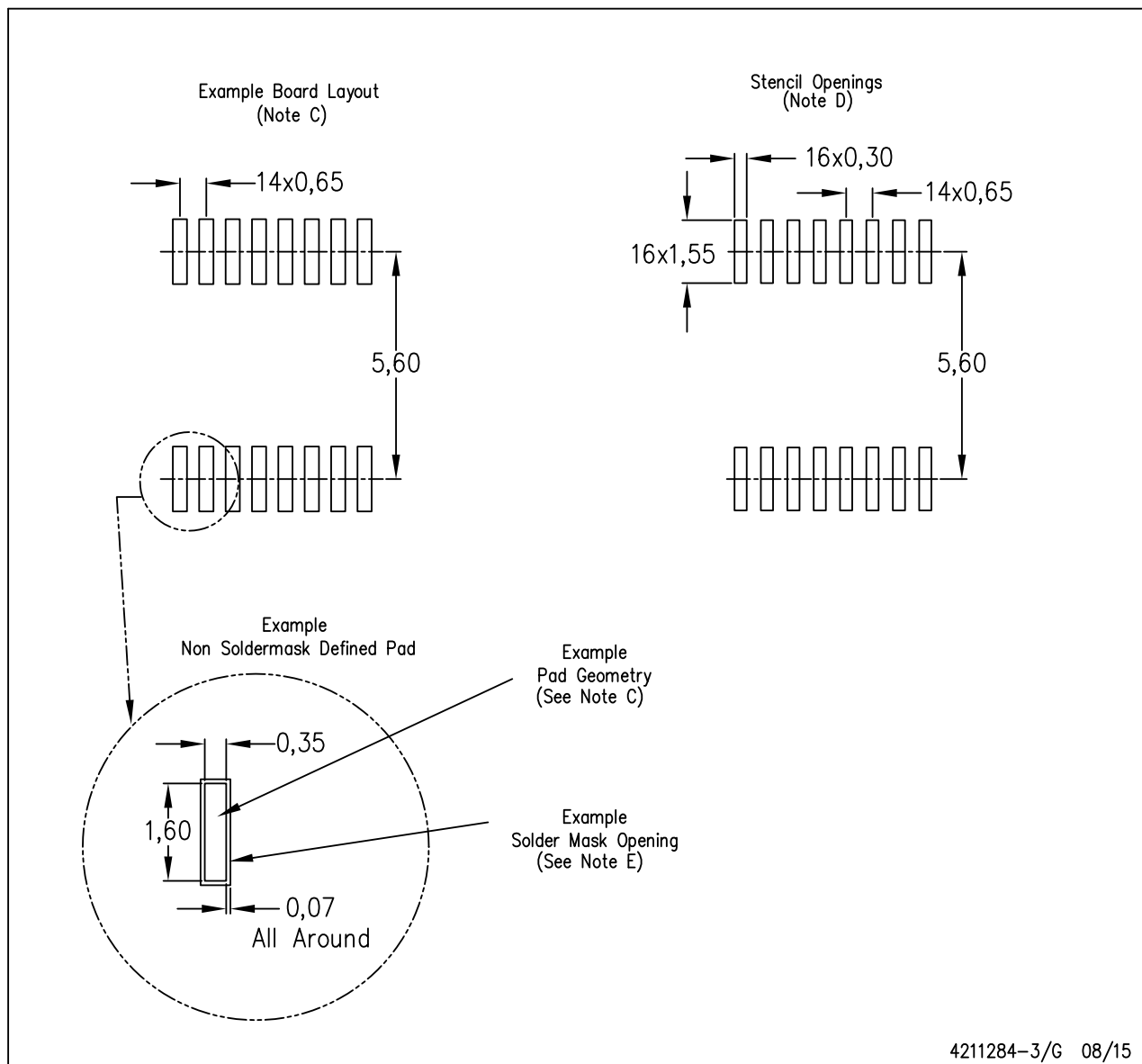


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

LAND PATTERN DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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