FAIRCHILD SEMICONDUCTOR®

July 2013

FDMC89521L

Dual N-Channel PowerTrench® MOSFET

60 V, 8.2 A, 17 mΩ

Features

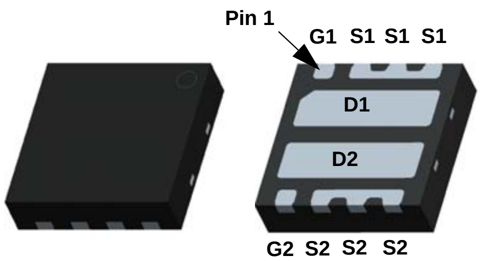
- Max $r_{DS(on)}$ = 17 mΩ at V_{GS} = 10 V, I_D = 8.2 A
- Max $r_{DS(on)}$ = 27 mΩ at V_{GS} = 4.5 V, I_D = 6.7 A
- Termination is Lead-free
- RoHS Compliant

General Description

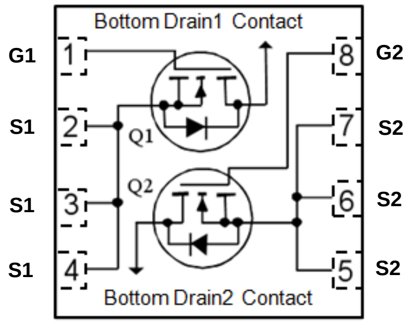
This device includes two 60 V N-Channel MOSFETs in a dual Power 33 (3 mm X 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

Applications

- Battery Protection
- Load Switching
- Bridge Topologies



Power 33



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous T_A = 25 °C (Note 1a)	8.2	A
	-Pulsed	40	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	32	mJ
P_D	Power Dissipation T_A = 25 °C (Note 1a)	1.9	W
	Power Dissipation T_A = 25 °C (Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	155	

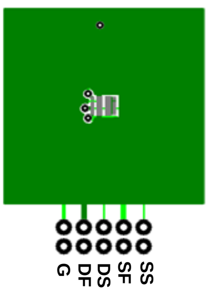
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC89521L	FDMC89521L	Power 33	13 ”	12 mm	3000 units

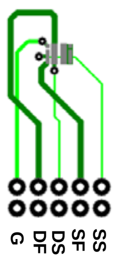
Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		30		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 8.2 A		13	17	mΩ
		V_{GS} = 4.5 V, I_D = 6.7 A		21	27	
		V_{GS} = 10 V, I_D = 8.2 A, T_J = 125 °C		20	26	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 8.2 A		28		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz		1228	1635	pF
C_{oss}	Output Capacitance			243	325	pF
C_{rss}	Reverse Transfer Capacitance			10	15	pF
R_g	Gate Resistance			0.7		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 8.2 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		7.9	16	ns
t_r	Rise Time			2.1	10	ns
$t_{d(off)}$	Turn-Off Delay Time			18	33	ns
t_f	Fall Time			1.7	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 30 V, I_D = 8.2 A		17	24	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 30 V, I_D = 8.2 A		7.9	12	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 30 V, I_D = 8.2 A		3.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			1.9		nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 8.2 A (Note 2)		0.85	1.3	V
		V_{GS} = 0 V, I_S = 1.6 A (Note 2)		0.75	1.2	
t_{rr}	Reverse Recovery Time	I_F = 8.2 A, di/dt = 100 A/μs		25	40	ns
Q_{rr}	Reverse Recovery Charge			11	20	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 65 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 155 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 32 mJ is based on starting T_J = 25 °C, L = 1 mH, I_{AS} = 8 A, V_{DD} = 54 V, V_{GS} = 10 V. 100% tested at L = 3 mH, I_{AS} = 5.4 A.

Typical Characteristics T_J = 25 °C unless otherwise noted

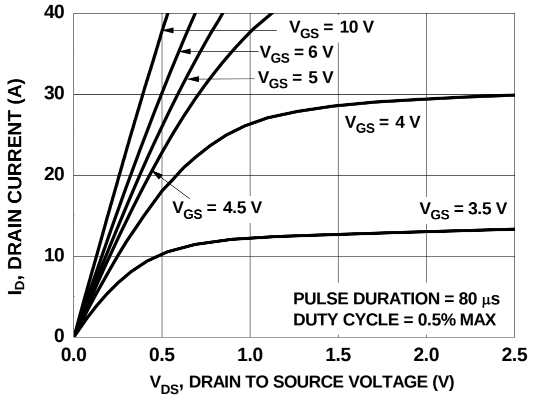


Figure 1. On Region Characteristics

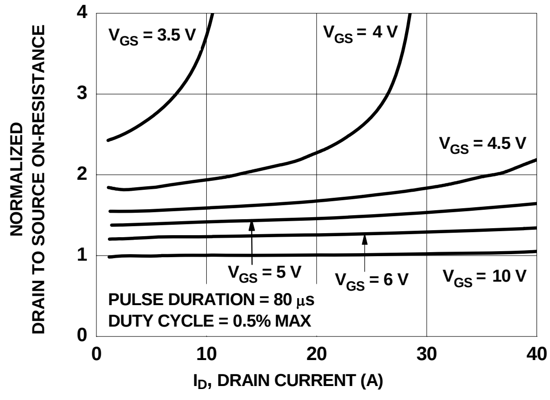


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

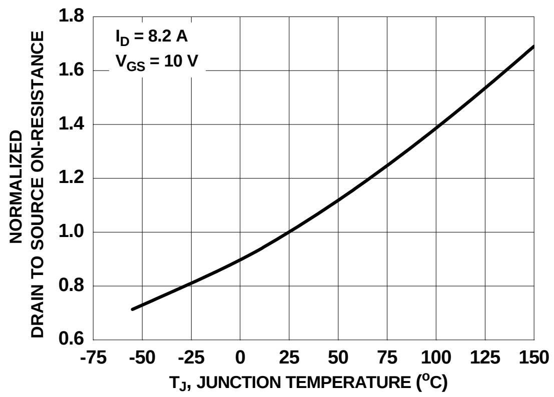


Figure 3. Normalized On Resistance vs Junction Temperature

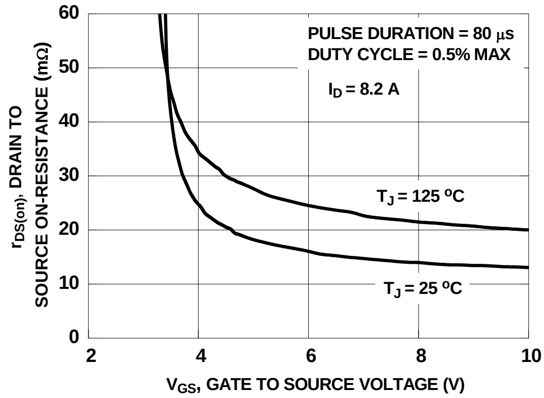


Figure 4. On-Resistance vs Gate to Source Voltage

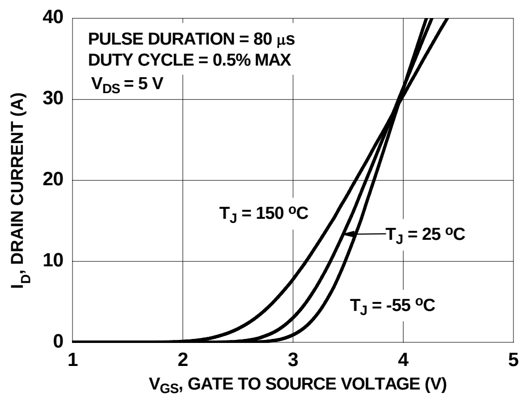


Figure 5. Transfer Characteristics

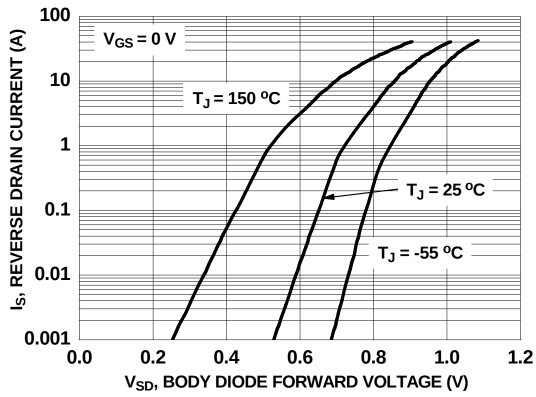


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

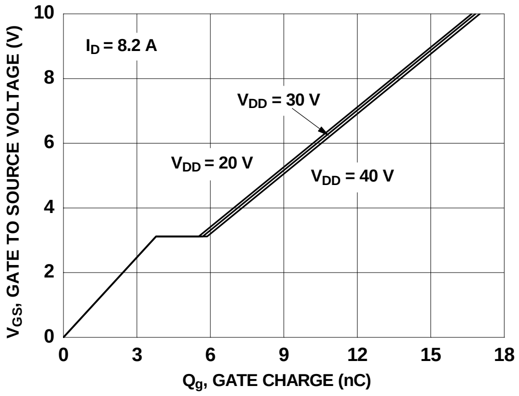


Figure 7. Gate Charge Characteristics

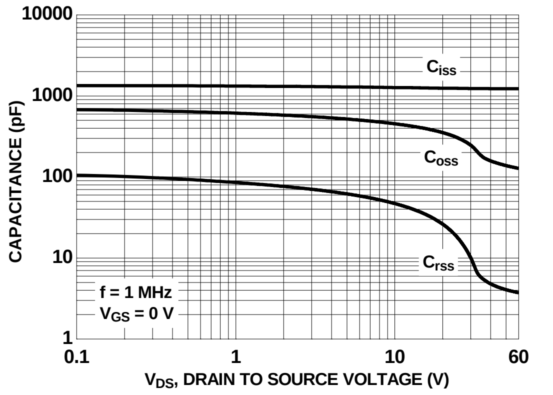


Figure 8. Capacitance vs Drain to Source Voltage

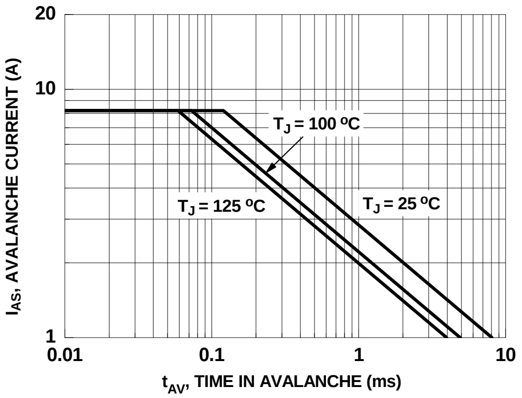


Figure 9. Unclamped Inductive Switching Capability

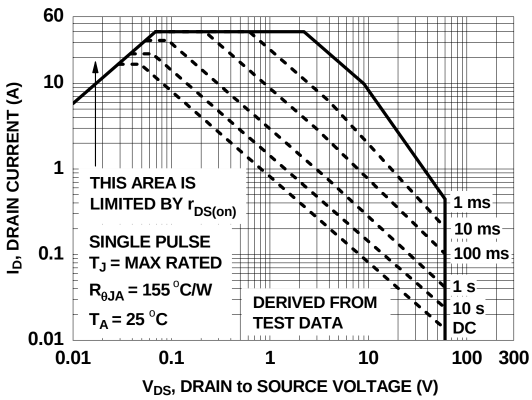


Figure 10. Forward Bias Safe Operating Area

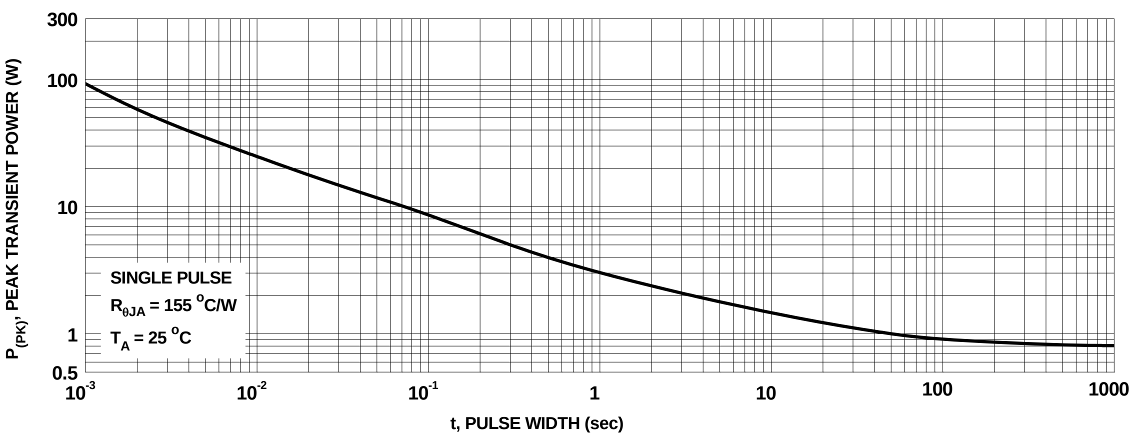


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

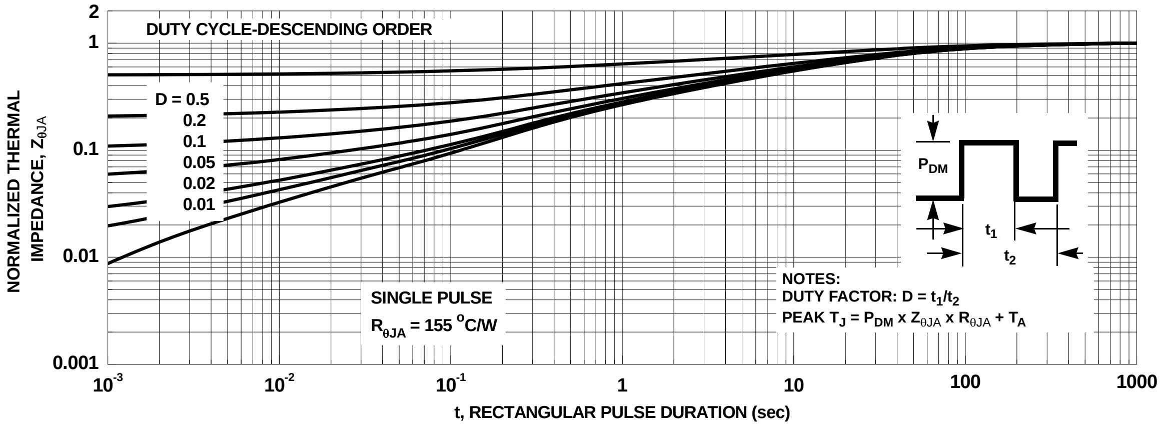
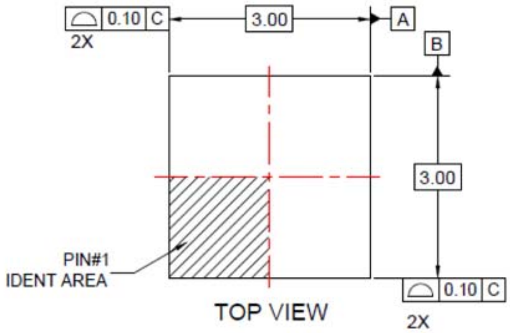
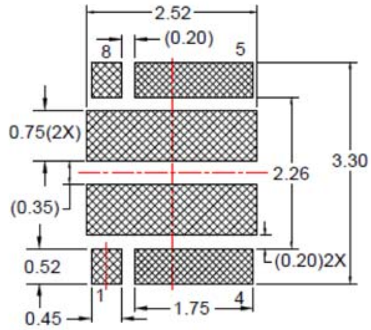


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

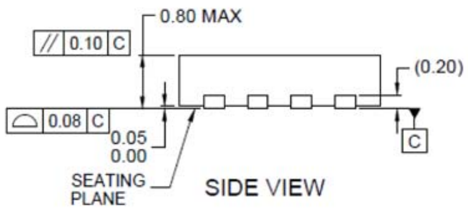
Dimensional Outline and Pad Layout



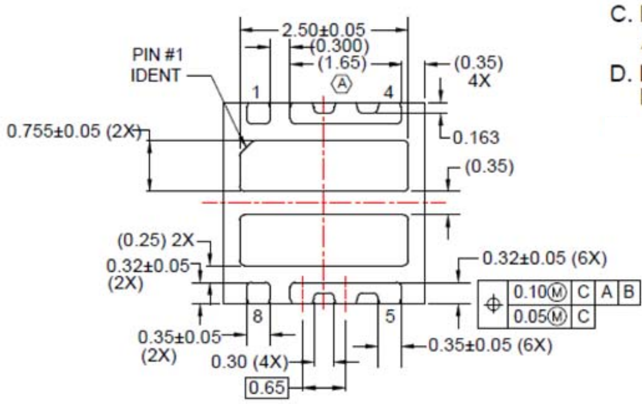
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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